An In-Situ Microcoaxial Fabrication and Attachment Strategy

Submitted By
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Abstract

Micro-coaxial cables (MCCs), with an outer diameter of 100 μm or less, enable a new microelectronics packaging platform that will reduce the time required to design and fabricate complex multi-chip microelectronic assemblies. Low-inductance MCCs for power distribution and 30-75 Ω MCCs for signal distribution, eliminate the need for lengthy simulations and fabrication processes, as in board design of photo-lithographically patterned microchips, because each individually shielded MCC provides sufficient isolation to prevent electro-magnetic interference (EMI) and crosstalk. The in-situ fabrication method presented here utilizes only conventional wire bonding and microfabrication techniques, providing a high-feasibility path toward a new interconnect paradigm based on MCCs.

Each cable measured consists of a 25.4 μm gold bond wire coated first with a dielectric and then a 5.0 μm thick gold shield. For power distribution, the dielectrics evaluated are 1.0 μm thick Parylene C dielectric and 100 nm thick HfO_2. Their characteristic impedances are measured to be 3.2-5.9 Ω and 0.11-0.18 Ω, respectively. A third MCC, appropriate for signals, has a 38 μm thick Parylene C dielectric and a characteristic impedance of 39-68 Ω. For a wire pitch of 0.51 mm cross-talk is -62 dB at 1 GHz for micro-coax. Cross-talk increases to -30 dB at 26.5 GHz.

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1 Introduction and Background

1.1 *System on Chip (SoC) vs. System in Package (SiP)*

A common architecture in packaging electronics is a 2D assembly of single chip modules, or multichip modules, on a printed circuit board (PCB) [1]. This arrangement allows for a packaging hierarchy where PCBs may be integrated with other PCBs or external hardware via a motherboard or backplane [2]. An image of a typical assembly using PCBs can be seen in Figure 1-1. This packaging scheme has allowed designers to focus on fabricating integrated circuits (ICs) on chips. The fabrication of complex circuits on a die is also referred to as System on Chip (SoC) [3] .

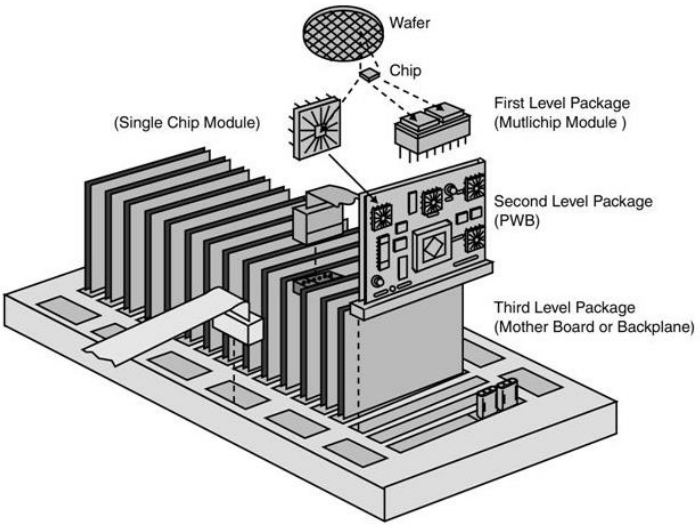


Figure 1-1 Packaging hierarchy using PCB technology. Image taken from [2].

SoC has reached some of its limitations in fabrication. As the need for miniaturization and more functionality on a chip increases, fabrication becomes more difficult to implement [3]. There are continuing demands for further miniaturization, complex power distribution, cost reduction, customization, and quick turnaround time for packaging technology. Devices such as smartphones, pacemakers, automotive systems, and other devices, parts of the "Internet of Things (IoT)" are

demanding more heterogeneous technology integration [4]. As a result, designers have begun to focus their attention to making complex systems at the package level by assembling two or more dissimilar chips into a package. This advanced packaging platform is known as the System in Package (SiP) [4].

SiP may incorporate a diverse set of devices such as microelectromechanical systems (MEMS), optical, RF, and biochemical components into one package [3]. A common form of SiP integration is die stacking. This method of integration utilizes wire bonding, flip chip bonding, and embedded conductors, within the die itself, to make interconnects between different dies possible [4]. This has moved packaging schemes from the 2D planar level to 3D. Figure 1-2 illustrates the different uses of interconnects to build a SiP device.

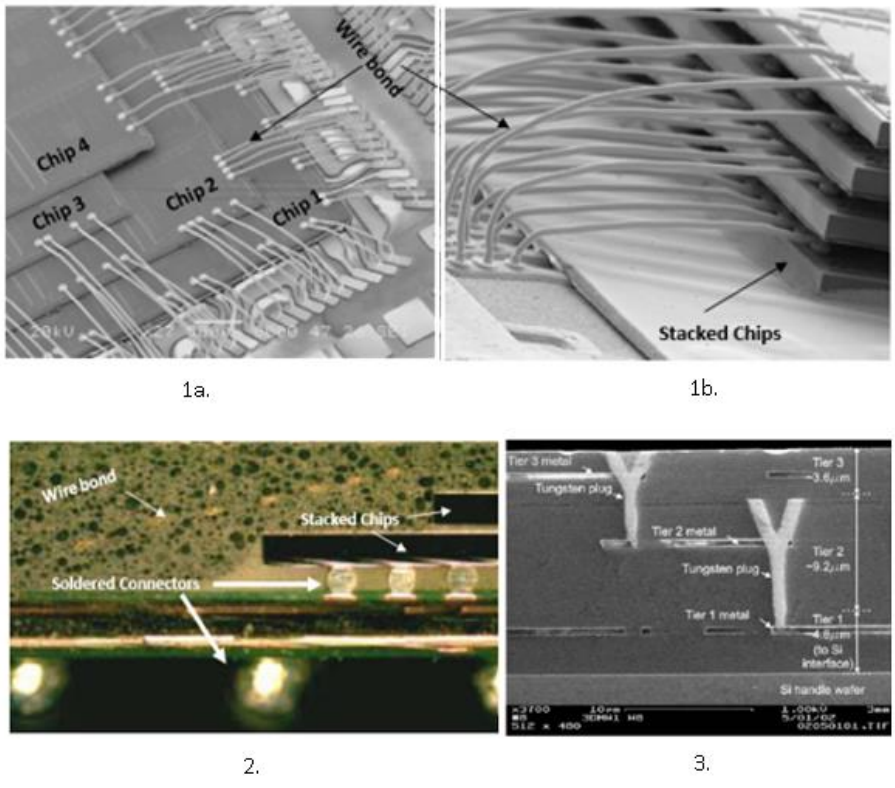


Figure 1-2 3D Packaging Techniques. 1a&1b) Die stacking. 2) Flip chip bonding. 3) Stacked dies interconnected within the dies by Tungsten conductors. All images are taken from [1].

1.1.1 SiP Market

In the SiP market, RF modules account for 66% of the market distribution (Figure 1-3) [4]. As a result, proper shielding between interconnects, especially when using interconnects as shown in Figure 1-2, is becoming increasingly important in SiP manufacturing. Additionally, interconnects used in RF modules will require low inductance for good power distribution, and low transmission loss for signal distribution. This will continue to be a priority as pitch between interconnects decreases, and IO counts increase.

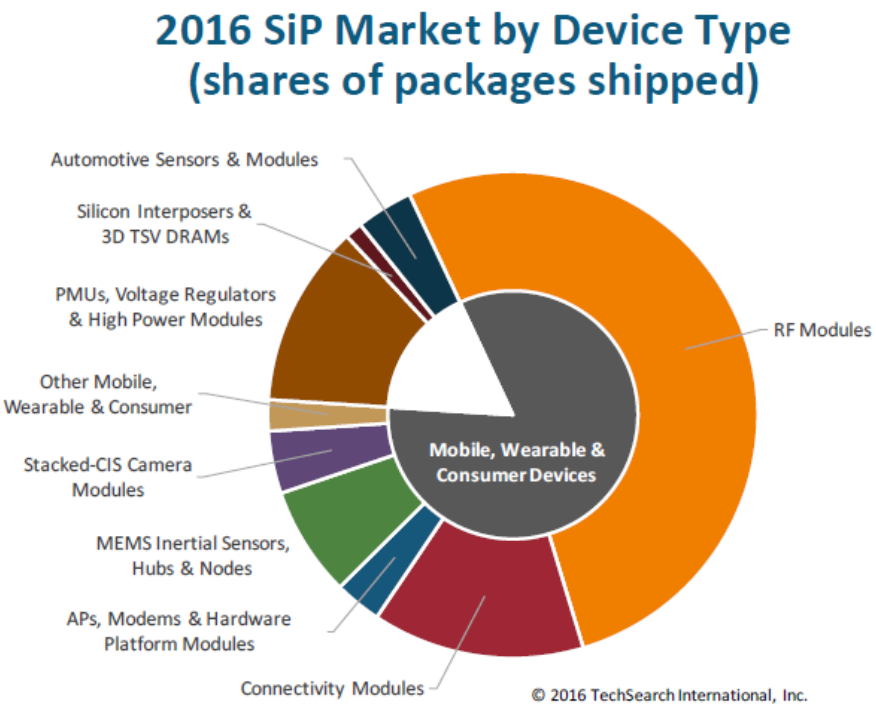
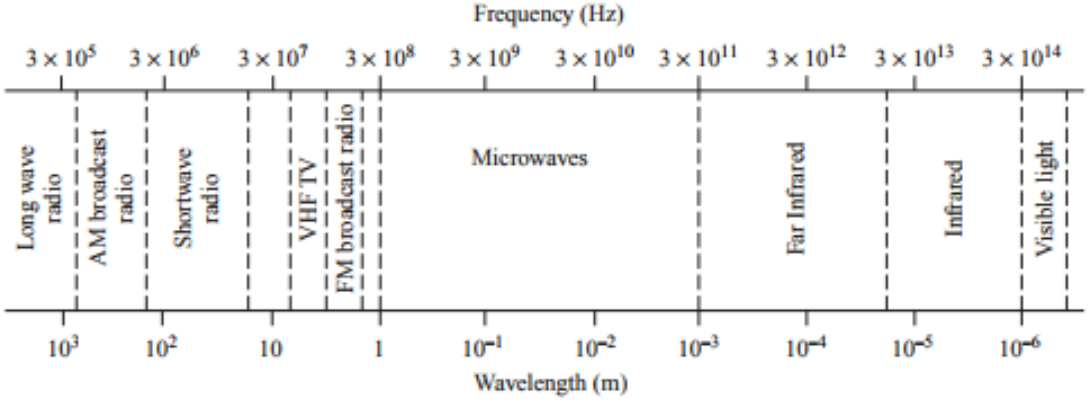


Figure 1-3 Break down of SiP market demands [4]. RF modules account for the majority the SiP market.

1.2 *Radio Frequency Waves and Microwaves*

A primary focus for this thesis is packaging of high frequency modules. Radio frequency (RF) waves and microwaves typically have alternate current (AC) signals with frequencies between 100 MHz – 1000 GHz [6]. The electromagnetic spectrum shown in Figure 1-4 illustrate that RF frequencies consists of waves that range from Very High Frequencies (VHF) of 30 – 300 MHz to

Ultra High Frequencies of 300-3000 MHz. Microwaves consists of even higher frequencies usually covering a range between 3 - 300 GHz and with wavelengths on the order of 10 cm to 1 mm [6]. Due to the high frequencies of RF waves and microwaves, circuit elements cannot be analyzed using standard Kirchhoff-style circuit theory, but instead through electromagnetic and transmission line theory. At these high frequencies voltage and current vary in magnitude and in phase along the physical lengths of devices that use RF and Microwave technology. This is especially true in microsystems where the wavelengths of AC signals are comparable to electrical lengths [6].



Typical Frequencies	
AM broadcast band	535–1605 kHz
Short wave radio band	3–30 MHz
FM broadcast band	88–108 MHz
VHF TV (2–4)	54–72 MHz
VHF TV (5–6)	76–88 MHz
UHF TV (7–13)	174–216 MHz
UHF TV (14–83)	470–890 MHz
US cellular telephone	824–849 MHz
	869–894 MHz
European GSM cellular	880–915 MHz
	925–960 MHz
GPS	1575.42 MHz
	1227.60 MHz
Microwave ovens	2.45 GHz
US DBS	11.7–12.5 GHz
US ISM bands	902–928 MHz
	2.400–2.484 GHz
	5.725–5.850 GHz
US UWB radio	3.1–10.6 GHz

Approximate Band Designations	
Medium frequency	300 kHz–3 MHz
High frequency (HF)	3 MHz–30 MHz
Very high frequency (VHF)	30 MHz–300 MHz
Ultra high frequency (UHF)	300 MHz–3 GHz
L band	1–2 GHz
S band	2–4 GHz
C band	4–8 GHz
X band	8–12 GHz
Ku band	12–18 GHz
K band	18–26 GHz
Ka band	26–40 GHz
U band	40–60 GHz
V band	50–75 GHz
E band	60–90 GHz
W band	75–110 GHz
F band	90–140 GHz

Figure 1-4 Frequency spectrum of RF waves and Microwaves taken from [10].

RF waves and Microwaves have unique properties that are utilized in military, science, and commercial applications [6]. In antenna and radar design high frequencies allow for more antenna gain and better target detection. For communication systems, RF waves and microwaves are not easily deflected by the ionosphere, making technology like GPS, weather analysis, and communication around the globe possible. Additionally, higher frequencies provide higher bandwidth capabilities which improve networking and communication systems. Lastly, the use of RF waves and microwaves have improved medical diagnostics as molecular resonances occur at high frequencies improving biomedical sensors and imaging [6].

Packaging devices that operate at these high frequencies can prove to be challenging as high frequency modules face hurdles that DC or lower frequency modules do not. These issues are addressed in more detail in chapter 4 of this thesis. The key problems packaging manufacturers face are parasitics, discontinuities, and electromagnetic interference (EMI) [7]. In this thesis focus will be spent on utilizing microcoaxial cables as a rapid integration method, with a focus on shielding to reduce EMI, and low inductance to enable efficient power distribution.

1.3 *Micro-Coaxial Interconnects for SiP RF Modules*

Standard wire bonding, flip chip methods, and embedded die techniques are just a few of the methods that designers in the semiconductor industry are using to create RF SiP modules. Nuvotronics' Coaxial Waveguide, Hitachi Chemical Co.'s Multi-Wire Board, and BridgeWave and Kulicke & Soffa Industries' in-situ microcoax fabrication and attachment process are three technologies that employ the use of waveguides, insulated wires, and micro-coaxial cables as the primary mode of interconnects to enhance signal integrity for RF modules. These methods use clever attachment strategies, or automated wire bonding and routing technology to achieve high speed and reconfigurable integration. These three existing technologies have influenced an internal

research and development (IRAD) project at Draper named Miniature-Multi-Wire Systems (MMS) which has served as the basis for this Master's Thesis.

1.3.1 Nuvotronics Coaxial Waveguide and Reconfigurable RF Components

Figure 1-5 illustrates a fabricated coaxial waveguide microstructure with a rectangular cross section fabricated by Nuvotronics in 2003. This structure consists of an inner conductor surrounded by four walls that make up the outer conductor. Both conductors are separated and their structures are held in place by dielectric support members that are enclosed in some volume between the inner and outer conductor. The dielectric material of this coaxial waveguide is primarily air under vacuum enclosed in the space between the inner and outer conductor [8]. The waveguide is made to be used for signal transmission with a characteristic impedances between 30-70 Ω. The structure is made through various lithographic patterning and metal deposition steps, utilizing highly conductive metals such as Gold, Copper, Nickel and Aluminum [8].

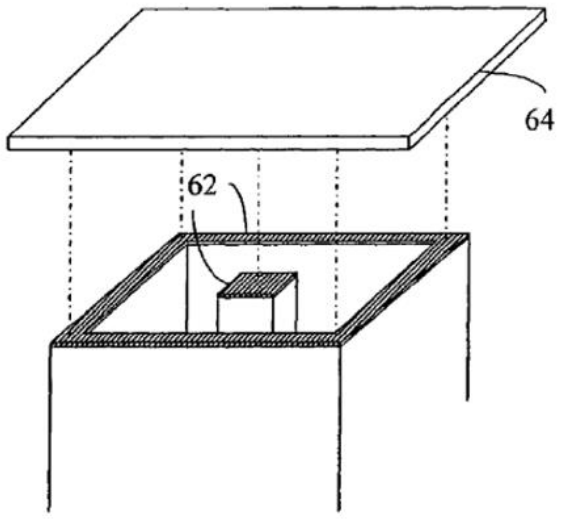


Figure 1-5 Images of a coaxial waveguide microstructure taken from [8]. Schematic of inner and outer conductors, labeled as 62, enclosed by a passive or active device, labeled as 64, that will utilize the coaxial wave guide.

Nuvotronics incorporates the use of this coaxial waveguide structure with other micro machined structures such as RF filters, antennas, switches, inductors, capacitors, and other passive and active components (Figure 1-6). Each component is uniquely fabricated to have micro-mechanical interconnects that allow for assembly between other components. These attachments also allow for rearrangement within the RF module if new components are to be added or if components are to be removed or replaced [9].

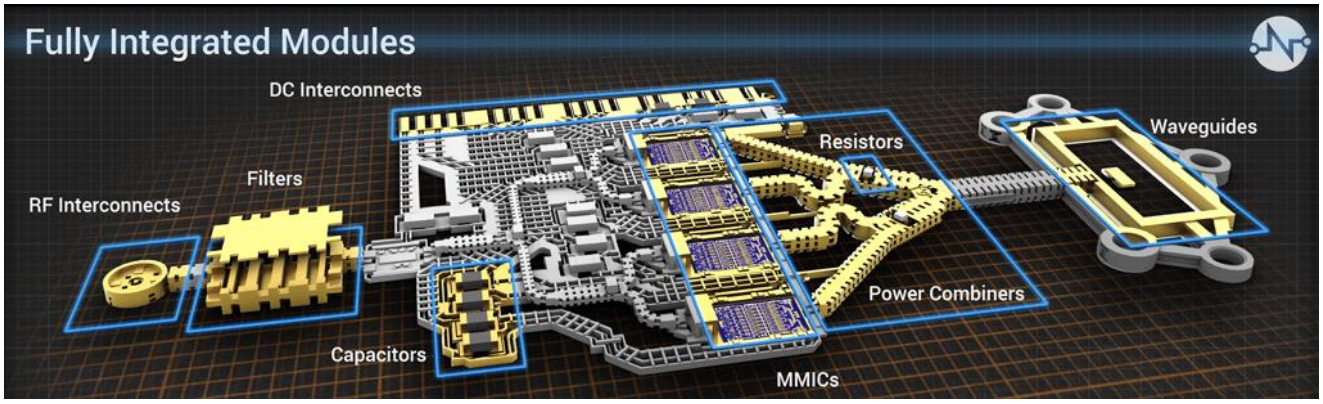


Figure 1-6 Schematic of a fully integrated RF module by Nuvotronics. Micro sized interconnects are used to attach components to each other. These interconnects are reconfigurable. Figure taken from [9].

1.3.2 Hitachi Chemical Co.'s Multi-Wire Board

Hitachi Chemical Co.'s Multi-Wire board introduced in 2015 is a SiP technology that utilizes rapid routing of pre-fabricated wires to package microchips. Current capabilities include automated high-density routing of Copper wires insulated with Polyimide resin 80 – 100 µm in diameter (Figure 1-7) and with wire lengths up to 650 µm. Hitachi is capable of packaging chips with substrates that are up to 6300 µm thick and up to substrate areas of $330 \cdot 10^9$ µm^2. These wires have been shown to have higher signal integrity relative to planar PCB technology of comparable dimensions illustrated in Figure 1-7. Propagation loss per length is $25 \cdot 10^{-6}$ dB/µm up to 5 GHz [10].

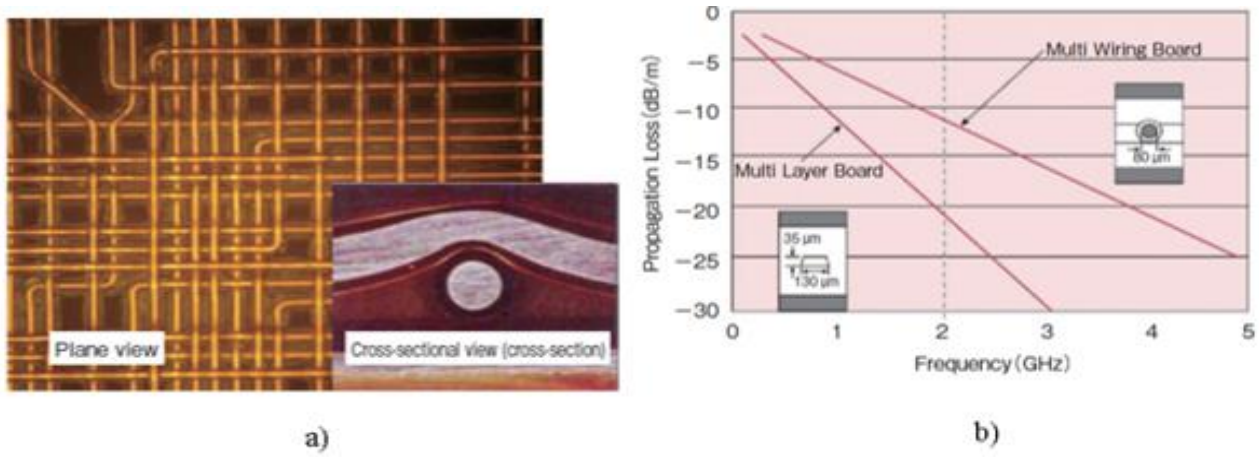


Figure 1-7 a. Routed connections using Multi-Wire Board technology and a cross section of insulated Cu wire. 6b. Propagation loss (dB/m) of 2D planar multilayers with a cross sectional area of 4550 um^2, and 3D coaxial geometry with a cross sectional area of 5027 um^2. Images taken from [10].

1.3.3 In-Situ Fabrication and Attachment of Micro-Coax

A third micro-coax integration strategy comes from Sean Cahill, Eric Sanjuan, and Lee Levine from BridgeWave Communications and Kulicke & Soffa Industries. The process, illustrated in Figure 1-8, was introduced in 2006 [11] and involves an in-situ signal coax fabrication and attachment strategy targeting characteristic impedances of 40 Ω and 50 Ω. The signal fabrication process involves: wire bonding Gold interconnects, using a conformal coating of Parylene C or Parylene N as a dielectric material, laser etching to expose ground paths, metalizing all wires by depositing a thin adhesion metal layer, and Gold plating a thick metal shield. Cahill, Sanjuan, and Lee have been successful at fabricating signal coax 92- 113 µm in diameter and up to wire lengths of 2000 µm. Transmission line performance reported in their work include transmission line losses of 0.00025 dB/µm and cross-talk isolation of 40-50 dB up to 50 GHz and with bond pitch sizes of 160-213 µm [11].

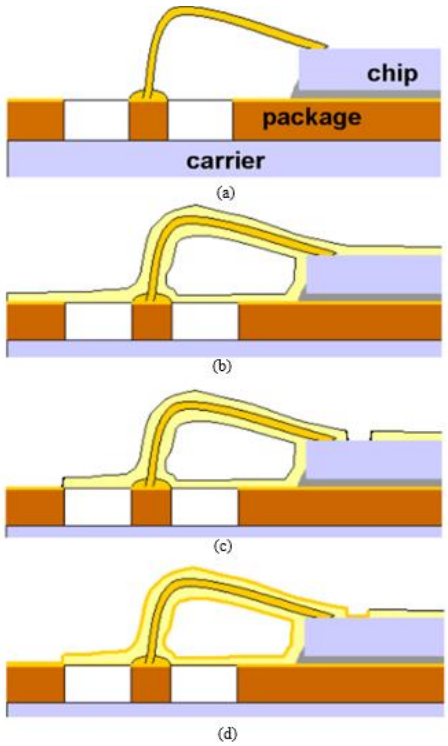


Figure 1-8 Outline of Signal Micro-Coax Fabrication Known as an in-situ micro-coax fabrication and attachment strategy [11]. (a) Wire Bonding from a chip to package. (b) Dielectric coat. (c) Laser etch to expose ground path. (d) Metallization of shield.

1.3.4 Miniature Multi-Wire Systems

An internal research and development (IR&D) project at Draper named Miniature Multiwire Systems (MMS) aims to use shielded microcoax for *all* component interconnects to eliminate the lengthy layout and fabrication processes associated with power and signal distribution. MMS final form of technology (Figure 1-9) would involve a process similar to wire bonding: a tool that is capable of spooling microcoaxial cables, which are fabricated beforehand in a reel to reel process, with in line shield stripping capabilities, and capable of bonding the core and shield at both ends

of the wire [12].

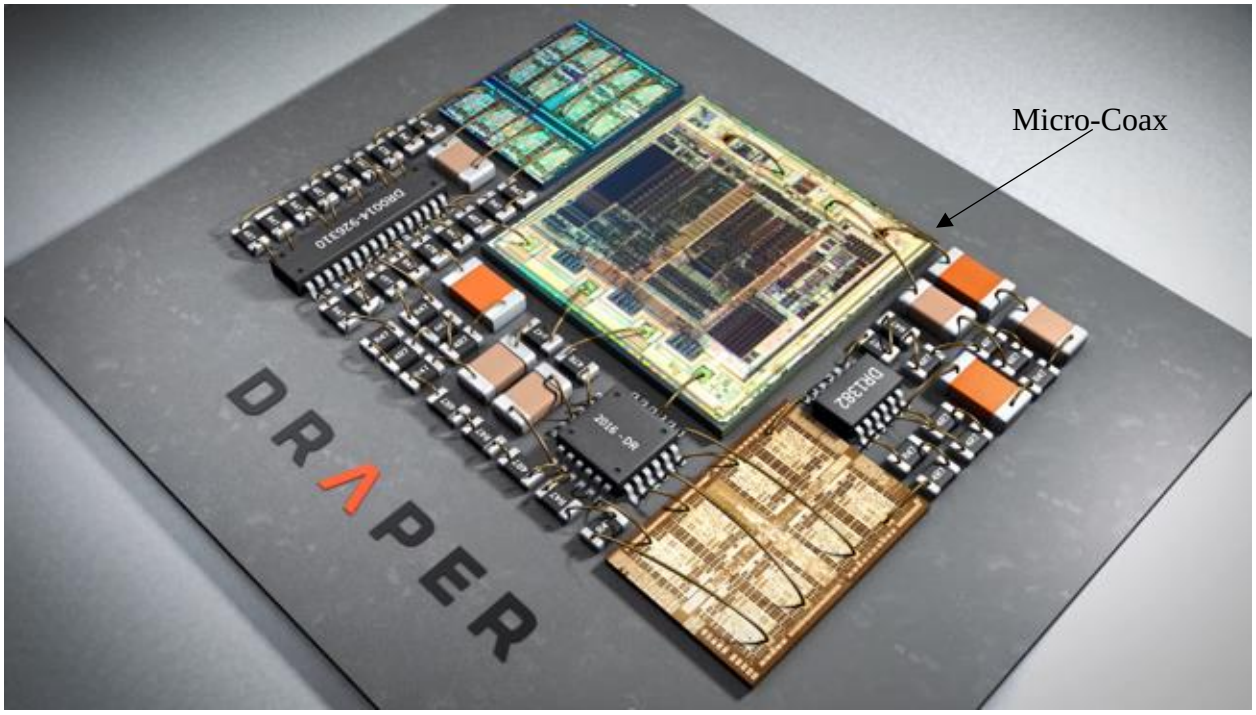


Figure 1-9 Illustration of MMS technology. Components are placed onto a substrate (grey) and interconnected together with micro-coax by an automated micro-coax bonder.

Current wires utilize dielectrics such as Parylene C, Polyeurethane, and Polyesterimide with conductors such as Copper, Gold, and Silver. For power distribution measured characteristic impedances are between 2.87-16.7 Ω. For signal distribution characteristic impedances are measured to be between 33 – 81 Ω. Cross-talk integrity is low at -60 dB up to 10 GHz.

A summary of coaxial transmission lines for SiP and their properties can be found in Table 1-1.

Table 1-1 Summary of Coaxial Transmission Lines for SiP and Their Properties

	Thesis Work	MMS	In-Situ MicroCoax	Hitachi's Multi-Wire	Nuvotronics' Waveguide
Wire Type	Power & Signal	Power & Signal	Signal	Signal	Signal
Dielectric	Parylene C ALD HfO_2	Polyesterimide Polyurethane Parylene C Parylene N	Parylene C Parylene N	Polyimide Resin	Air or Vacuum

Conductors	Gold	Copper Gold Sn/Ag Eutectic	Gold	Copper	Copper, Gold, Nickel, Aluminum
Measured Characteristic Impedance	Power: 0.07-3.5Ω Signal:40-60 Ω	Power:2.87-16.7Ω Signal: 33-81Ω	40-50Ω	45-55Ω	30-70Ω
Measured Cross-Talk	-40 to -62 dB up to 26.5 GHz	-60dB up to 10 GHz	-40to -50 dB up to 50 GHz	n/a	n/a
Loss	Power: 0.004dB/ µm up to 12 GHz Signal: 0.0001 dB/µm up to 12 GHz	n/a	0.00025 dB/ µm up to 50 GHz	$25 \cdot 10^{-6}$ dB/ µm up 5 GHz	n/a

1.4 *Contributions*

Chapter 3 of this thesis is a paper being submitted to *iMAPS Journal of Microelectronics and Electronic Packaging*. This paper outlines design criteria for microcoaxial cables intended for power distribution. Design is centered around requirements in a power distribution network in which lower impedances are necessary (impedances less than 20 Ω). Chapter 3 also outlines the fabrication process primarily used by MMS to create microcoax which differs from the fabrication process used in Chapter 4. The fabrication process highlighted in Chapter 3 is a first step towards a reel to reel microcoaxial fabrication process for an automated microcoaxial wire bonder. RF characterization methods primarily used for MMS are also highlighted in Chapter 3 with measured electrical properties of the first set of cables fabricated by Draper.

Chapter 4 of this thesis is a paper being submitted to *IEEE Components Packaging and Manufacturing Technology*. This paper is focused on utilizing a different fabrication process than the one discussed in chapter 3. This analysis contains the majority of contributions for this thesis

work. The main goals for this analysis was to expedite integration and characterization of micro-coaxial cables for Miniature Multi-Wire Systems using an the in-situ microcoaxial fabrication and attachment process by Sean Cahill, Lee Levine, and Eric Sanjuan, that was described previously. This process has the advantage of not needing a new tool or new processing techniques to create micro-coax; instead it uses existing technology to do so. To extend some of the work that has been done previously, this thesis is focused on fabricating both power and signal coax with different thin dielectrics to achieve even lower impedances as well as thick dielectrics for proper signal distribution. This thesis work also outlines the characterization of both the electrical properties of each wire and cross-talk between wires.

Prior to both of those papers is Chapter 2 which is focused on providing some background theory that is used in all experimental and analytical work. A basic understanding of transmission lines, microcoaxial geometry and its effect on electrical performance, network theory, and data display techniques were necessary to properly characterize microcoax at high frequencies.

2 Background Theory

2.1 *Transmission Line Basics*

A transmission line is a distributed component where along its length, voltage and current may vary in magnitude in phase. Most transmission lines (i.e coaxial cables) can be represented by the distributed circuit seen in Figure 2-1. Each line has a length Δz, current I(z,t), voltage v(z,t) between two conductors, resistance (R) per length (Ω/m), conductance (G) per length (S/m), inductance (L) per length (H/m), and capacitance (C) per length (F/m). A Transmission line can be represented by multiple segments each with length Δz.

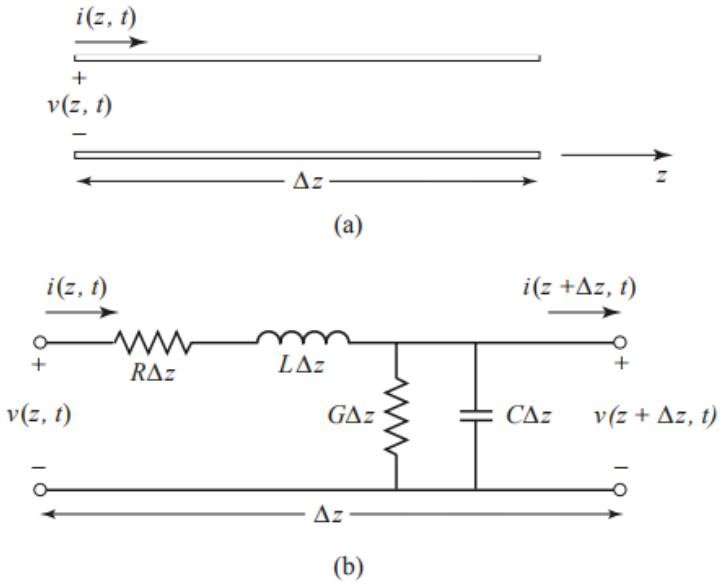


Figure 2-1 Basic Transmission Line Representation. a) Illustration of a transmission line with length Δz. b) Distributed circuit model of a transmission line. Image taken from [6].

Using the circuit described in Figure 2-1 it is possible to derive the following wave equations (1) for a voltage V(z) and I(z), using Kirchhoff's voltage and current laws, the telegrapher equations, and solutions to the wave equation [6]:

$$V(z) = V_0^{+} e^{-\gamma z} + V_0^{-} e^{\gamma z}$$
$$I(z) = I_0^{+} e^{-\gamma z} + I_0^{-} e^{\gamma z} \quad (1)$$

Where V_0^+, V_0^-, I_0^+, and I_0^- represent the amplitudes of the transmitted and reflected voltage and current waves, $e^{-\gamma z}$ represents transmitted wave propagation, $e^{\gamma z}$ represents reflected wave propagation, and γ represents the complex propagation constant. The complex propagation constant is described in (2) as [6]:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2}$$

where α represents the attenuation constant of the line and β represents the phase constant of the line. Furthermore, a transmission line may be further characterized by its characteristic impedance, Z_0, which is defined as the ratio between the amplitudes of the voltage and current waves. Z_0 is expressed in (3) as [6]:

$$Z_0 = \frac{V_0^+}{I_0^+} = \frac{-V_0^-}{I_0^-} = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{3}$$

The wavelength, λ, of a transmission line is defined in (4) as [6]:

$$\lambda = \frac{2\pi}{\beta} \tag{4}$$

The phase velocity, v_p, of the waves that propagate within the transmission line is defined in (5) as [6]:

$$v_p = \frac{\omega}{\beta} = \lambda f \tag{5}$$

For a lossless transmission line it is assumed that conductivity and dielectric losses resulting from R and G are equal to zero, and therefore α is equal to zero. This can be true for metals with high conductivity, such as gold and copper, and for polymer dielectrics with low conductivities. This results in the following changes (6) to the definitions of γ, Z_0, λ, and v_p [6]:

$$\gamma = \alpha + j\beta = j\omega\sqrt{L\,C}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

$$\lambda = \frac{2\pi}{\omega\sqrt{L\,C}} \tag{6}$$

$$v_p = \frac{1}{\sqrt{L\,C}}$$

It is important to note that characterizing a transmission line this way assumes that the waves in the line propagate as transverse electromagnetic (TEM) waves [6]. TEM is a mode of propagation where the electric and magnetic fields are normal to the direction of propagation. In the case of Figure 2-1 waves propagate in the z-direction.

2.2 *Transmission Line Parameters for Coaxial Cables*

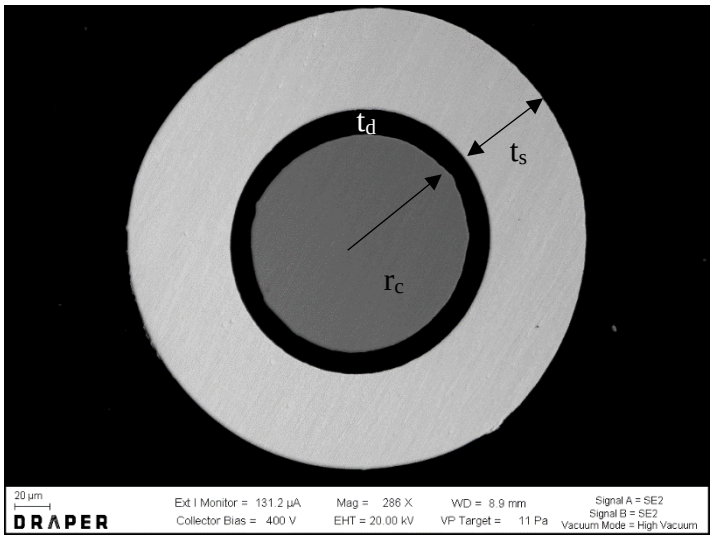


Figure 2-2 Scanning Electron Microscope image of cross section of fabricated micro-coax (fabricated for this work) with a 63.5µm radius core, 12 µm Polyesterimide dielectric, and a 55 µm gold plated shield. In this image r_c represents the radius of the core, t_d represents the dielectric thickness, and t_s represents the shield thickness.

Typical coaxial cable geometry (Figure 2-2) consists of an inner conductor (core), dielectric material (insulator), and an outer conductor (shield). Geometric, magnetic, and dielectric

properties of the coaxial cable will have direct influence on R, G, L, and C of the cable. In typical coaxial transmission lines it is assumed that the core and shield metals are highly conductive and weakly paramagnetic, the core and shield carry currents equal in magnitude but opposite in direction, and the magnetic field produced by the core is directed radially outward while the magnetic field produced by the shield is directed radially inward [12]. This typical behavior maintains the magnetic fields, produced by the wire, within the wire itself.

The resistance of a coaxial transmission line, R, represents conductivity losses of the cable and is defined in (7) as [6]:

$$R = \frac{R_s}{2\pi}\left(\frac{1}{r_c} + \frac{1}{r_c + t_d}\right) \tag{7}$$

where r_c is the radius of the core, t_d is the dielectric thickness, and R_s is the surface resistance of both the core and shield which is defined in (8) as [6]:

$$R_s = \frac{1}{\sigma \delta_s} \tag{8}$$

σ is the conductivity of the core and shield and δ_s is the skin depth of both those conductors. The skin depth of a conductor is defined in (9) as [6]:

$$\delta_s = \frac{1}{\alpha} = \sqrt{\frac{2}{\omega \mu_0 \mu_r \sigma}} \tag{9}$$

where μ_0 is the permeability of free space equal to $4\pi \cdot 10^{-7}$ H/m and μ_r is the magnetic permeability of the dielectric. It is important to note that skin depth is a function of frequency, ω. Typically, at higher frequencies one can expect the resistance of a conductor to increase as the effective cross sectional area of the wire that carries current is essentially reduced due to the skin effect [6]. The

conductance, G, of a coaxial transmission line represents the dielectric losses of the cable and is defined in (10) as [6]:

$$G = \frac{2\pi\omega\varepsilon_0 \,\mathrm{Im}\{\varepsilon_r\}}{\ln\left(\frac{r_c + t_d}{r_c}\right)} \tag{10}$$

where ε_0 is the permittivity of free space and equal to $8.85 \cdot 10^{-12}$ F/m and ε_r is the dielectric constant. The self-inductance between both the core and shield, L, of a coaxial transmission line is defined in (11) as [6]:

$$L = \frac{\mu_0 \mu_r}{2\pi} \ln\left(\frac{r_c + t_d}{r_c}\right) \tag{11}$$

The capacitance, C, of a coaxial transmission line formed due to the spacing between the core and shield is defined in (12) as [6]:

$$C = \frac{2\pi\varepsilon_0 \,\mathrm{Re}\{\varepsilon_r\}}{\ln\left(\frac{r_c + t_d}{r_c}\right)} \tag{12}$$

Throughout the analysis in this thesis focus will be spent characterizing L (equation 11), C (equation 12), and Z_0 (equation 3) of different coaxial cables fabricated for the Miniature Multi-wire Systems (MMS) packaging platform; assuming that conductivity and dielectric losses are at a minimum, and therefore we can neglect R (equation 7) and G (equation 10).

2.3 *Two-Port Network Theory and Scattering (s) Parameters*

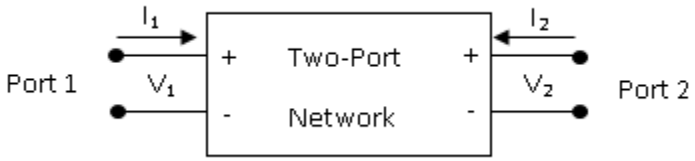


Figure 2-3 Schematic of a two-port network.

Active or passive RF components may be analyzed using any number of ports in a network analysis. For analyzing and measuring coaxial transmission lines a two-port network analysis (Figure 2-3) is commonly used where the transmission line and its substrate is defined as a network. The advantage of measuring RF components this way is that the network can be fully characterized by measuring a set of parameters at each port (i.e each end of a wire) without knowing all the details within the network itself. As illustrated in Figure 2-3, each port may be excited with voltages, V_1 and V_2, which will produce currents, I_1 and I_2, within the network [13]. Admittance (y) and impedance (z) parameters are typical parameters used to describe a network as they directly relate currents, I_1 and I_2, to voltages, V_1 and V_2, via Ohm's law. However, for RF or microwave applications, where frequencies are high and voltages and currents are best described as waves that travel within the network, scattering (s) parameters are more suitable for analysis [6]. Scattering parameters describe the network by relating the incident, a_i, voltage waves at port i to the reflected, b_i, voltage waves at port i. The incident and reflected waves at each port, denoted as i (where for a two-port network i = 1,2), are defined in (13) as [13]:

$$a_i = \frac{Voltage\ wave\ incident\ at\ port\ i}{\sqrt{Z_0}} = \frac{V_i + I_i Z_0}{2\sqrt{Z_0}}$$
$$b_i = \frac{Voltage\ wave\ reflected\ at\ port\ i}{\sqrt{Z_0}} = \frac{V_i - I_i Z_0}{2\sqrt{Z_0}} \qquad (13)$$

where V_i denotes the complex voltage at port i, I_i denotes the complex current at port i, and Z_0 denotes an arbitrary reference characteristic impedance. The full two-port network is then described in (14) using s-parameters as [13]:

$$b_1 = s_{11}a_1 + s_{12}a_2$$

$$b_2 = s_{21}a_1 + s_{22}a_2$$

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (14)$$

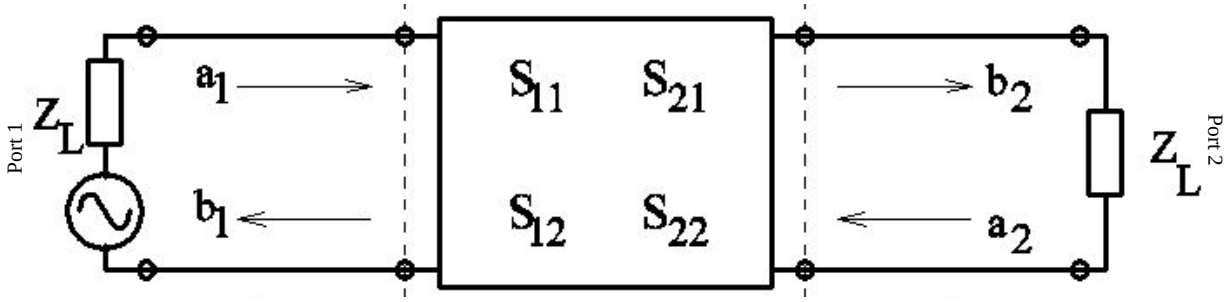


Figure 2-4 Two-Port Network with incident and reflected waves at each port. Also illustrated is the voltage source, V_s, from the Vector Network Analyzer (VNA), source impedance and load Impedance, Z_L, supplied by the VNA. Image taken from [13].

A Vector Network Analyzer (VNA) is capable of directly measuring s-parameters by inducing voltage waves a_i and b_i via voltage source V_s (Figure 2-4). To properly isolate each s-parameter a termination source impedance at port 1, Z_s, and a termination load impedance, Z_L, is introduced by the VNA (Figure 2-4). For example, to isolate S_{11}, voltage wave a_2 is terminated by a setting $Z_L = Z_0$ which sets $a_2 = 0$. S_{11} is then defined as a ratio of the reflected wave at port 1 (b_1) and the incident wave at port 1 (a_1) (15) [13]:

$$b_1 = s_{11}a_1 + s_{12}\cancel{a_2} = s_{11}a_1$$

$$s_{11} = \frac{b_1}{a_1} \tag{15}$$

Similar terminations are done to gather a full matrix of s-parameters. The definition of S_{11} can be broken down further by inputting the definitions of b_1 and a_1 (16) [13]:

$$s_{11} = \frac{b_1}{a_1} = \frac{\frac{V_1 - I_1 Z_0}{2\sqrt{Z_0}}}{\frac{V_1 + I_1 Z_0}{2\sqrt{Z_0}}} = \frac{V_1 - I_1 Z_0}{V_1 + I_1 Z_0} \tag{16}$$

Dividing by the current at port 1, I_1, results in (17) [13]:

$$s_{11} = \frac{\frac{V_1}{I_1} - Z_0}{\frac{V_1}{I_1} + Z_0} = \frac{Z_1 - Z_0}{Z_1 + Z_0} \tag{17}$$

Where Z_1 denotes the input impedance at port 1 [13]. Similar relationships between s-parameters and impedance can be made which will be useful for understanding the Smith chart (described in later chapters). Another name for S_{11} and S_{22} are the reflection coefficients of the network. Whereas S_{12} and S_{21} are named the transmission coefficients of the network [13]. It is important to recall that since voltage and current waves carry magnitude and phase, s-parameters are complex values.

2.4 *Four-Port Network Theory*

A four-port network analysis is useful for studying the coupling effects (cross-talk) between adjacent coaxial transmission lines. As frequency increases in a coaxial transmission line the magnetic fields produced by the core and shield conductors radiate and extend beyond the physical

dimensions of the coaxial cable partly due to the skin effect [12]. This magnetic radiation may be picked up or absorbed by nearby RF components (i.e another coaxial transmission line) [12]. In a four-port network the definition of incident (a_i) and reflected waves (b_i) remains the same (ports 1-4 will have their own incident and reflected waves), but the s-parameter matrix becomes larger since there is the added coupling relationship between wires [13]:

$$\begin{aligned} b_1 &= s_{11}a_1 + s_{12}a_2 + s_{13}a_3 + s_{14}a_4 \\ b_2 &= s_{21}a_1 + s_{22}a_2 + s_{23}a_3 + s_{24}a_4 \\ b_3 &= s_{31}a_1 + s_{32}a_2 + s_{33}a_3 + s_{34}a_4 \\ b_4 &= s_{41}a_1 + s_{42}a_2 + s_{43}a_3 + s_{44}a_4 \end{aligned}$$

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} & s_{13} & s_{14} \\ s_{21} & s_{22} & s_{23} & s_{24} \\ s_{31} & s_{32} & s_{33} & s_{34} \\ s_{41} & s_{42} & s_{43} & s_{44} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \tag{18}$$

The s-parameters outlined in blue and green are characteristic to each individual wire (no-coupling). These results would be the same s-parameters gathered from a two-port measurement of each individual wire. The s-parameters outlined in orange are the reflection and transmission coefficients of coupled wires that can be used to determine at which frequency the wires are well isolated from each other. Coupled transmission s-parameters (i.e S_{14} and S_{23}) are typically plotted on a magnitude vs. frequency plot. At low frequencies it is expected that the magnitude of coupled s-parameters is low (>-50 dB). At a certain frequency magnitude it is expected to increase as the radiated fields from one wire begin to induce a current in the adjacent wire.

2.5 *De-embedding*

To test a coaxial cable's set of s-parameters using a Vector Network Analyzer (VNA) it is necessary to attach or fabricate the cables onto a test fixture. As a result, the full s-parameter matrix gathered from the VNA are that of the cable, often referred to as the device under test (DUT), and the test fixture. In order to properly characterize the transmission line parameters of the DUT the test fixture characteristics need to be removed from the full set of s-parameters. One of the methods used to remove the effects of the test fixture is known as de-embedding. De-embedding requires proper modeling or measurement of the test fixture to mathematically remove its effects [14].

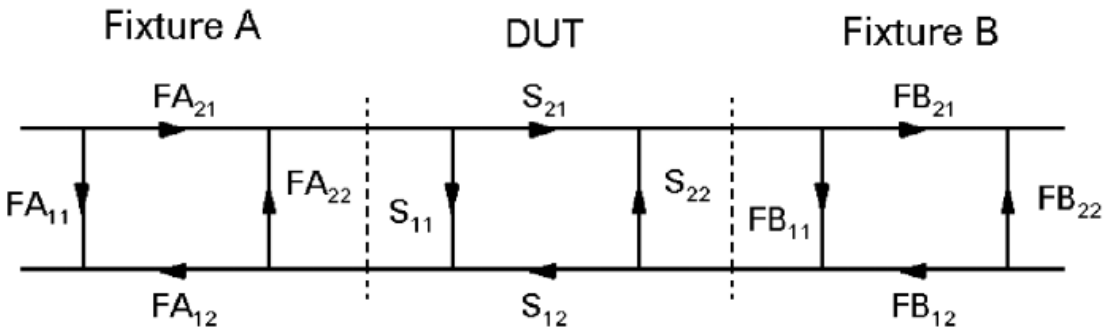


Figure 2-5 Signal flow graph of a two-port network analysis of a DUT and its test fixture effects at both ports [14].

To de-embed, it is assumed that the DUT, the test fixture component connecting the DUT to port 1 of the VNA (Fixture A), and the test fixture component connecting the DUT to port 2 (Fixture B) each contribute their own set of s-parameters. In Figure 2-5, fixture A's s-parameters are labeled as FA and fixture's B's s-parameters are labeled as FB. The full measurement of s-parameters gathered ($S_{Measured}$) from the VNA are then represented by the following cascaded matrices (19) [14]:

$$[S_{Measured}] = [S_{FA}][S_{DUT}][S_{FB}] \quad (19)$$

Assuming that S_{FA} and S_{FB} are invertible, S_{DUT} may be extracted by a left and right multiplication of S_{FA}^{-1} and S_{FB}^{-1} which represent the matrix inverse of S_{FA} and S_{FB} (20) [14]:

$$[S_{FA}]^{-1}[S_{FA}][S_{DUT}][S_{FB}][S_{FB}]^{-1} = [S_{FA}]^{-1}[S_{Measured}][S_{FB}]^{-1} = [S_{DUT}] \quad (20)$$

S_{FA} and S_{FB} may be gathered directly, by separately measuring a test fixture without a DUT via a VNA known as measurement based De-embedding. Another method, which is a primary method used in this thesis, involves properly modeling the test fixture in software such as Advanced Design System (ADS) [14]; this method is known as model based de-embedding. Both methods will produce a set of S_{FA} and S_{FB} that can be inverted for de-embedding and extracting S_{DUT}.

2.6 *Plotting and Interpretation of S-Parameters*

After gathering s-parameters from a Vector Network Analyzer (VNA), it is useful to plot s-parameters for full interpretation of results. A VNA sweeps voltage over a range of frequencies and each frequency carries its own set of s-parameters. The most common way this information is presented is using a Smith chart plot and magnitude vs. frequency plot.

2.6.1 Smith Chart

A Smith chart is a useful graphical tool used to plot reflection coefficients and relate them to impedance. Transmission coefficients may also be plotted on a Smith chart, but it is more common to plot reflection coefficients. The Smith chart overlays two coordinate systems: the first is a polar plot of complex s-parameters. The second is an impedance grid [15]. Recall the relationship described in (17) which relate the complex reflection coefficient to impedance [13]. This relationship is important since one of the end goals is to determine the impedance of the device under test (DUT). Additionally, the Smith chart is normalized to Z_0, the same Z_0 defined in (13). Finally, each point on the Smith chart corresponds to a different frequency and its respective reflection coefficient.

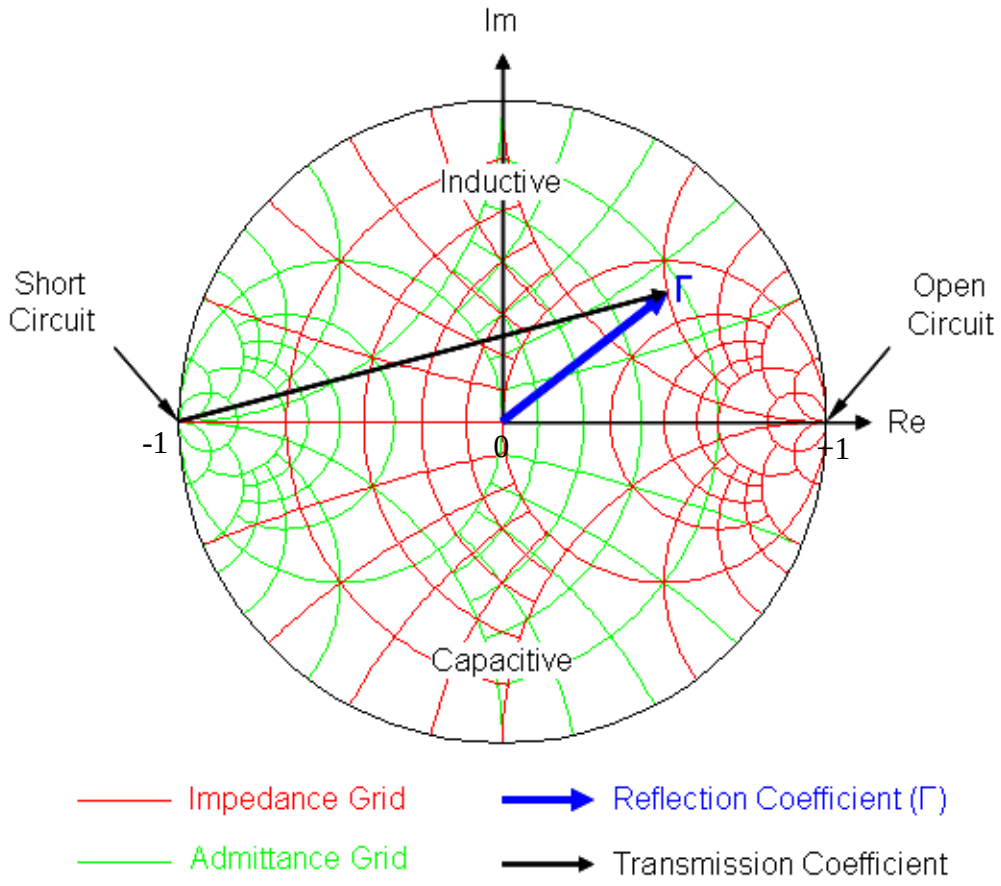


Figure 2-6 Overview of a Smith Chart taken from [15].

Figure 2-6 outlines some important details of the Smith chart. Resistance, which is a real impedance, is located on the horizontal axis of the Smith chart. Inductance, which is a complex impedance, represents the top half of the Smith chart, and capacitance, which is also a complex impedance, represents the bottom half of the Smith chart [15]. A short circuit on the Smith chart is located far left since in order for a short circuit to be possible there should be a zero potential at the short. To get a zero potential the incident and reflected voltage waves should cancel each other out. This results in the magnitude of the reflection coefficient being equal to 1 (full reflection) with a phase of 180°. This is equivalent to saying that the reflection coefficient is equal to -1 on the Smith chart [15].

An open circuit on the Smith chart is located far right since in order for there to be an open circuit the incident and reflected voltages waves should be equal in magnitude and phase. This would result in the magnitude of the reflection coefficient being equal to 1 with a phase of 0°. This is equivalent to saying that the reflection coefficient is equal to 1 on the Smith chart [15]. The center of the Smith chart represents no reflections which means the DUT is matched perfectly to Z_0. This is equivalent to saying that the reflection coefficient is equal to zero [15].

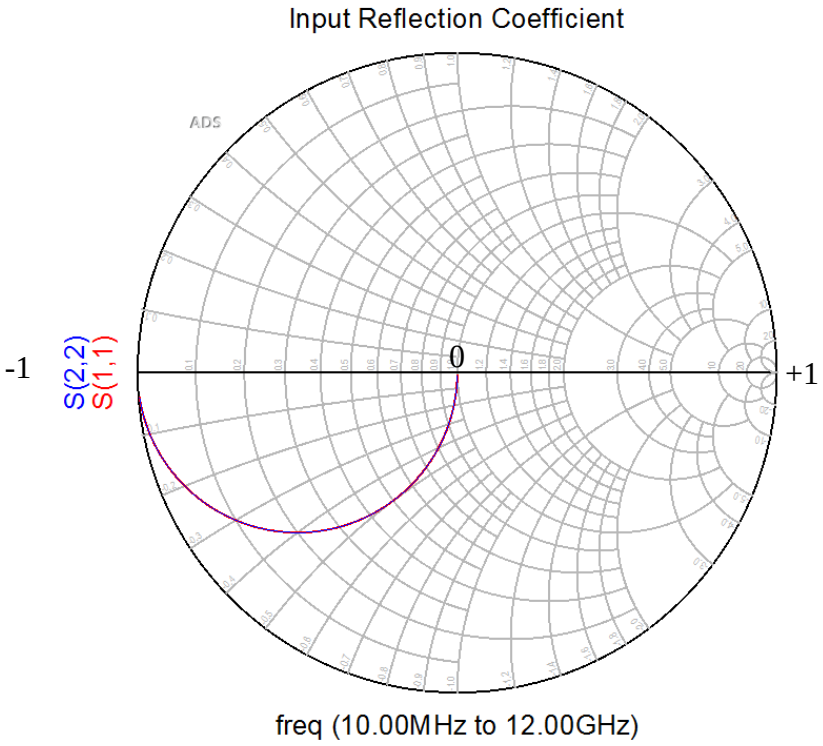


Figure 2-7 Ideal capacitor behavior with minimal inductance from 10 MHz to 12 GHz.

Figure 2-7 illustrates how an ideal capacitor with minimal to no inductance is represented on a Smith chart. Frequency is swept clockwise such that at 10 MHz the plot begins at the center. Recall, that the circuit for a two port network connected to a VNA consists of the network (in this case a capacitor) and a load and source impedance. Typically, the load and source impedance are 50 Ω resulting in the Smith chart being normalized to a 50 Ω impedance. At low frequencies the

capacitor is open meaning the only impedance existing at port 1 or port 2 is the source or load impedance. A 50 Ω impedance is generally well matched with incoming voltage waves which result in zero reflections in the network. This explains why the Smith chart begins at the center. As frequency is swept, the capacitor impedance drops and it begins to behave as a short, which is why the scattering parameters sweep over to the left side of the Smith chart.

2.6.2 Magnitude vs. Frequency Plot

Transmission coefficients are plotted on a magnitude vs. frequency plot (Figure 2-8). Since a coaxial cable is a passive RF component one should expect at low frequencies for the gain, or magnitude, of the transmission coefficient to be equivalent to 0 dB on a magnitude vs. frequency plot. 0 dB is a logarithmic representation of a transmission coefficient equal to 1. At low frequencies it is expected that a coaxial cable has minimal losses (no reflections) and thus is only transmitting voltage waves. At higher frequencies, as loss becomes more apparent one should expect the magnitude of the transmission coefficient to decrease. Since reflection and transmission coefficients are ratios, their magnitudes are typically less than 1. A magnitude less than 1 is represented on a magnitude vs. frequency plot as negative dB values.

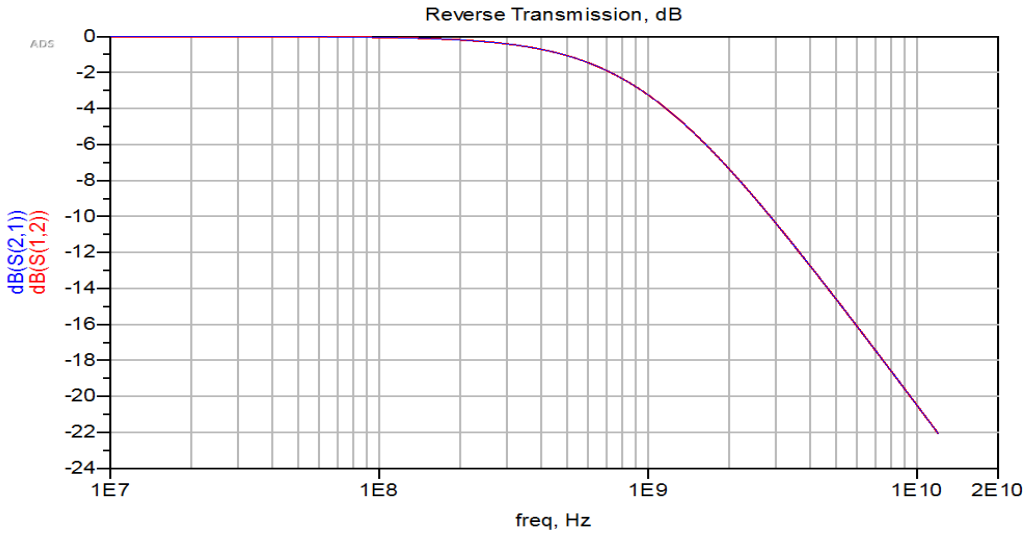


Figure 2-8 Behavior of transmission coefficients on a magnitude vs. frequency plot of an ideal capacitor.

3 Characterization of Low Impedance Micro-Coaxial Cables for Power Distribution

3.1 *Abstract*

Low impedance micro-coaxial cables have been developed to supply power to microchips. These uniquely low inductance cables are enabled by a very thin dielectric compared to a conventional 50 Ω cable. These cables will be used in a novel packaging platform in which traditional interconnects are replaced by micro-scale coaxial cables. This method saves time, cost, and labor for small production volume and custom electronics, compared to conventional multilayered packaging techniques. These micro-coaxial cables are designed to have minimal impedance to meet the stringent power supply requirements of today's electronics. As a concrete example, we consider a Kintex 7 FPGA. To power this chip with interconnect lengths of 25 mm, voltage ripple less than 30 mV, and max current draw of 3.4W, a resistance of 3.20-6.40 mΩ/mm and an inductance of 12-15 pH/mm is needed. The tight voltage ripple constraint is what makes this device challenging to design power distribution for. One cable fabricated by Draper, to achieve these power requirements, is the focus of this paper. The Draper cable consists of a 127 μm Copper core, 12 μm polyester-imide dielectric layer, and 55 μm gold shield. The measured resistance per unit length at DC, inductance per unit length, capacitance per unit length, and characteristic impedance of the Draper cable are 2.0 mΩ/mm, 40 pH/mm, 118 pF/mm, and 6.56 Ω respectively.

3.2 *Introduction*

A common architecture in packaging electronics is a 2D assembly of single chip modules on a printed circuit board (PCB) or other appropriate substrates. This packaging scheme has allowed designers to integrate multiple functions from various integrated circuits (ICs) in a single system.

However, this method has reached some of its limitations in fabrication. As the need for miniaturization and more functionality on a chip increases, 2D planar fabrication is challenging [16]. There are also increasing demands for complex power distribution, cost reduction, customization, and quick turnaround time for packaging technology [17]. Devices such as smartphones, pacemakers, automotive systems, and hybrid devices for the "Internet of Things (IoT)" are demanding more heterogeneous technology integration. As a result, designers are focusing their attention on making complex systems at the package level, by assembling multiple dissimilar chips into a package. This packaging platform is known as the System in Package (SiP) [17], which is different from System on a Chip (SoC). SoC is even more highly integrated, but less flexible and requires a longer design cycle.

SiP may incorporate a diverse set of devices such as microelectromechanical systems (MEMS), optical, RF, and biochemical components, into one package [16]. Some common forms of SiP integration are die stacking, wire bonding, and flip chip bonding. These methods have transformed packaging from the 2D planar level to 3D. Wire bonding has the advantage of being a rapid method of integration, however, one limitation is shielding between wires, needed to reduce cross-talk while maintaining required the impedance. The cross-talk issue is more prominent in RF modules that make up 65% of SiP packages [17], and thus the need for good signal and power integrity for these modules is increasingly important especially as IO counts, pitch, and miniaturization.

Previously described wire bonding and flip chip methods have been extended by some in the semiconductor industry to include integrated shields. Two technologies that employ the use of coaxial structures as the primary mode of interconnects to enhance signal integrity for RF modules

are Nuvotronics' Coaxial Waveguide [18]and BridgeWave and Kulicke & Soffa Industries' wire-bond based micro-coaxial interconnects [20]. Hitachi Chemical Co.'s Multi-wire Board [9] demonstrates a rapid wire-only interconnect system using insulated wires. All three integration platforms have been designed with impedances between 30-70 Ω. However, to fully eliminate the need for lithographically patterned circuit layers, power distribution, which requires lower impedance coax, also needs to be addressed.

We have examined the existing layout and fabrication processes for SiP device and it appears that there are two major lead-time and cost drivers. First, finalizing a layout can take months due the need for multiple iterations because designs fail in simulation. Second, the multi-step microfabrication of the substrate can take weeks or months, due to multi-layer lithography and/or lamination steps, which can take days at a time and are not flexible to rapid changes in interconnect design often needed for custom and editable circuits. To minimize the time it takes to progress from an electrical schematic to a built, testable device, we propose using shielded microcoax for all interconnects. This eliminates the need for lengthy simulation and layout iterations. Fabrication time is also saved because the interconnects are fabricated with a single tool that resembles a modified wire bonder, capable of stripping and attaching micro-coaxial cables. The implementation of coax for signal distribution with impedance ranges between 30 Ω-70 Ω is well understood and has previously been studied for RF applications [6]. In this paper, we describe design criteria, fabrication methods, and RF characterization of micro-coax for power distribution with substaintially lower impedances than previously reported in the literature, <10 Ω.

3.3 *Low Impedance Microcoax Design*

Replacing traditional planar interconnects with micro-coaxial cables requires unique design considerations. Design is centered around a power distribution network (PDN) where a target impedance value can be used to design proper coaxial geometry for a given device. Target impedance values can then be related back to coaxial geometry, dielectric properties, and metal conductivity of the core and shield, which each influence the electrical properties of coax. Of particular interest is the resistance and inductance of micro-coaxial cables at near DC and at high frequencies due to its impact on a PDN.

3.3.1 Case Studies of a Power Distribution Network

A power distribution network (PDN) may consist of multiple components, all of which are responsible for distributing power and handling return currents of a system. Components may include sources such as batteries or local decoupling capacitors, package leads, interconnects such as wire bonds, traces, vias, solder joints, or metalized pads on a chip. A key difference of a PDN compared to signal distribution is that the PDN is global and fully coupled across the system. Therefore, any component may have an effect on the whole delivery network [21]. For this analysis the major contributing elements in a PDN will be the resistance and inductance of micro-coaxial cables.

In order to focus the design space for developing micro-coaxial cables for a PDN, we chose the Kintex 7 FPGA as a case study for power handling. This system has demanding power requirements: needing 3.4 W at 1.0 V and a voltage ripple tolerance of less than 30 mV [22]. A PDN model of this system can be seen in Figure 3-1 where V_{Source} represents a constant 1.0 V supply, R_{Budget} represents the allowable resistance of a micro-coaxial cable in the PDN, L_{Budget} represents the allowable inductance of a micro-coaxial cable in the PDN, and I_{Sink} represents the current sink of the Kintex 7.

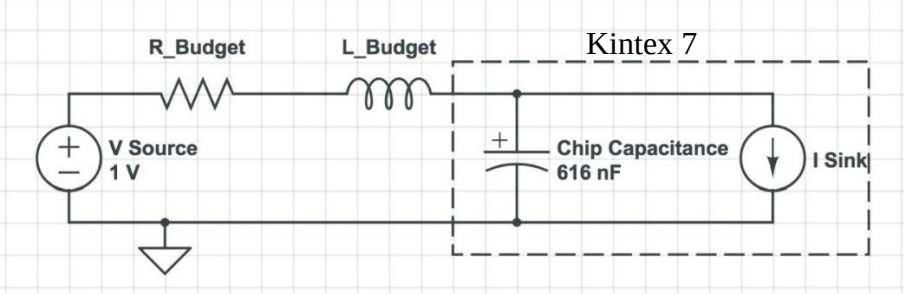


Figure 3-1 PDN Used to Estimate R_{budget} and L_{budget} for the Kintex 7 FPGA

The on chip capacitance is estimated by using the following relationship [21]:

$$C_{Chip} = \frac{\varepsilon_0 \varepsilon_{r\_die} A_{tdie} P_{gate}}{r_{oxide}} \tag{21}$$

Where C_{Chip} is the on chip capacitance, ε_{r_die} is the dielectric constant of the chip oxide, which for this FPGA is 3.9, A_{tdie} is the die area taken up by the core transistors estimated to be 1 cm^2, P_{gate} is the percentage of gate area estimated in [21] as 10 percent. This 10 percent estimate is taken from a general rule of thumb that not the entire die area makes up the transistor gate area. It is assumed that the on die capacitance is due only to its p and n junctions. r_{oxide} is the ratio of the gate oxide thickness to channel length estimated in [21] as 2 percent. This 2 percent estimate is taken from a general rule of thumb that with current transistor technology the gate oxide thickness is about 2 nm per 100 nm of channel length. This results in a C_{chip} of 600 nF.

The total impedance contributions of this PDN due to R_{Budget}, L_{Budget}, and C_{Chip} is known as Z_{pdn}. The goal of PDN design is to minimize Z_{pdn} through specifying geometric and material properties to ensure enough battery voltage appears at the chip. Additionally, small Z_{pdn} will minimize voltage ripple, V_{ripple}, occurring at the chip which could lead to heating of components and distortion [20]. In the chip's idle state and during operation I_{Sink} may vary over time resulting in a varying voltage at the chip; this variation is known as voltage ripple. Z_{pdn} may be bounded as:

$$Z_{pdn} < \frac{V_{ripple}}{\Delta I} \tag{22}$$

Where V_{ripple} should be ≤30 mV for the Kintex 7 FPGA, and ΔI is the dynamic current. For a 3.4 W requirement and a 1.0 V voltage source, the max current that the chip may draw at any moment is 3.4 A. The chips static current is ~0.4 A and the transient current is 3.0 A [22] . We assume that the max current differential, ΔI, occurs from the idle state to the start of operation. From this we estimate ΔI is 3.0 A. This is a conservative approach as it assumes that the rise time of the chip from idle state to operation is small. For this analysis we assume the rise time is 10 ns.

Using (22), a V_{ripple} of 30 mV results in a maximum Z_{pdn} of 10 mΩ. To package the Kintex 7 FPGA using micro-coax a total of 16 wires are needed. For 16 wires the maximum impedance for each wire, Z_{pdn_wire}, is 160 mΩ. Generally, due to the mutual inductance between wires, assuming that each wire contributes the same impedance is not a good assumption. However, because these wires are shielded, the assumption that mutual inductance is minimal is reasonable for this PDN analysis. This is one advantage of micro-coax.

To determine the appropriate sizing for the core, dielectric and shield of a power distribution coax for the Kintex 7, we must establish appropriate value ranges for R_{budget} and L_{budget} given that Z_{pdn_wire} must be below 160 mΩ. R_{budget} will be directly correlated with the shield and core metal thickness tolerances, and L_{budget} will establish the allowable dielectric thickness for a given length of wire. R_{budget} and L_{budget} can be studied parametrically.

As a first case study, R_{Budget} is set to meet Z_{pdn} exactly and L_{Budget} is adjusted until the frequency response of Z_{pdn} is critically damped. Simulating this response in Advanced Design System (ADS) using the circuit in Figure 3-1, values for R_{Budget} and L_{Budget} are estimated as 160 mΩ and 320 pH

respectively. In Figure 3-2 the frequency response of Z_{pdn} is shown up to 1 GHz. Z_{pdn} is indicated to be 10 mΩ at frequencies lower than 19 MHz before being damped at higher frequencies. Also shown in Figure 3-2 is the time domain response of voltage ripple at the chip. Voltage ripple for this case remains below 30 mV.

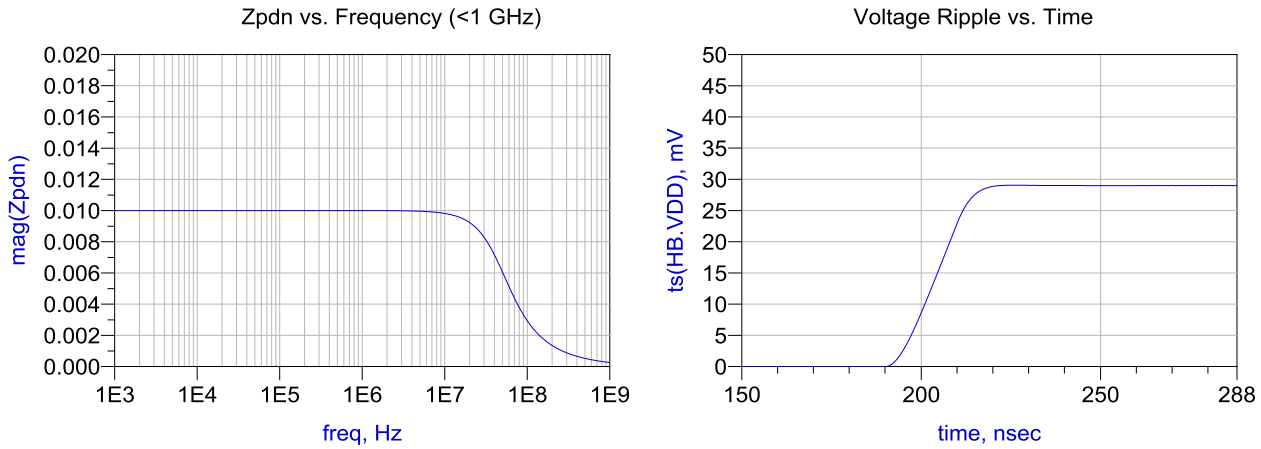


Figure 3-2 Frequency of Zpdn up to 1 GHz (Left) and Time Domain voltage ripple response (Right) simulated in ADS with R Budget equal to 160mΩ and LBudget equal to 320 pH.

As a second case study, R_{Budget} is reduced to 80 mΩ. A higher L_{Budget} of 380 pH is allowable and maintains Z_{pdn} below 10 mΩ. The frequency response of Z_{pdn} can be seen in Figure 3-3. This low R_{Budget} and higher L_{Budget} produces a resonant peak at 38.40 MHz. For this case, voltage ripple maintains below 17 mV.

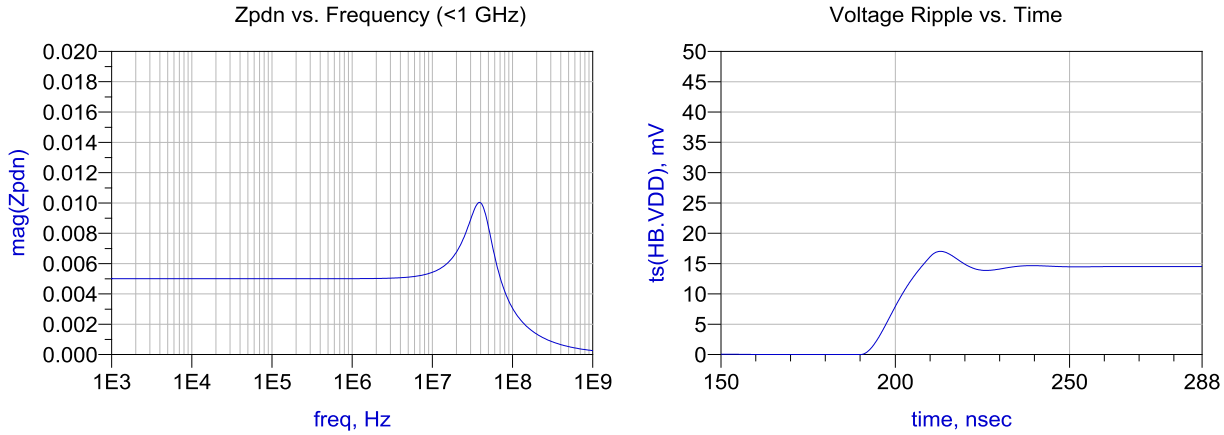


Figure 3-3 Frequency of Zpdn up to 1 GHz (Left) and Time Domain voltage ripple response (Right) simulated in ADS with R Budget equal to 80 mΩ and LBudget equal to 380 pH.

The average wire length needed to package the FPGA Kintex 7 with 16 Micro-Coaxial cables is 25 mm. This results in a R_{Budget}, using case 1 and case 2, of 3.20-6.40 mΩ/mm and an L_{Budget} of 12.8-15 pH/mm. These are the target specifications that drive design of the power distribution with micro-coax.

3.3.2 Resistance, Inductance, Characteristic Impedance and Capacitance of Coaxial Cables

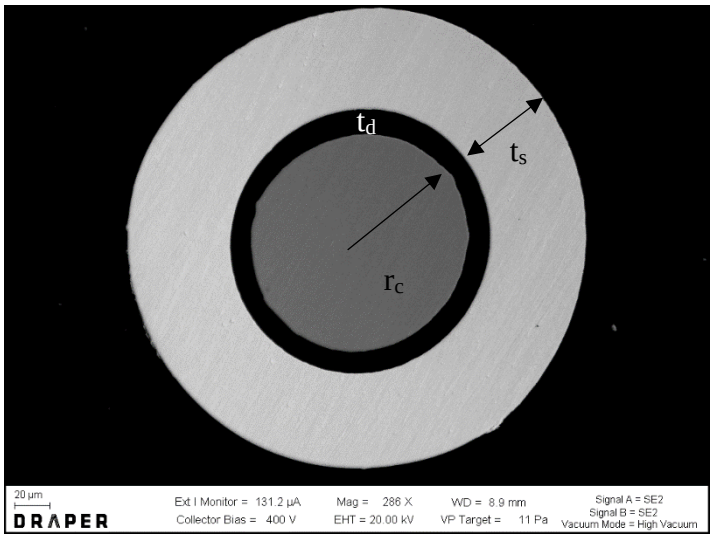


Figure 3-4 Scanning Electron Microscope cross section of fabricated micro-coax (this work) with a 63.5µm radius core, 12 µm Polyesterimide dielectric, and a 55 µm gold plated shield.

We now need to relate the electrical performance goals to coax geometry. A cross section of a fabricated micro-coaxial cable is seen in Figure 3-4. Coaxial cable geometry consists of an inner conductor (core), dielectric material, and an outer conductor (shield). Geometric properties, magnetic and dielectric properties, will have an influence on the resistance, inductance, capacitance, and characteristic impedance of the cable. A table of important properties can be seen in Table 3-1:

Table 3-1 Important Properties of Coax That Influence Electrical Properties

Parameter	Value	Units
r_c	Core Radius	μm
t_d	Dielectric thickness	μm
t_s	Shield thickness	μm
ρ_c	Core Resistivity	Ω·cm
ρ_s	Shield Resistivity	Ω·cm
μ_0	Magnetic Permittivity Free Space = $4\pi \cdot 10^{-7}$	H/m
μ_r	Magnetic Permittivity Constant = 1	
ε_0	Electric Permittivity Free Space = $8.85 \cdot 10^{-12}$	F/m
ε_r	Dielectric Constant	
l	Wire Length	mm

The DC resistance, R_{DC}, of a coaxial cable can be expressed as the sum of the core resistance, R_{core}, and the shield resistance, R_{shield}, both normalized to wire length [23]:

$$\frac{R}{l} = \frac{R_{core}}{l} + \frac{R_{shield}}{l} \tag{23}$$

At DC R_{core} and R_{shield} are only functions of wire geometry. The total resistance at DC, R_{DC}, per unit length in Ω/m becomes:

$$\frac{R_{DC}}{l} = \frac{R_{core}}{l} + \frac{R_{shield}}{l} = \frac{\rho_c}{\pi r_c^2} + \frac{\rho_s}{\pi \left[(r_c + t_d + t_s)^2 - (r_c + t_d)^2 \right]} \tag{24}$$

To determine the core radius, r_c, we assume that the core and shield metals of the microcoaxial wire will carry equal magnitudes of current. From this we may assume that the core and shield metals will split R_{Budget}. For a maximum R_{Budget} of 6.40 mΩ/mm we assume that the core metal should carry a DC resistance of 3.20 mΩ/mm. Using the definition of R_{core} in (24) and a resistivity of copper of $1.68 \cdot 10^{-8}$ Ω·m [24], the core radius of microcoax should be 41.0 μm or greater to

maintain below the maximum core resistance of 3.20 mΩ/mm. We choose copper as our core material for the wires discussed in this paper since it has a high electrical conductivity.

To determine the shield thickness we must first determine a dielectric thickness. This can be done using L_{Budget}. The inductance, L, per unit length is:

$$\frac{L}{l} = \frac{\mu_0}{2\pi} \ln\left(\frac{r_c + t_d}{r_c}\right) \tag{25}$$

Given an L_{Budget} of 13-15 pH/mm and an r_c of 41.0 µm it is possible to determine the necessary dielectric thickness for microcoax. A plot of inductance per unit length versus dielectric thickness can be seen in Figure 3-5 Inductance per unit length in H/m versus dielectric thickness determined by using (25). To target an inductance of 15 pH/mm or less, the maximum allowable dielectric thickness is 3.0 µm. It is important to note that this is true for a dielectric material that is not ferromagnetic, such that μ_r is 1.0.

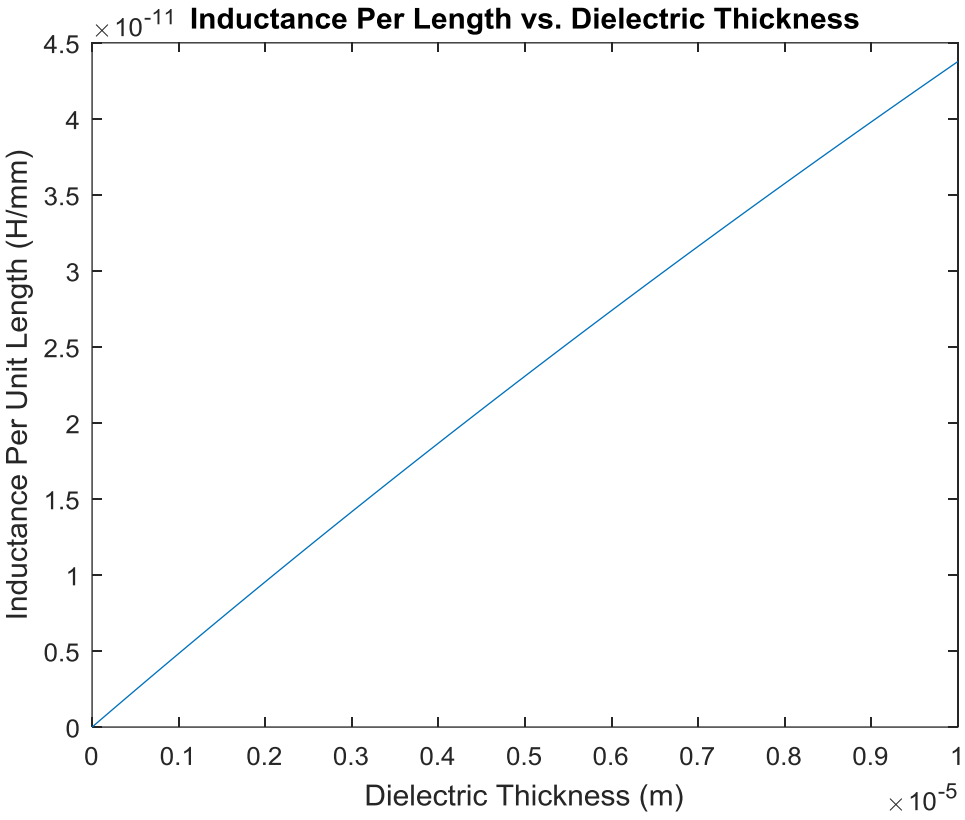


Figure 3-5 Inductance per unit length in H/m versus dielectric thickness determined by using (25).

Given a core radius of 41.0 µm and a target dielectric thickness of 3.0 µm we can determine the shield thickness using the definition of R_{shield} described in (24). Since the core and shield will be splitting R_{Budget} the shield thickness can be determined by targeting a shield resistance of 3.20 mΩ/mm. For the wires in this paper we are interested in using a gold shield as we will later describe is possible to electroplate on dielectrics with an adhesive metal layer. The resistivity of our electroplated gold is $3.30 \cdot 10^{-8}$ Ωm [25]. A plot of resistance per unit length versus shield thickness can be seen in Figure 3-6. To target a shield resistance of 3.20 mΩ/mm or less a shield thickness of 28.0 µm or greater is required.

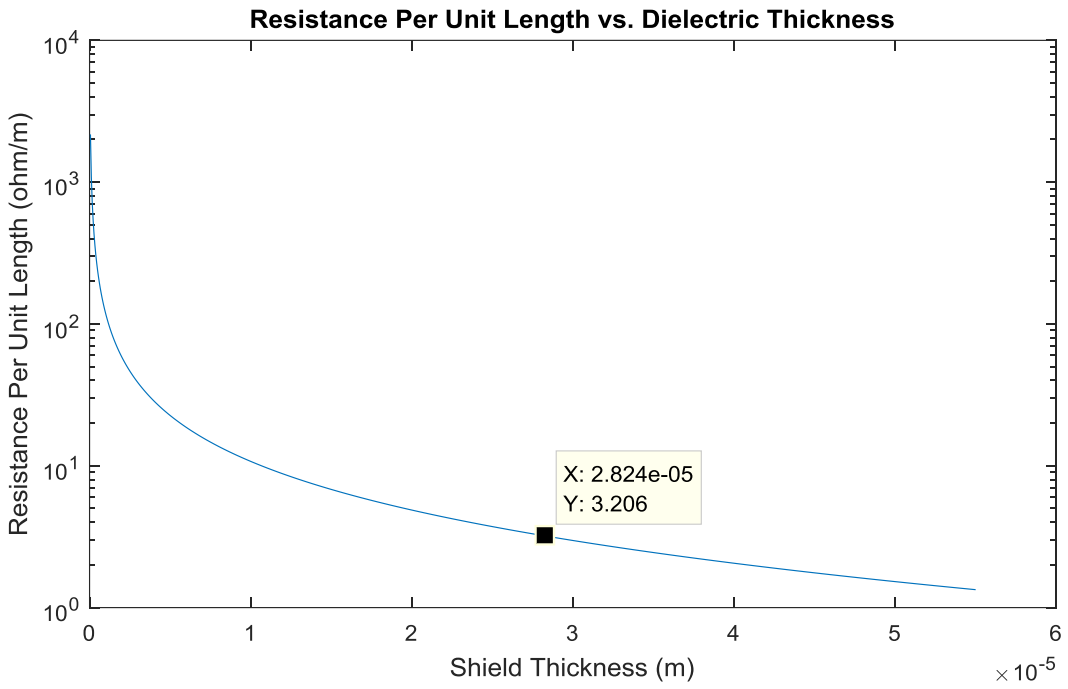


Figure 3-6 Resistance per unit length in H/m versus shield thickness determined by using (24).

Another important property of a coaxial transmission line is the characteristic impedance of the cable. Most generally, the characteristic impedance, Z_0, is derived from the telegrapher equations as [26]:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{26}$$

Where for a coaxial cable R is the total resistance per unit length (Ω/m), L is the total inductance per unit length (H/m), G is the conductance per unit length (S/m), and C is the total capacitance per unit length (F/m). For low loss dielectrics and low loss conductors the characteristic impedance simplifies to the following as R and G are minimal [26]:

$$Z_0 \cong \sqrt{\frac{L}{C}} \tag{27}$$

Where the capacitance, C, per unit length, F/m, is [25]:

$$\frac{C}{l} = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln\left(\frac{r_c + t_d}{r_c}\right)} \tag{28}$$

Characteristic impedance and capacitance are other electrical properties that we are capable of measuring and serve as good values to compare measurements to analytical results. A summary of target microcoaxial geometry can be seen in Table 3-2.

Table 3-2 Summary of Target Microcoaxial Geometry for Fabrication Given PDN Requirements of RBudget and LBudget

Parameter	Target Value	Notes
r_c	>41μm	Determined using a core R_{Budget} of 3.20 mΩ/mm, copper core material, and the definition of R_{core} in (24)
t_d	<3.0 μm	Determined using L_{Budget} of 15 pH/mm and the definition of L in (25)
t_s	>28 μm	Determined using a shield R_{Budget} of 3.20 mΩ/mm, gold shield material, and the definition of R_{core} in (24)

For a conservative approach, it is desired to pick a larger core radius greater than 41 μm and a larger shield thickness greater than 28 μm to reduce the overall resistance of micro-coax. A lower resistance will keep micro-coax below the target characteristic impedance of 160 mΩ per wire (10 mΩ total for the entire device being packaged with 16 micro-coaxial cables). Similarly, a thinner dielectric than 3.0 μm is desired to minimize micro-coax inductance and also keep characteristic impedance below 160 mΩ per wire.

3.4 *Low Inductance Microcoax Fabrication*

We have developed a standard material set and fabrication process for power micro-coax fabrication. The process for fabricating discrete lengths of micro-coax is illustrated in Figure 3-7. Fabrication implementation was first described in [25]. Insulated wires, which were commercially available from wire manufacturers, formed the core and dielectric layers of the coax. The wire in this paper has a 62.5 µm Copper core radius, larger than the minimum allowable radius of 41.0 µm to reduce R_{Budget} of the core below 3.20 mΩ/mm. The wire also has a 12 µm Polyesterimide dielectric layer. The dielectric thickness is 9.0 µm larger than the initial targeted thickness but this was the smallest available from manufacturers. Because the dielectric layer is larger than desired, it is expected that our wire inductance will exceed 40 pH/mm and thus put us above our original target of 15 pH/mm, which under the most extreme conditions may cause the power coax to exceed voltage ripple requirements of 30 mV of the Kintex 7 FPGA.

The wires were mounted onto a fixture that is used throughout the fabrication process. To prepare the wires for a shield deposition, a seed layer is thermally evaporated onto the dielectric with a Titanium layer of 50 nm and a gold layer of 300 nm. To ensure the seed was continuous around the wire circumference, the fixture is flipped in between two evaporation runs. Photoresist beads are placed throughout the wire to prevent shield metal from plating in those areas. This is necessary to gain access to the core in later etching steps. A gold sulfite bath purchased from Transene is used to plate a 55 µm gold shield. For the same reasons as the core metal we fabricated a thicker shield than the target value to reduce micro-coax resistance even further below a shield R_{Budget} of 3.20 mΩ/mm.

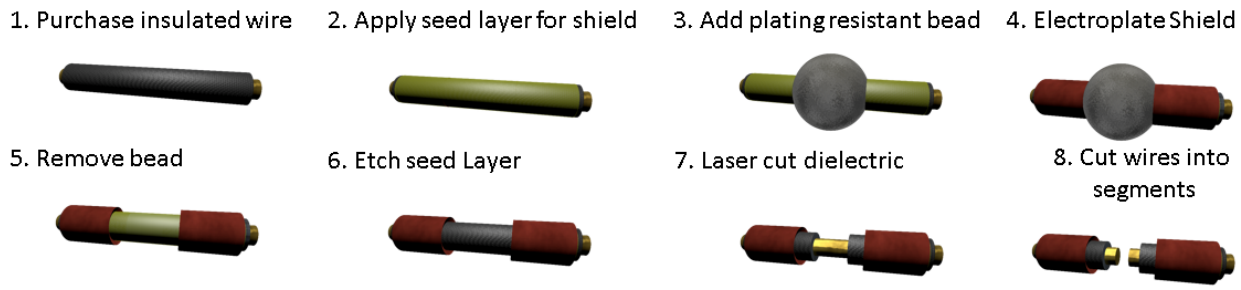


Figure 3-7 Fabrication steps for developing stripped microcoaxial cables.

To create individual wire segments with the core exposed for bonding and integration, the photoresist beads were removed in acetone. The seed layer was etched in both a Potassium Iodine (to remove the gold layer) and a Hydrofluoric Acid based solution (to remove the titanium layer), both purchased from Transene, and the polymer dielectric is removed using a JPS UV laser with a wavelength of 248 nm. A Scanning Electron Microscope (SEM) image of a wire after the fabrication process can be seen in Figure 3-8. Since the core was exposed on each end of the segment as part of fabrication, the segment was now ready for bonding to the characterization board.

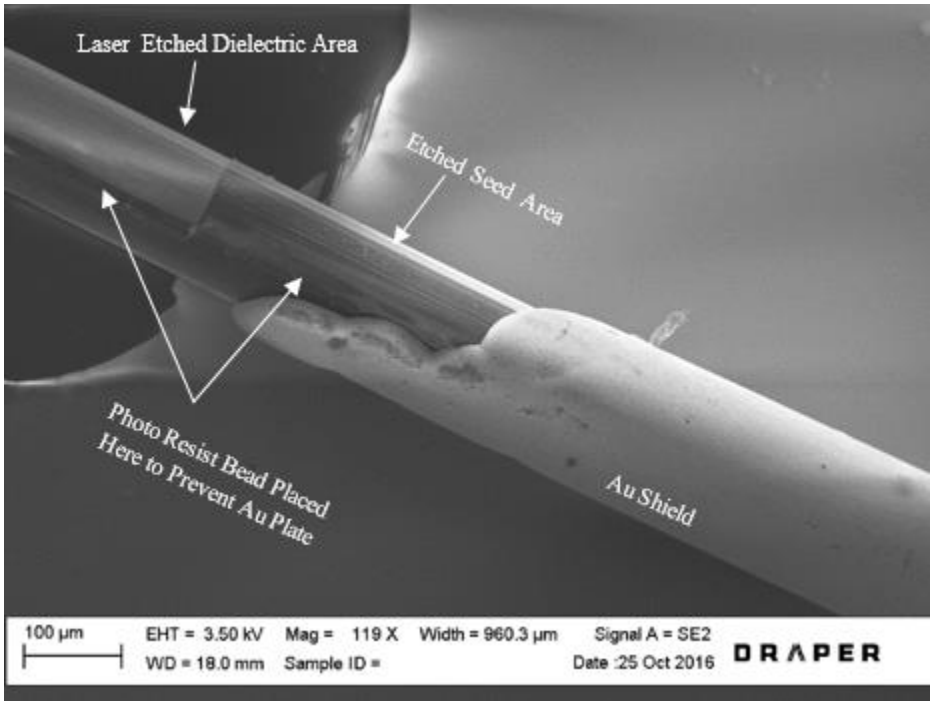


Figure 3-8 SEM image of micro-coax after fabrication process.

3.5 *Two-Port RF Characterization*

To characterize micro-coax, fitted s-parameters gathered from vector network analyzer (VNA) measurements are fit to a quasi-distributed model built in Advanced Design System (ADS). The quasi-distributed model was made to represent a micro-coaxial transmission line and its connection joints. From proper fitting to this model it was possible to determine the inductance, capacitance, and characteristic impedance of fabricated coaxial cables. To verify that measurements and modeling were being done properly, results were compared to results from electromagnetic simulations in Ansys High Frequency Electromagnetic Field Simulation (HFSS).

3.5.1 Vector Network Analyzer Measurements

VNA measurements of micro-coax were taken using a two-port RF test fixture. Each port on the fixture, also known as a "launch", has patterned Ground-Signal-Ground (GSG) pads for matching GSG probes with a 250 µm pitch. The core of the wire was soldered to the signal pads of the fixture. Norland 86H Insulating epoxy was used to protect the core attachment and EpoTek H20E silver conductive epoxy was used to connect the shield to the ground pads of the fixture. An image of the fixture is illustrated in Figure 3-9. The RF board itself is made of 1 Mil thick Polyimide film with 0.7 Mil thick patterned Copper. The total thickness of the board is 4.40 Mils. The boards are mounted onto glass slides for mechanical support.

Figure 3-9 Schematic of 2-port RF test fixture used for electrical characterization of micro-coax.

To test, a 2-port Vector Network Analyzer (VNA) from Agilent Technologies (Model Number: E8363B) was used to sweep voltage linearly from 10 MHz-2.0 GHz. To de-embed the effects of the board, a separate VNA measurement was made of a single launch. Two-port de-embedding was implemented to gather s-parameter results of micro-coax. Prior to measurements, a standard Short, Open, Load, Thru (SOLT) calibration was made using a CS-9 calibration substrate from Pico Probe.

3.5.2 Circuit Modeling in Advanced Design System (ADS)

A circuit model of micro-coax and its attachment points can be seen in Figure 3-10. This model consists of 50 Ω termination points at either end modeling the loads on each port from the two-port network VNA. The model also consists of two inductors on either end modeling the attachment points of the micro-coax. Four individual cells, each of which are 5 mm long segments, model the micro-coax itself.

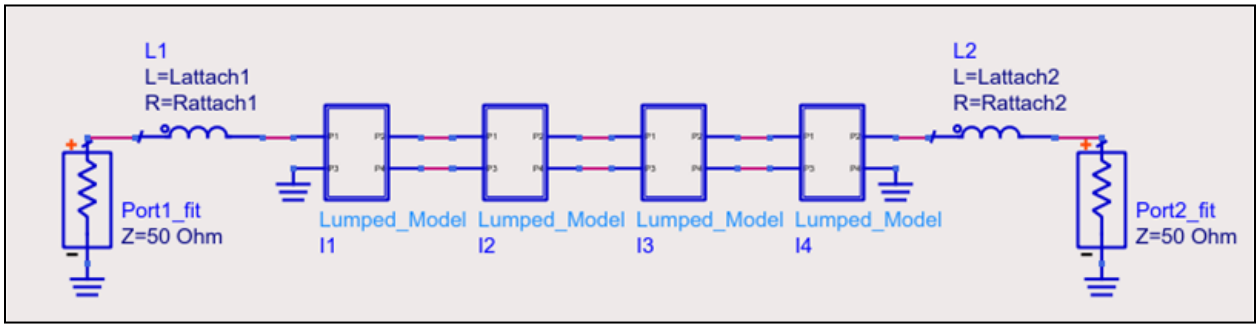


Figure 3-10 Discrete Model of Micro-Coax Modeled in Advanced Design System (ADS). Model Represents a Total Wire Length of 20 mm.

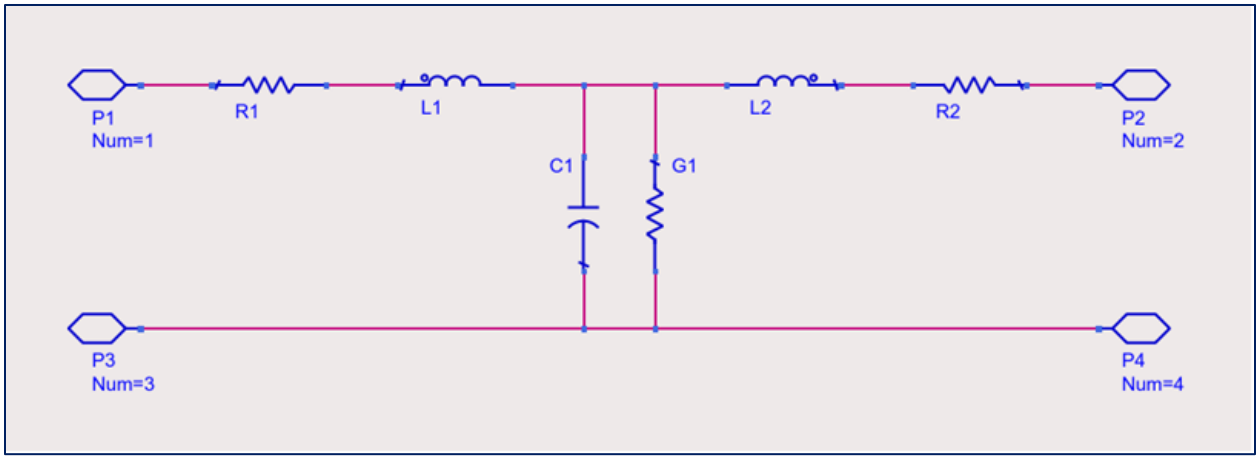


Figure 3-11 Cell Model of Micro-Coax Segment Representing 5 mm Length of Wire.

An individual cell segment can be seen in Figure 3-11. Within each segment a resistor and inductor are paired in series to model the shield and core conductors. A capacitor and resistor are paired in parallel to model the dielectric and spacing between the core and shield of the micro-coax.

This model is capable of isolating the micro-coax inductance from the inductance of the coaxial cable's joints. An optimization algorithm was used to adjust parameters until the modeled s-parameters matched measured VNA s-parameters. From fitted results, the inductance, capacitance, and characteristic impedance of each micro-coax was determined.

3.6 *Results*

The properties of fabricated micro-coax described in this paper are: a core radius of 64.5 µm, shield thickness of 55.0 µm, core resistivity of copper equal to $1.7 \cdot 10^{-7}$ Ωm taken from [24], shield resistivity of $3.30 \cdot 10^{-8}$ Ωm [25], dielectric thickness of 12 µm, and a dielectric constant of 3.1, taken from [27]. DC Resistance is estimated as 2.30 mΩ/mm using (24). Inductance is estimated to be 40 pH/mm using (25). Theoretical capacitance is estimated to be 0.98 pF/mm calculated from (28). The characteristic impedance is estimated as 5.98 Ω calculated from (27). These results

give us a sense of expectations. However, for comparison to VNA measurements, a better estimate is made using ANSYS High Frequency Electromagnetic Field Simulations (HFSS).

Measured resistance per unit length, inductance per unit length, capacitance per unit length, and characteristic impedance for this cable can be seen in Table 3-3. These were fitted in the ADS model from 10 MHz-2 GHz and provide a good match to both measured, from VNA, and simulated, from HFSS, frequency response. Measured resistance is also shown, but this was DC resistance measured with a four point probe. Measured and simulated capacitance per unit length are in good agreement, each 0.93 pF/mm and 0.94 pF/mm respectively. The measured and simulated inductance per unit length are 40 pH/mm and 50 pH/mm respectively; in good agreement with analytical results. Measured and simulated characteristic impedance is 6.56 Ω and 7.29 Ω respectively which is also in good agreement with theoretical calculations.

Table 3-3 Analytical, Measured, and Simulated Electrical Properties of Fabricated Microcoax for Power Distribution

	L (pH/mm)	C (pF/mm)	Z_0 (Ω)	R(mΩ/mm)
Analytical	40	0.98	5.98	2.30
Measured	40	0.93	6.56	2.00
Simulated	50	0.94	7.30	--

3.7 *Conclusions and Future Work*

We have fabricated and characterized low impedance micro-coaxial cables that could be used in lithography-free microelectronic systems suitable for applications with demanding power requirements. We have developed a method of determining coaxial geometry and material sets from a PDN analysis. This approach is applicable to a variety of design problems, but has been demonstrated using the specific example of the Kintex 7 FPGA. Future analysis will aim to include more parameters in the PDN, such as the inductance, capacitance, and resistance contributions of

substrates and package leads. These components may introduce additional resonances in Z_{pdn} that will further limit R_{Budget} and L_{Budget} for micro-coax.

Another method of limiting R_{Budget} and L_{Budget} further is to reduce the allowable voltage ripple. A smaller voltage ripple will result in a smaller Z_{pdn} target given the same current requirements. This is conservative method that may be useful to pick usable micro-coaxial geometry with low enough resistance and inductance for simpler PDN designs or to account for possible skin effect losses at higher frequencies. Generally a micro-coaxial cable with a larger core, larger shield thickness, and thin dielectric will reduce overall micro-coax characteristic impedance.

Working fabrication, stripping, and connection methods have been developed and demonstrated to characterize and test micro-coaxial cables. From measurements we have achieved a resistance of 2.0 mΩ/mm and an inductance of 40 pH/mm. Good agreement exists with our electric field simulations which report an inductance of 50 pH/mm. Good agreement also exists in our analytical solutions at high frequency reported to be 40 pH/mm. We have also shown good agreement in analytical, measured, and simulated results for microcoax capacitance and characteristic impedance which has provided us confidence in our testing methods. Measured capacitance and characteristic impedance are 0.93 pF/mm and 6.56 Ω respectively, which compare well to our simulated results of 0.94 pF/mm and 7.30 Ω. We have also shown agreement for our DC resistance analytical calculations which report a value of 2.3 mΩ/mm. We have managed to maintain within our R_{Budget} but inductance remains challenging. A thinner dielectric is needed.

Further future work includes lowering the inductance of micro-power coax even further by minimizing dielectric thickness. In house fabrication methods such as vapor coated Parylene C and dielectrics deposited by Atomic Layer Deposition will allow for thinner dielectrics. Other tests that are of interest for further characterization include cross-talk testing of micro-coax.

4 Co-fabrication of Micro-Coaxial Interconnects and Substrate Junctions for Multi-Chip Microelectronic Systems

4.1 *Introduction*

Microwave and RF applications are broad, including advanced communication systems, antenna and radar design, navigation and weather, as well as medical diagnostics. Microwave and RF frequencies are defined within the 30MHz – 300 GHz band. The advantage of utilizing high frequency waves include higher bandwidth communications, high gain and target detection in radar, the ability to penetrate the ionosphere, and the ability to detect molecular resonances in biomedical sensing [6]. Enhanced bandwidth, gain, and resolution are unique and enabling advantages motivating the implementation of Microwave and RF frequencies into a diverse set of microelectronics. A study done by Yole reports that RF modules made up to 65% of System in Package (SiP) components [4] in 2017.

There are key problems that drive packaging constraints of high frequency modules. Packages may introduce parasitics that influence performance at higher frequencies [28] [29] [30]. They may also introduce discontinuities or impedance mismatches that reduce performance [7]. Additionally, due to the demands for miniaturization, packaged high frequency modules face electromagnetic interference [31]. In most cases high frequency modules are paired with other microelectronic devices making heterogeneous integration more difficult [31].

There are many competing methods to address packaging needs. For instance, SiGe and GaAs

substrates provide excellent high frequency performance, but can be difficult and expensive to integrate with multi-chip modules (MCM) [32]. Flip chip bonding is a popular SiP method of integration and introduces low insertion losses [29]. In [30] only 0.4 dB of insertion loss at 9.5 GHz was introduced when used to package MCMs in a liquid crystal polymer package. Wire bonding is another rapid method of integration and may also be used to package MCMs [7]. However, current wire bonding introduces discontinuities [7] [33] and may contribute as much as 2.2 dB of insertion loss at 9.5 GHz as shown in [30] with a similar liquid crystal polymer package. In addition, wire bonds may exhibit significant cross-talk and EMI problems. In one study done in cross talk was as high as 0 dB at 10 GHz [7]. Wire bonds may be unsuitable, in some situations, for power distribution networks [22].

In this paper we are interested in utilizing the speed of wire bonding as a method to minimize the time it takes to progress from an electrical schematic to a built, testable device. However, to combat the problem of cross-talk and EMI, we propose using shielded wire bonds for all interconnects, both power and signal, to eliminate the need for lengthy simulation and layout iterations that are necessary to build multi-chip microelectronic systems. We are interested in investigating wire bonding over flip chip methods because wire bonding allows provides a versatile platform to form interconnects between bare die components as well as interconnects between packaged dies. In addition, we developed low impedance shielded wire bonds suitable for power distribution at DC.

4.2 *In-Situ Microcoax Fabrication and Attachment*

Microcoax have previously been implemented in rapid packaging schemes. One particular demonstration authored by Sean Cahill, Eric Sanjuan, and Levine Lee, from BridgeWave Communications and Kulicke & Soffa Industries [21], has motivated the work in this paper. Their

process involves an in-situ attachment and fabrication strategy that integrates microcoax for signal distribution in multi-chip modules. An illustration of the process can be seen in Figure 4-1 [21].

The process begins by wire bonding to signal pads to create core attach. The core wire is coated by a protective conformal dielectric. To create access to ground the dielectric is laser etched and removed. Laser etching is preferred to lithographic patterning as it is capable of removal of polymer dielectrics and the process may be automated for more rapid integration. Finally, the formation of the coaxial shield is made by depositing a metal adhesive layer and electroplating to a fuller shield thickness. Cahill, Sanjuan, and Lee have been successful at fabricating signal coax 80 μm in diameter. Transmission line performance reported in their work include losses less than 0.5 dB for 3.0 mm long wires. Cross-talk between wires was measured to be -40 between 25-50 GHz [11].

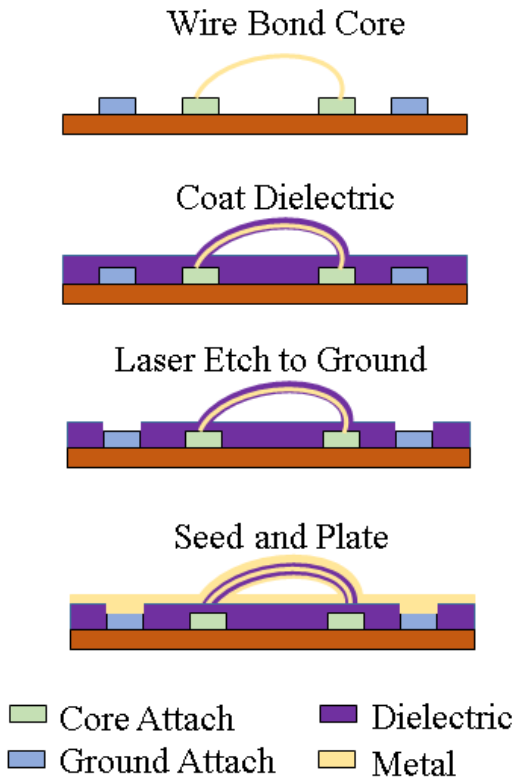


Figure 4-1 Micro-Coax Fabrication introduced in [11]. The process begins by wire bonding Au to create core attach. Bonding is followed by a conformal dielectric coating. The dielectric is laser etched to expose ground locations. Finally, the shield is fabricated by depositing an adhesive layer and electroplating metal.

In this work, we will define processes and build coax appropriate for both signal and power distribution because a fully integrated multi-chip module will require both types of coax. Additionally, these techniques will eliminate the lengthy layout and fabrication processes associated with separate methods for power and signal distribution. Signal coax is well understood and has previously been studied for RF applications such as in [21] [6] [8] [9] [10]. For the majority of applications target characteristic impedances for signal coax range from 30Ω-70 Ω. Here, we extend the work done by Cahill, Sanjuan, and Lee, we describe RF characterization of micro-coax for power distribution using low impedance microcoax. Wires are fabricated by their co-fabrication and attachment process. In extension of previous work, we have explored thin dielectrics such as HfO_2 deposited via Atomic Layer Deposition (ALD) and thin vapor deposited

parylene C coatings. We also compare predicted electrical properties to measurements, using measured cross sectional geometry and s-parameters to compare with simulations. Finally, we determine the cross-talk integrity between adjacent wires and compare our results to those of Cahill, Sanjuan, and Lee.

4.3 *Microcoaxial Fabrication and Analytical Calculations of Capacitance, Inductance, and Characteristic Impedance*

All wires have a 25.4 µm diameter gold core that has been wire bonded to signal pads on an RF board, a dielectric coating, an adhesion metal bi-layer, and a 5.0 µm Au plated shield. In this work we find that conformal coatings drive microcoaxial fabrication. Coatings include the thin 100 nm thick dielectric hafnium, HfO_2, deposited via Atomic Layer Deposition (ALD), thin 1.0 µm thick vapor coated parylene C, and 38 µm thick vapor coated parylene C. Conformal adhesive metal layers are also key to forming an effective plated metal coaxial shield. It has been possible to estimate the electrical properties of each cable by evaluating the cross-sectional geometry, measuring film thicknesses, and estimating dielectric properties of each fabricated cable.

4.3.1 Low Inductance Microcoax with HfO_2 Dielectric

A focus ion beam (FIB) cross section of a microcoaxial cable with a thin HfO_2 dielectric can be seen in Figure 4-2. The cables fabricated this way each have a 25.4 µm diameter core Au wire bonded to signal pads on an RF board with a Kulicke and Soffa wire bonder. The HfO_2 was deposited with a Cambridge Nanotech Savannah Atomic Layer Deposition tool with a tetrakis(dimethylamido)hafnium (TDMAH) precursor heated to 75ºC. The chamber temperature was set to 200ºC, the pulse time for TDMAH was set to 0.20 s, the purge time for TDMAH was set to 10 s, followed by a 10 s purge of water vapor (H_2O) to achieve a deposition rate of 1.01 Å/cycle. 1000 cycles were used to achieve a total thickness of 100 nm. No pretreating was needed

to prepare the surface, including the gold wire bonds or the RF board, prior to ALD for an effective deposition. This thin dielectric enables the microcoaxial cable to have a low inductance and makes it unique compared to signal microcoaxial cables that have larger impedances. ALD allows conformal coating on all sides of the core, precise thickness control, and pinhole free deposition.

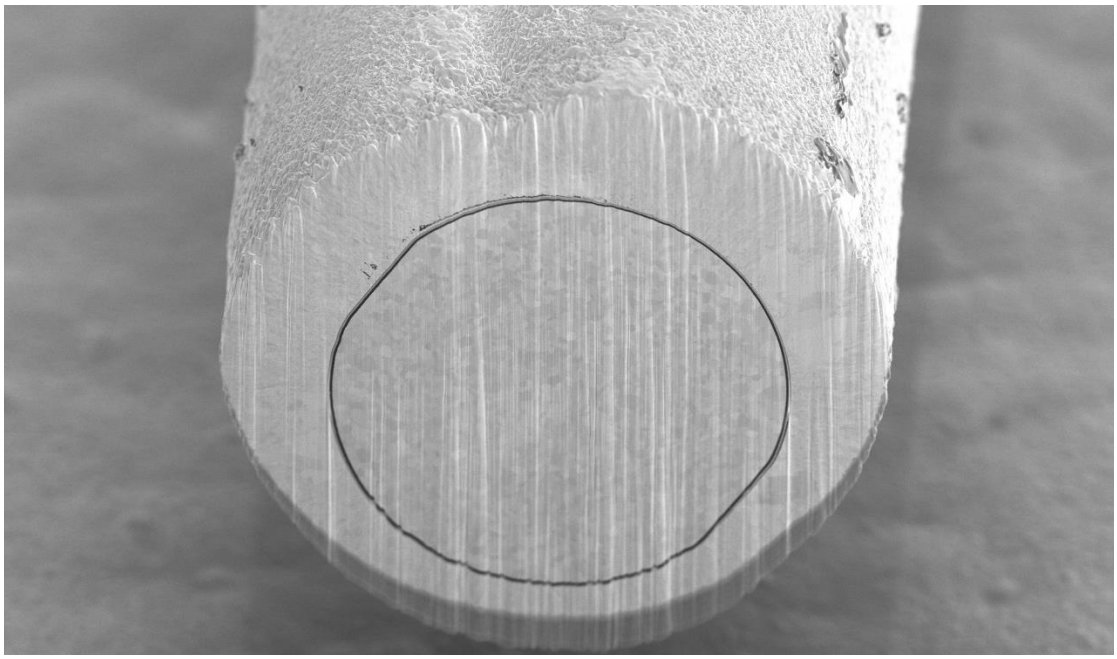


Figure 4-2 FIB cross section of micro-coax with 25.4 µm Au core, 100 nm HfO_2 dielectric, an adhesion and seed layer of Cr and of Au, and a 5.0 µm electroplated Au shield.

After ALD, the entire board, including all pads, is coated with HfO_2. Therefore, to expose the ground pads on the RF board a UV laser with a wavelength of 248 nm from JPS Advanced Technology was used to etch deposited HfO_2 from those locations. Laser power was set to 0.220 W and pulsed 10 times. Spot size of the laser was square and set to cover an area of 100 µm x 100 µm; within the size of the ground pads which cover an area of 200 µm by 200 µm.

The shield was fabricated by sputtering an adhesive bi-layer of 20 nm of chromium and 200 nm of Au using a dual gun DC Magnetron sputter tool (NSC3000, Nanomaster Inc). Argon, Ar, gas was used as the process gas at a pressure of 5.0 mTorr. The gun with a Cr target was set to a DC power level of 200 W and the gun with an Au target was set to a DC power level of 150W. Cr

deposition rates were measured to be 3.40 Å/s and Au deposition rates were measured as 7.0 Å/s. Base pressure was recorded as $1.2 \cdot 10^{-6}$ Torr. The wires were sputtered twice each at an angle of 45º when placed on the stage of the sputter tool; between runs the board was flipped. This improves conformal coverage. An Au sulfite bath purchased from Transene was used to plate a 5.0 µm shield. Current density was 2.0 mA/cm^2, bath temperature was 60ºC, and the plating rate was approximately 1.0 µm/min [26] The resistivity of the Au shield is measured, via four point probe, to be $3.30 \cdot 10^{-8}$ Ω·m [34].

4.3.2 Low Inductance Microcoax with Parylene C Dielectric

A FIB cross section of a microcoaxial cable with a thin parylene C dielectric can be seen in Figure 4-3. These wires were fabricated similarly to the HfO_2 wires except with a vapor coated parylene C dielectric. The core is 25.4 µm diameter wire bonded Au, with a 1.0 µm vapor coated parylene C dielectric deposited using a PDS2010 Parylene Deposition System from Specialty Coatings Systems (SCS). The furnace, chamber, and vaporizer temperatures were set to 690ºC, 135ºC, and 175ºC respectively. 2.0 g of dimer is used per µm of parylene C film thickness as estimated from previous depositions. The same JPS laser settings are used except 20 pulses are necessary to etch through 1.0 µm of parylene C. The same shield parameters are also used to fabricate these wires. As in the HfO_2 wires, low inductance is enabled by a thin dielectric.

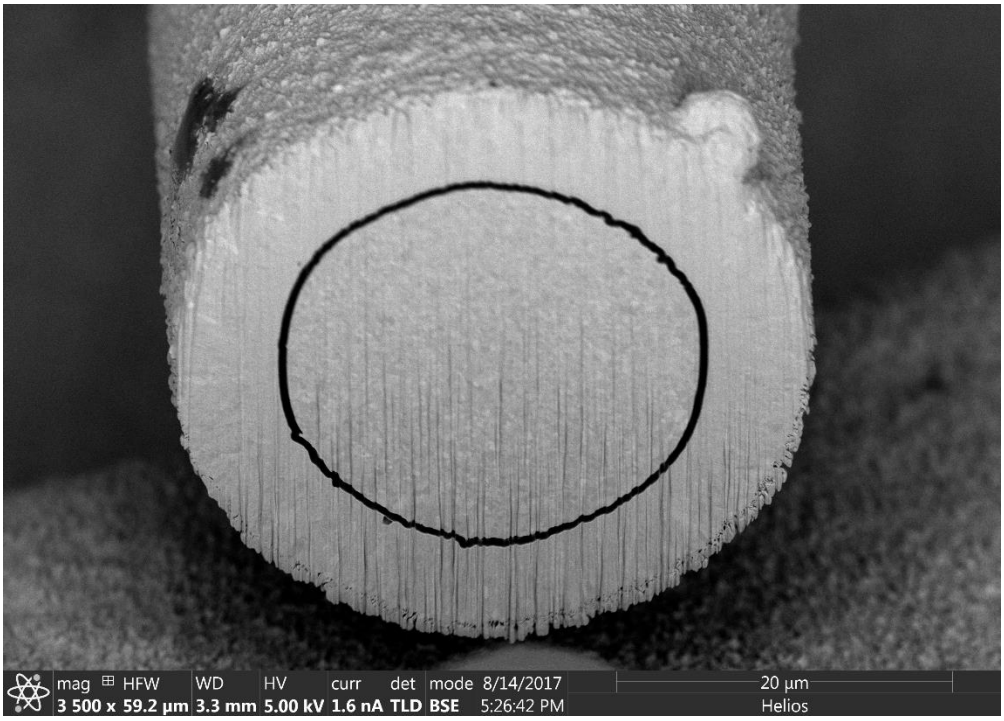


Figure 4-3 FIB cross section of micro-coax with 25.4 µm Au core, 1.0 µm parylene C dielectric, an adhesion and seed layer of sputtered Cr and of Au, and a 5.0 µm electroplated Au shield.

4.3.3 Signal Microcoax with Parylene C Dielectric

A microscope image of a potted cross section of a signal microcoaxial cable can be seen in Figure 4-4. These wires were fabricated with the same process as the thin parylene coated wires. These wires have a 25.4 µm diameter Au wire bonded core and a 38.0 µm vapor coated parylene C dielectric. 76 g of dimer was used for deposition. The ground locations on the RF board were exposed by laser etching the parylene C with 420 pulses of UV laser. The same shield parameters were used to fabricate these wires. Unlike the low inductance microcoax, these wires were targeted to have a 50Ω characteristic impedance.

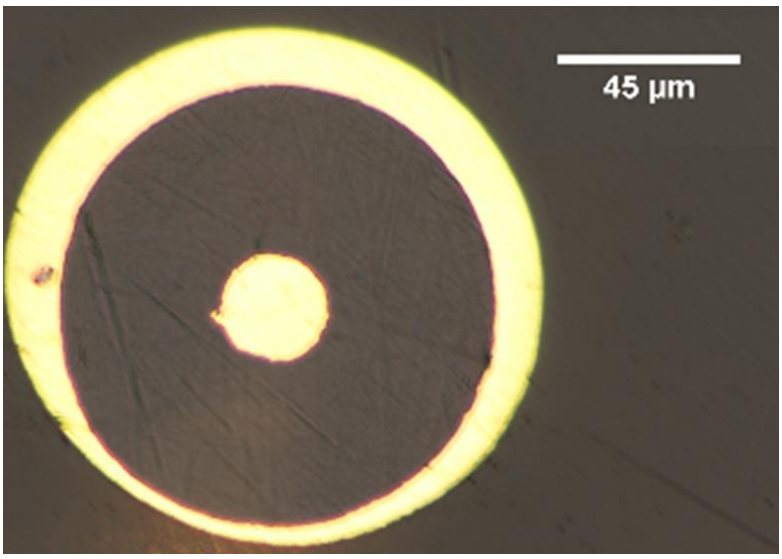


Figure 4-4 Potted cross section of micro-coax with 25.4 µm Au core, 38.0 µm parylene C dielectric, an adhesion and seed layer of sputtered Cr and of Au, and a 5.0 µm electroplated Au shield.

4.3.4 Analytical Derivations for Capacitance, Inductance, and Characteristic Impedance for Fabricated Microcoax

The ideal inductance, *L*, per unit length of wire, *l*, for an infinite coaxial cable with tangential fields is [6]:

$$\frac{L}{l} = \frac{\mu_0 \mu_r}{2\pi} \ln\left(\frac{r_c + t_d}{r_c}\right) \tag{29}$$

Where μ_0 is the magnetic permittivity of free space, μ_r is the magnetic permittivity of the dielectric, r_c is the radius of the core in m, and t_d is the dielectric thickness in m. Similarly, the ideal capacitance, *C*, per unit length of wire is [6]:

$$\frac{C}{l} = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln\left(\frac{r_c + t_d}{r_c}\right)} \tag{30}$$

Where ε_0 represents the electric permittivity of free space, and ε_r is the dielectric constant. Another important property of a coaxial transmission line is the characteristic impedance of the cable. Most generally, the characteristic impedance, Z_0, is derived from the telegrapher equations as [6]:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{31}$$

Where R is the total resistance per unit length in Ω/m and G is the conductance per unit length in S/m. For our purposes G is nearly zero since we choose highly electrically resistive dielectrics. A low loss transmission also assumes R is nearly zero, since we choose highly conductive metals for our core and shield, which results in:

$$Z_0 \cong \sqrt{\frac{L}{C}} \tag{32}$$

where Z_0 is in Ω. To predict C, L, and Z_0,of the wires that have been fabricated, r_c, t_d, μ_r, and ε_r were measured or estimated from microscope images, ellipsometer measurements, profilometer measurements, pinhole tests, and from prior literature, for all three sets of wires. From FIB cross sections the minimum and maximum core radii were 12.0 µm and 13.0 µm respectively. Film thickness measurements of ALD HfO_2 and parylene C were made using a Bruker Dektak XT-S profilometer and an Ocean Optics Nanocalc Thin Film Reflectometer. For ALD HfO_2 thickness was measured to be 100 nm. This is very uniform due to ALD's high uniformity. For thin parylene C coatings thickness was measured to be 0.80-1.20 µm. For thicker parylene C coatings thickness was measured to be 37.0-46.5 µm. μ_r is estimated to be 1.0 since HfO_2 and parylene C are not ferromagnetic materials. ε_r is estimated from literature. For HfO_2, ε_r is estimated to be 16-40 from [35] and [36] for frequencies less than 1 GHz. ε_r for parylene C is estimated to be 2.95-3.15 from [33], [37], [38] for frequencies less than 6.0 MHz.

Analytical calculations for L, C, and Z_0 per unit length are shown in Table 4-1 using (29),(30), and (32), measured wire geometry, and estimated dielectric properties. Expected inductance for the

HfO_2 and thin parylene C wires is low, as desired, estimated to be 1.40-1.70 pH/mm for HfO_2 and 13.6-21.0 pH/mm for thin parylene C. This is mainly due to the thin dielectric layers. This also allows the HfO_2 and thin parylene C wires to have low characteristic impedances of 0.07-0.13 Ω and 2.30-3.70 Ω respectively. These low impedances are useful for distributing power effectively as low impedances are desirable for designing power distribution networks [39]. Capacitance for these power microcoaxial cables are expected to be 104-298 pF/mm for HfO_2 wires and 1.60-2.60 pF/mm for thin parylene C wires. For the thick parylene C coated wires characteristic impedance is expected to be 44-57 Ω. These analytical estimates of *C*, *L* and Z_0 per unit length will be used to compare to values gathered from high frequency electrical measurements with a Vector Network Analyzer (VNA) and Advanced Design System (ADS) circuit simulations.

Table 4-1 Expected L, C, and Z_0 From Fabrication

Symbol	Units	HfO_2 Power Coax	Parylene C Power Coax	Parylene C Signal Coax
L/l	pH/mm	1.40-1.70	13.6-21.0	262-326
C/l	pF/mm	104-298	1.6-2.60	0.10-0.13
Z_0	Ω	0.07-0.13	2.30-3.70	44-57

4.4 *Extraction of Electrical Properties of Microcoax With 2-Port RF Network Analysis*

To characterize each fabricated microcoaxial wire, scattering parameters (s-parameters) gathered from two-port VNA measurements were fit to two circuit models built in ADS. These circuit models were used to compare measured results to analytical calculations. From proper fitting to each model it was possible to determine the inductance, capacitance, and characteristic impedance of fabricated coaxial cables. Additionally, modeling of the RF launch board was necessary to de-embed the s-parameters of the microcoaxial cables from the board.

4.4.1 VNA Measurements

VNA measurements of micro-coax were taken using a two-port RF test fixture. An image of the fixture is illustrated in Figure 4-5. Each port on the fixture has patterned Ground-Signal-Ground (GSG) pads for matching GSG probes with a 250µm pitch (Model 4A) from GGB Industries. Prior to fabrication, the pad locations for the GSG probes are masked using polyimide tape to prevent dielectric and metal from coating the GSG pads. The core of the wire is attached to the signal pads on either launch. Core attach is protected by the HfO2 or parylene C dielectric coating. The ground pads were exposed by laser etching, and the seed and Au plated metal coat create the ground attach of the shield.

Figure 4-5 Illustration of one pair of launches of the RF board used for VNA measurements of microcoax. Microcoax is attached onto two launch segments, each with corresponding GSG pads, that are 3500 µm apart. GSG probes from a VNA probe station is used to sweep voltage form 10 MHz-12GHz.

The RF board substrate is made of polyimide and copper films with 18 µm thick patterned Au pads. The total thickness of the board is 112 µm. The spacing between each launch, which dictates the approximate wire length, is 3500 µm. The boards were mounted onto glass slides for mechanical support. An image of a board after fabrication can be seen in Figure 4-6.

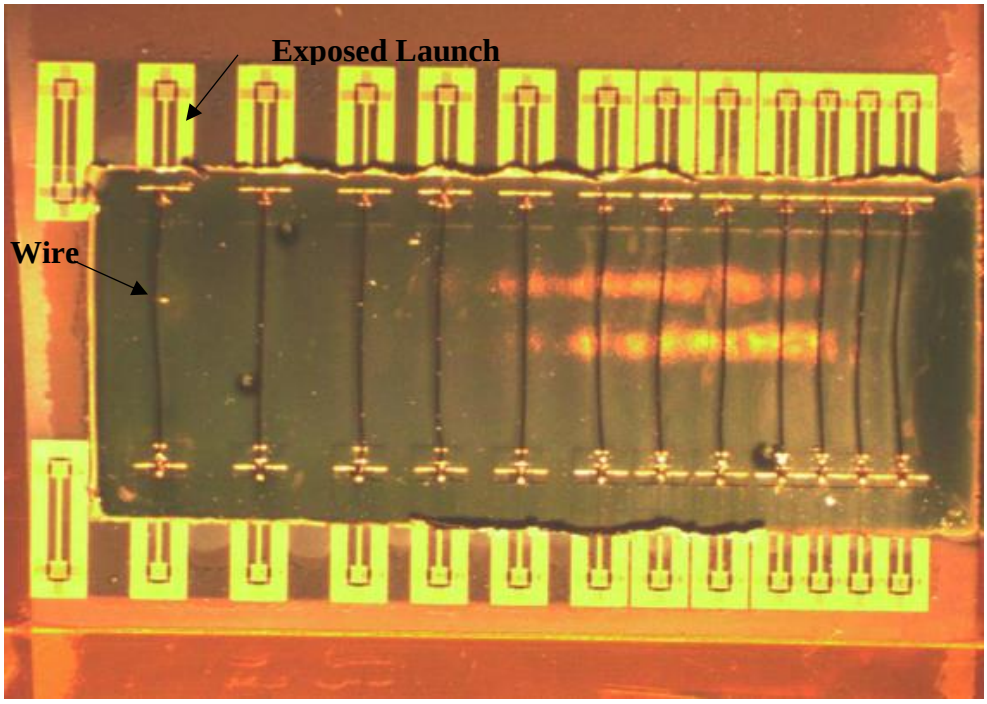


Figure 4-6 Microscope image of RF board with 12 microcoaxial cables after fabrication.

To test, a 2-port Vector Network Analyzer (VNA) from Agilent Technologies (Model Number: E8363B) was used to sweep voltage linearly from 10 MHz-12.0 GHz. Prior to measurements, a standard two port Short, Open, Load, Thru (SOLT) calibration was made using a CS-9 calibration substrate from GGB Industries. A total of 16001 data points were collected from each wire and each measurement utilized an IF bandwidth of 10 kHz to increase the number of spectrum acquisitions in a single sweep.

4.4.2 ADS Circuit Simulations

To determine the capacitance, inductance, and characteristic impedance of the coaxial cables, two circuit models in ADS were built to simulate the electrical properties of microcoax. Each circuit model underwent an s-parameter simulation with a linear frequency sweep from 10 MHz-12 GHz with 16001 data points to match VNA measurements. VNA measurements were fit to circuit models using a gradient optimization algorithm.

The circuit models that worked best to fit to the wires with 100 nm HfO_2 and 1.0 µm of Parylene C was a model with capacitance, inductance, and resistance. A separate transmission line model was used to measure characteristic impedance. The only circuit model that worked to fit the signal coaxial cables with 38 µm of parylene C dielectric was the transmission line model; which allowed us to measure the characteristic impedance for signal wires. Capacitance, inductance, resistance, and characteristic impedance were all variables used in optimization. An image of an ADS circuit model with coax capacitance, inductance, and resistance can be seen in Figure 4-7. An image of an ADS transmission line circuit model with characteristic impedance can be seen in Figure 4-8.

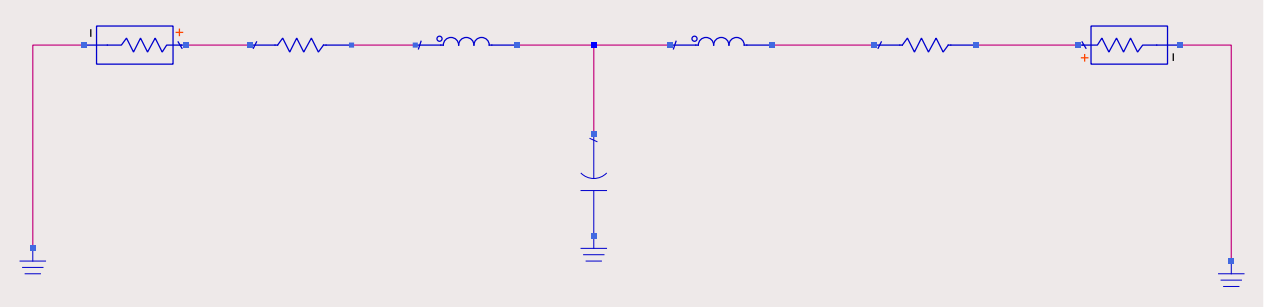


Figure 4-7 ADS circuit model of microcoax with capacitance, inductance, and resistance used to fit VNA data to gather electrical properties of measured wires.

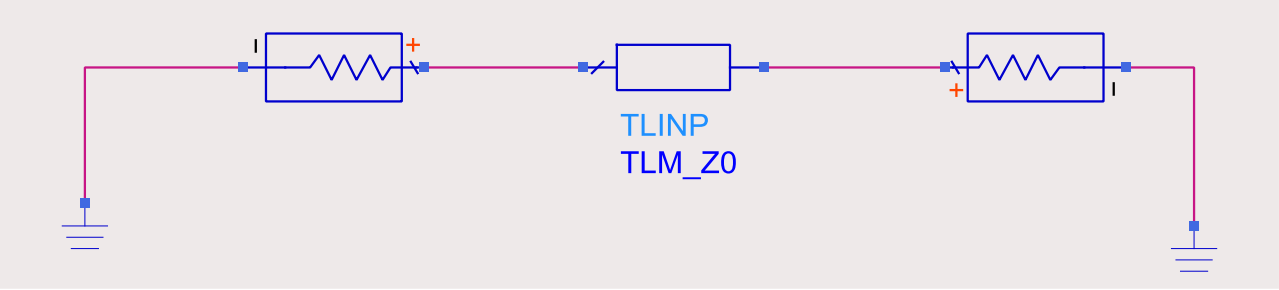


Figure 4-8 ADS transmission line model used to fit characteristic impedance to measured VNA s-parameters.

In addition to modeling microcoax, a model of the RF board was needed for of model based de-embedding. De-embedding is necessary to distinguish the s-parameters of microcoax from the substrate. Measurement based de-embedding of the substrate proves difficult for this fabrication process due to the excess dielectric and shield metal films that alter the substrate properties after

the fabrication process. Thus we cannot directly measure the substrate separately from the wires. Additionally the fabrication process makes access to the GSG pads on the unmasked portions of a launch difficult. A model of a launch after the fabrication process with a corresponding SEM image of the RF board can be seen in Figure 4-9.

Each launch model includes a substrate capacitance which had been previously measured from prior VNA measurements to be 21.0 fF. This capacitance represents the capacitance of the substrate without any wires or added films. To model the effects of fabrication two transmission lines with individual characteristic impedances represent the masked and unmasked portions of the launch. The masked area represents a length of transmission line without added dielectric and metal and the unmasked area represents a length of transmission line with added material. Each length was measured after fabrication via a microscope for each wire and used as fixed variables during each simulation. At the unmasked end of the model an additional capacitance variable is used to model the effects of an added capacitance due to the spacing between the patterned board metal and the added shield metal. The characteristic impedance and added capacitance each served as optimization parameters whereas the substrate capacitance and transmission line lengths were fixed. For each circuit model of microcoax de-embedding was implemented at both ports and results with de-embedding were compared to results without de-embedding.

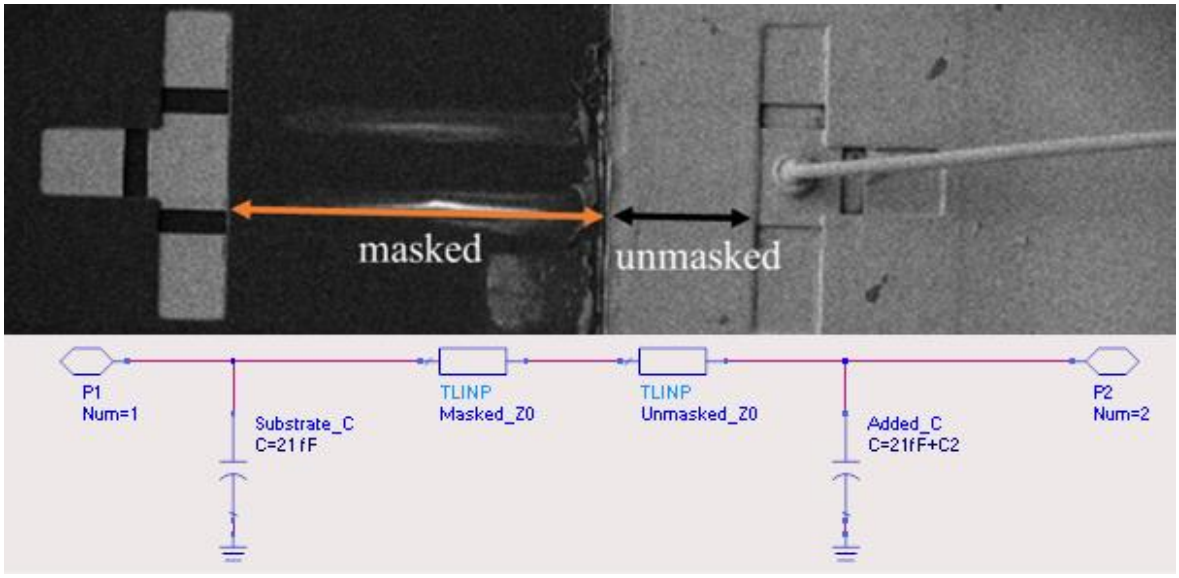


Figure 4-9 Substrate model of RF board after fabrication used to de-embed substrate s parameters from microcoax. In this model a launch is represented by the masked and unmasked area of the board from dielectric and metal coated films.

4.5 *Measured S-Parameter Results*

For each microcoaxial cable s-parameters from VNA measurements and circuit simulations were plotted on a Smith chart and a frequency response plot to illustrate how well the circuit model fit measured results. From each fit, values for capacitance, inductance, and characteristic impedance were gathered. Data sets of electrical properties for each microcoax are tabulated in Table 4-2, Table 4-3, and Table 4-4. For each set of wires the average value for capacitance, inductance, and characteristic impedance as well as standard deviation is shown. Results for values with and without de-embedding are shown and compared to analytical values.

4.5.1 Electrical Results for Low Inductance HfO_2 Microcoax

The reflection s-parameters for power microcoax fabricated with HfO_2 dielectric can be seen in Figure 4-10. The measured reflection s-parameters at port 1, S_{11}, and port 2, S_{22}, are illustrated in red and blue respectively. The simulated s-parameters from circuit modeling port 1, S_{33}, and port 2, S_{44} are illustrated in pink and black. The plot shown in Figure 4-10 corresponds to the fit as a

result of VNA measurements and a circuit model with capacitance, inductance, and resistance components with model based de-embedding. As expected, there is a high capacitive reactance at lower frequencies due to the very thin 100 nm dielectric. At higher frequencies the s-parameters trend towards the short end of the Smith chart before gaining inductive reactance.

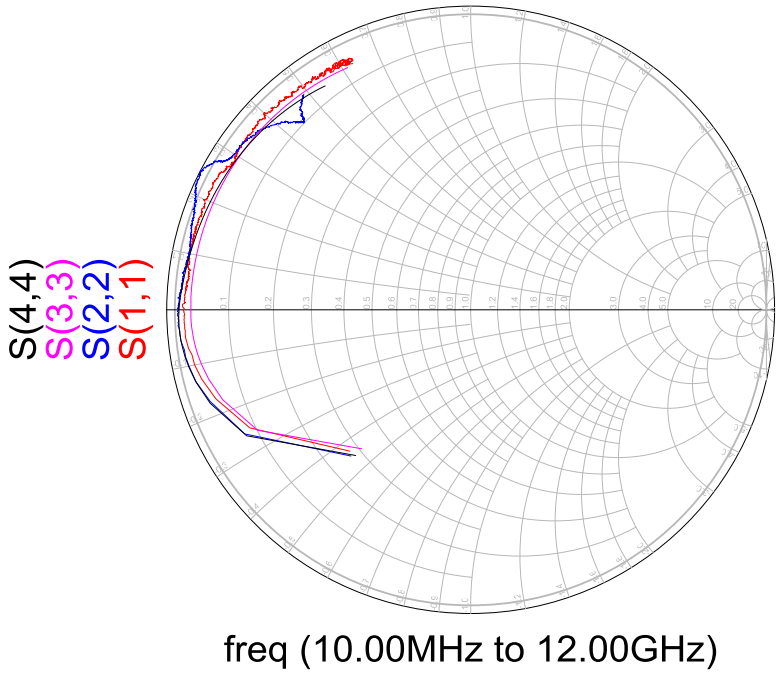


Figure 4-10 Reflection s-parameters from 10 MHz to 12 GHz plotted on a Smith chart. S-parameters were gathered from VNA measurements of microcoax with 100 nm of HfO_2 dielectric and from a de-embedded circuit simulation with capacitance, inductance, and resistance.

The transmission s-parameters from VNA measurements, S_{12} and S_{21}, are shown in Figure 4-11 as red and blue traces. The transmission s-parameters, S_{34} and S_{43}, from the circuit simulation can be seen as traces in pink and black. Here S_{34} and S_{43} overlay each other. The magnitude of these parameters are plotted in dB versus frequency. All circuit models match VNA measurements well with the best fit coming from the model with capacitance, inductance, and resistance. At around 10 GHz there seems to be a resonance peak that may be attributed to different excited modes of the coaxial cable or the substrate. A low impedance and mostly capacitive reactance were achieved for these wires as desired, again due to the thin 100 nm dielectric. This low impedance creates the

expected result of high transmission loss seen in Figure 4-11 since the low impedance coax differs significantly in magnitude compared to the 50 Ω loads of the VNA. The close fit between model and simulation lends confidence to the electrical parameters gathered from this data. Indeed, for designing power microcoax, we are targeting low impedance lines for power distribution rather than impedance matching to 50 Ω as done for signal microcoax.

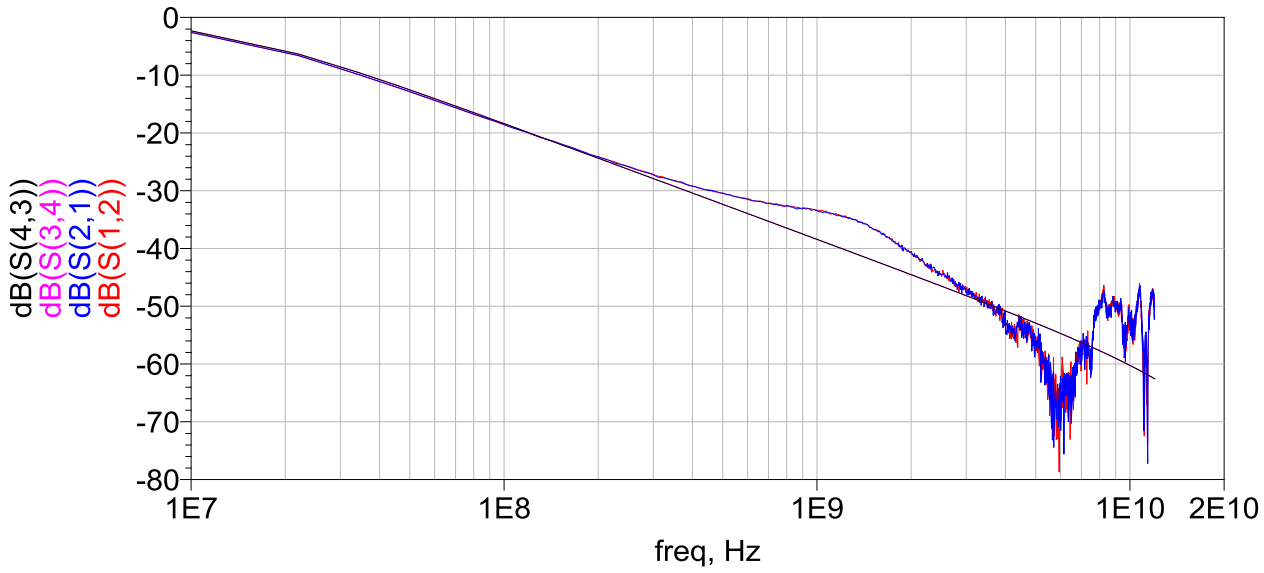


Figure 4-11 Transmission s-parameters from 10 MHz to 12 GHz plotted on a magnitude vs. frequency plot. S-parameters were gathered from VNA measurements of microcoax with 100 nm of HfO_2 dielectric and from a de-embedded circuit simulation with capacitance, inductance, and resistance with de-embedding.

4.5.2 Electrical Results for Low Inductance Parylene Microcoax

The reflection s-parameters for power microcoax fabricated with a thin 1.0 µm parylene C dielectric can be seen in Figure 4-12. As expected, there is a high capacitive reactance at lower frequencies due to the thin 1.0 µm dielectric. However, capacitance is not as high as the wires with thinner HfO_2 dielectric. As seen in the wires with thin HfO_2 dielectric, the s-parameters trend towards the short end of the Smith chart at higher frequencies before gaining inductive reactance. This is desired behavior for power coax. The plot shown in Figure 4-12 corresponds to the fit as a

result of VNA measurements and a circuit model with capacitance, inductance, and resistance components with model based de-embedding.

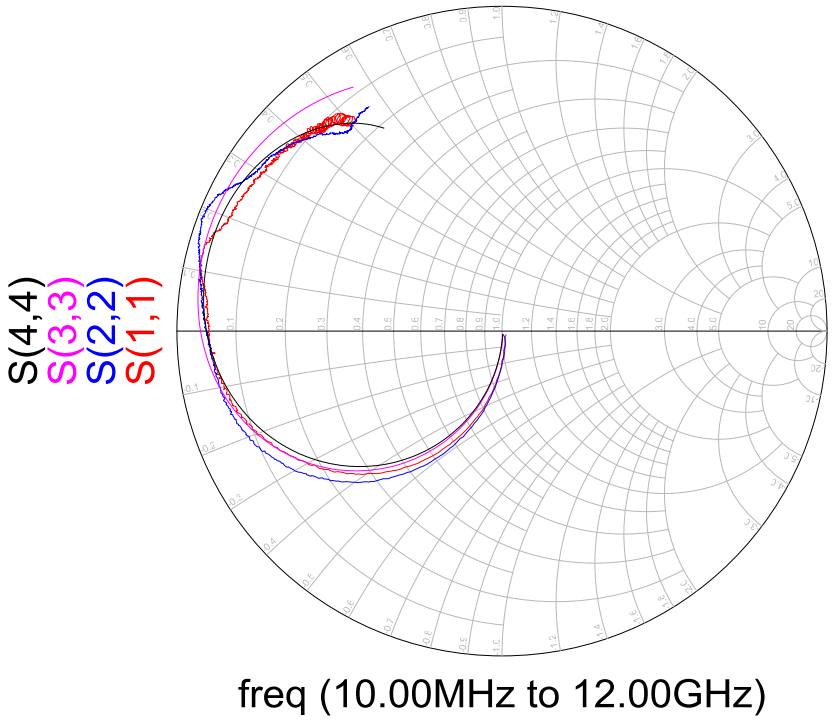


Figure 4-12 Reflection s-parameters from 10 MHz to 12 GHz plotted on a Smith chart. S-parameters were gathered from VNA measurements of microcoax with a 1.0 µm parylene C dielectric and from a de-embedded circuit simulation with capacitance, inductance, and resistance.

The transmission s-parameters for the same microcoax can be seen in Figure 4-13. The magnitude of these parameters are plotted in dB versus frequency. The fit to VNA measurements with circuit modeling is good. As in the wires with HfO_2 dielectric there is a resonance at around 10 GHz. These parylene C coated wires have a thicker dielectric as compared to the HfO_2 wires, resulting in a higher characteristic impedance, closer in magnitude to the 50 Ω loads of the VNA. For this reason, the transmission loss measured in Figure 4-13 is seen to roll off at higher frequencies as compared to Figure 4-11.

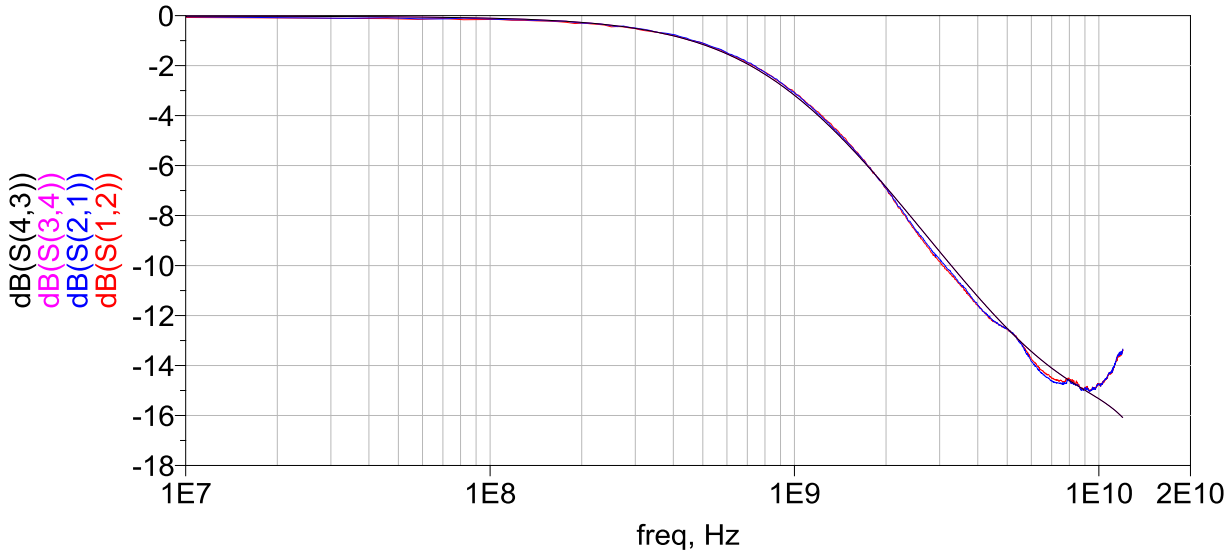


Figure 4-13 Transmission s-parameters from 10 MHz to 12 GHz plotted on a magnitude vs. frequency plot. S-parameters were gathered from VNA measurements of microcoax with a 1.0 µm parylene C dielectric and from a de-embedded circuit simulation with capacitance, inductance, and resistance with de-embedding.

4.5.3 Electrical Results for Signal Parylene Microcoax

Reflection s-parameters for signal microcoax fabricated with 38 µm parylene C and a target impedance of 50 Ω can be seen in Figure 4-14. The best circuit model fit for this set of wires was the transmission line model in ADS. Reflection coefficients from both measured and simulated s-parameters center around the middle (50 Ω point) of the Smith chart indicating the signal is well matched.

The magnitude of the transmission s-parameters are plotted in dB versus frequency in Figure 4-15. Because the signal is well matched, transmission line losses are much lower than the HfO_2 or thin parylene dielectric wires. Reported transmission loss is less than 0.35 dB up to 12 GHz. Transmission loss compares well to results gathered in [11] for a wire with a 15.24 µm core diameter and a parylene C thickness of 22 µm; the wire tested in [11] also had a target impedance of 50 Ω. Transmission loss for a 3.0 mm long wire was reported to be -0.75 dB at 55-90 GHz [11].

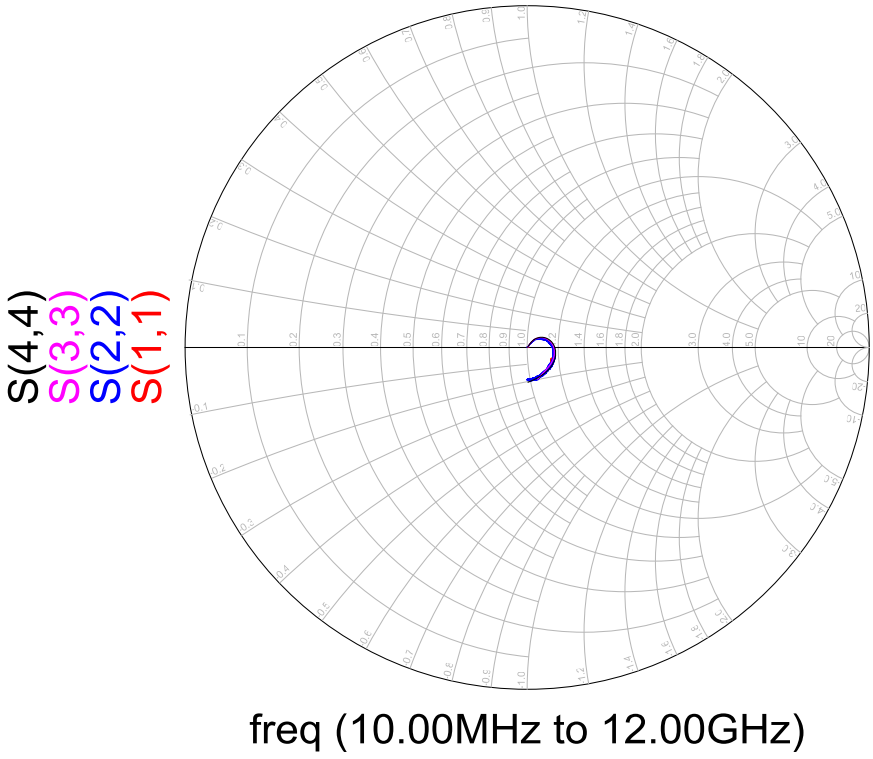


Figure 4-14 Reflection s-parameters from 10 MHz to 12 GHz plotted on a Smith chart. S-parameters were gathered from VNA measurements of microcoax with 38 µm parylene C dielectric and from a de-embedded transmission line model.

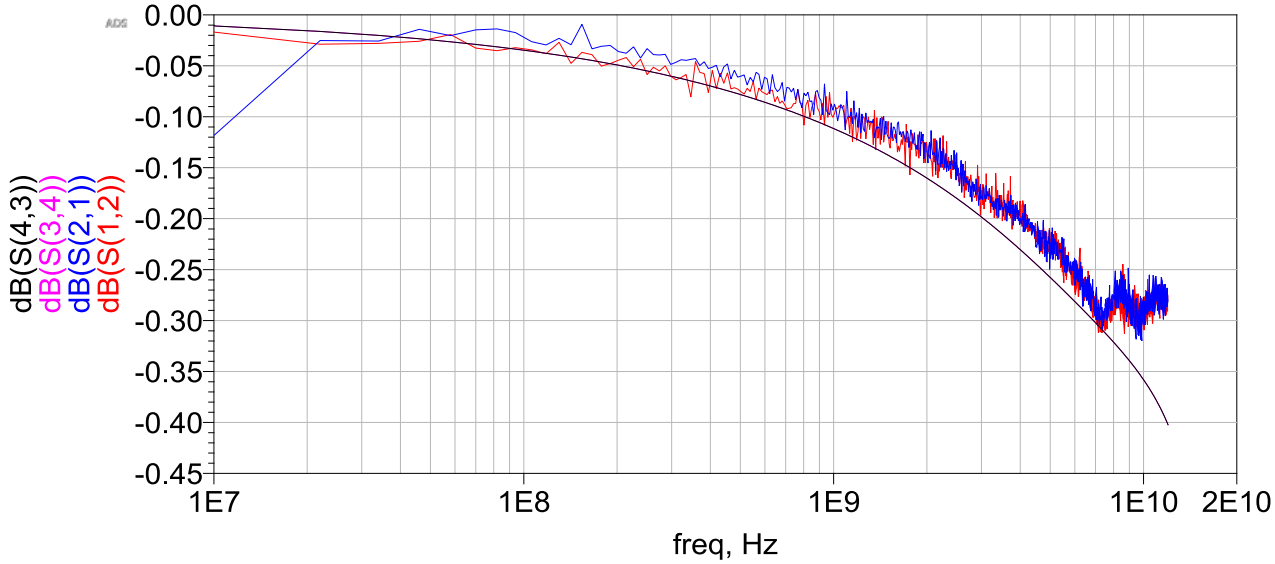


Figure 4-15 Transmission s-parameters from 10 MHz to 12 GHz plotted on a magnitude vs. frequency plot. S-parameters were gathered from VNA measurements of microcoax with 38 µm parylene C dielectric and from a de-embedded transmission line model.

4.5.4 Summary of Electrical Results

Results for wires with 100 nm HfO_2 dielectric are seen in Table 4-2. Average values for capacitance and characteristic impedance without de-embedding are 145 pF/mm and 0.17 Ω respectively. These values compare well to analytical calculations of capacitance and characteristic impedance which were 104-298 pF/mm and 0.07-0.13 Ω respectively. With de-capacitance is 139 pF/mm and characteristic impedance with de-embedding is 0.12 Ω. These fall within the expected range computed analytically. For a set of three wires that were measured, deviation does not exceed ±3.0 pF/mm for capacitance and is less than ±0.005 Ω for characteristic impedance.

Table 4-2 L, C, and Z0 for Power Coax with 100 nm Thick HfO_2 Dielectric for Data Set of 3 Wires

Method	L/l (pH/mm)	C/l (pF/mm)	Z_0 (Ω)
Analytical	1.40-1.70	104-298	0.07-0.13
No De-embedding	214±20 (LM)	145±3.0 (LM)	0.17±0.00 (TL)
Substrate Effects De-embedding	48±56 (LM)	139±3.0 (LM)	0.12±0.00 (TL)

For the same set of wires, results for inductance with and without de-embedding are 48 pH/mm and 214 pH/mm respectively. These results, unlike capacitance and characteristic impedance, show a strong dependence on de-embedding, and are much larger than expected inductance from analytical calculations. Deviation from wire to wire is also high. With de-embedding results deviate wire to wire by 56 pF/mm and without de-embedding results deviate by 20 pF/mm. Measured inductance exceeds analytical predictions by a factor of 30-150. This implies a much stronger effect of the substrate, bonds, and de-embedding on inductance, as compared to the other wire characteristics which may be more heavily influenced by the coaxial cable geometry itself.

Similar observations are made on wires with 1.0 μm of parylene C dielectric. Results are tabulated in Table 4-3. Average measured capacitance with and without de-embedding were 1.50 pF/mm

and 1.80 pF/mm respectively; each with low deviation from wire to wire of less than 0.07 pF/mm for a set of 13 measured wires. These results compare well to analytical calculations for capacitance which were 1.60-2.60 pF/mm. Average measured characteristic impedance also agrees well with analytical results. With and without de-embedding measured characteristic impedance was 4.20 Ω and 3.40 Ω each with deviation less than 0.75 Ω. Analytical characteristic impedance was calculated to be 2.30-3.70 Ω. Inductance for the same set of again measures much higher than analytical predictions, varying over 100 pH/mm compared to analytical results. Measured inductance with and without de-embedding were 97 pH/mm and 223 pH/mm. In each measured case deviation was greater than 15 pH/mm.

Table 4-3 L, C, and Z0 for Power Coax with 1.0 µm Thick Parylene C Dielectric for Data Set of 13 Wires

Method	L/l (pH/mm)	C/l (pF/mm)	Z_0 (Ω)
Analytical	13.6-21.0	1.60-2.60	2.30-2.70
No De-embedding	223±15 (LM)	1.80±0.06 (LM)	3.40±0.10 (TL)
Substrate Effects De-embedding	97±38 (LM)	1.50±0.07 (LM)	4.20±0.75 (TL)

Results for signal wires with 38 µm of parylene C can are presented in Table 4-4. With and without de-embedding the measured average characteristic impedance was 63 Ω and 42 Ω. Deviation was low for a set of nine wires; not exceeding 3.0 Ω. Results for characteristic impedance compare well to analytical calculations, as in the other wires. Analytical predictions were 44-57 Ω.

Table 4-4 Z_0 for Signal Coax with 38 µm Thick Parylene C Dielectric for Data Set of 9 Wires

Method	Z_0 (Ω)
Analytical	44-57
No De-embedding	42±1.0 (TL)
Substrate Effects De-embedding	63±3.0 (TL)

4.6 *Cross-Talk Measurements and Results*

A 4-port vector network analyzer measurement was used to determine the coupled s-parameters of a pair of adjacent microcoaxial cables. These coupled s-parameters give insight on the cross-talk integrity between wires. For each pair of microcoax, those fabricated with HfO_2 dielectric, and thin and thick parylene C dielectric, the measured isolation between pairs was compared to the performance of bare Au wires of the same length and pitch in a ground-signal-ground configuration.. The bare Au wires have a diameter of 25.4 µm and are bonded on the ground and signal pads of four launches on the RF board to mimic GSG interconnects on a multilayered board. An image of this configuration can be seen in Figure 4-16. The wire pitch between bare Au signal wires was 510 µm. The same RF boards with fabricated micro-coax used in two port testing was used for four port testing. Wire pitch between each microcoax was also 510 µm. Wire length in all cases was 3.5 mm.

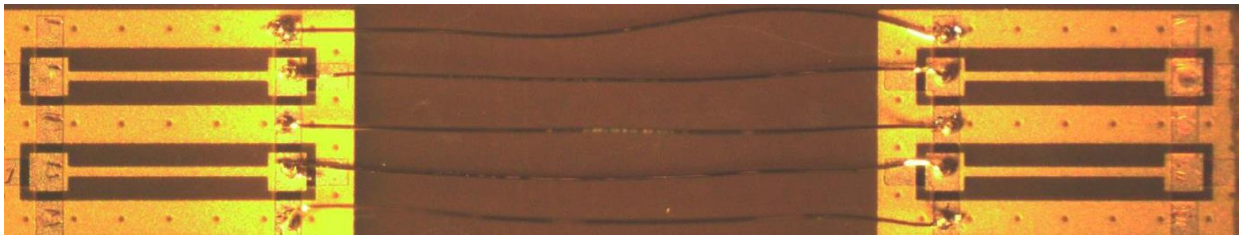


Figure 4-16 Bare Au wires with a 25.4 µm diameter bonded onto GSG pads of four launches. This board is used to compare the cross-talk integrity of microcoax to bare wires.

To probe each pair of wires four sets of GSG probes from GGB Industries with a 250 µm pitch were used to probe onto four individual launches on the RF board. With each launch representing a port from the VNA. The VNA used was an Agilent 4-port VNA (Model 2522A). Voltage was swept from 10 MHz to 26.5 GHz for each pair of coax or each set of bare GSG Au wires.

4.6.1 Cross-Talk Results

The results of coupled transmitted s-parameters, S_{14} and S_{23}, for bare Au wires, microcoax with 100 nm HfO_2, microcoax with 1.0 µm parylene C, and 38 µm parylene C cam be seen in Figure 4-17. The magnitude of S_{14} and S_{23} are plotted in dB versus frequency. Microcoax is seen to have substantially lower cross-talk than bare Au wires at frequencies up to 26.5 GHz due to the metal shield. At 1 GHz, cross-talk between bare wires is -30 dB, whereas for signal coax with 38 µm of parylene C dielectric cross-talk is -62 dB. Some resonance exists at frequencies between 2.0-20 GHz for the bare GSG wires. Resonance around 10-26.5 GHz exists for microcoax. These resonant peaks may be due to excited different modes of the wires or the substrate. Similar cross-talk and resonance of bare wires are seen in [7]. In [7] cross-talk is -20dB at 10 GHz, and worsens to full coupled transmission at 0 dB at 14 GHz for wires 2000 µm long. The cross-talk tests in [11] were done on 17.78 µm diameter core wires with 18 µm of parylene C dielectric fabricated to target a 40 Ω impedance. Cross-talk was reported to be -40 dB above 25 GHz for adjacent wires with a 160 µm wire pitch. Wires were 3000 µm long. Results in [11] are very comparable to results seen in this work.

Cross-talk for power-coax with thin 100 nm HfO_2 dielectric and thin 1.0 µm is also reported to be lower than that of bare wires. However, because the wires have a lower magnitude of characteristic impedance compared to the 50 Ω loads on the VNA, cross-talk may be low because power coax has lower transmission in this testing configuration. For the 1.0 µm of Parylene C transmission at 1 GHz is -3dB as indicated in Figure 4-13. This transmission loss is not low enough to prevent the cable from having some transmission, as a result the cross-talk shown in Figure 4-17 may be attributed to the wires. Cross-talk is lower than that of bare wires at -50 dB. For the wires with 100 nm HfO_2 dielectric transmission is low at -40 dB at 1 GHz as shown in Figure 4-11. Thus, the

transmission through the HfO_2 wires for the cross-talk test may be so low that the reported cross-talk value of - 82 dB may only be attributed to the substrate.

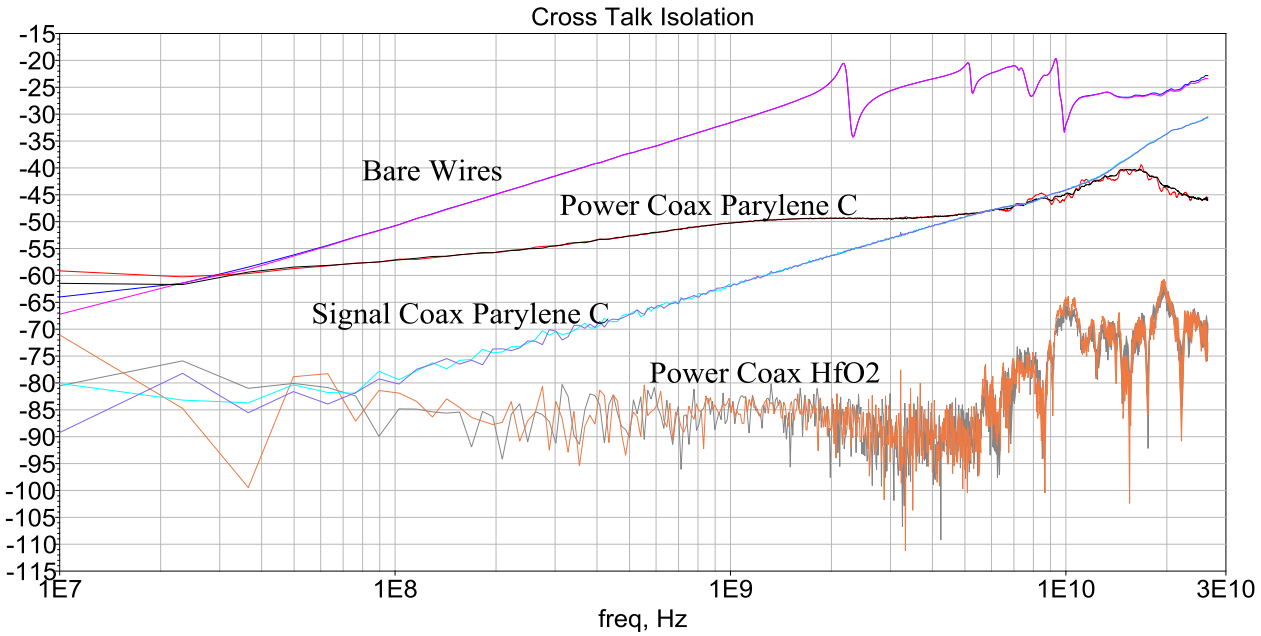


Figure 4-17 Magnitude of S_{14} and S_{23} in dB plotted versus frequency up to 26.5 GHz for adjacent wires. Improvement in isolation is seen with wires that have a coaxial shield.

4.7 *Conclusions*

We have fabricated and characterized low impedance and signal microcoaxial cables that could be used in lithography-free microelectronic interconnects. This is the first demonstration in the literature of which we are aware of low impedance microcoax for power distribution. We have found that ALD and vapor coated dielectrics are conformal when inspecting FIB cross sections; additionally, fixturing influences how conformal sputtered films are. A sputtered adhesion and seed film is preferred over an evaporated film for achieving a conformal electroplated shield. From cross sections, film thickness measurements, and estimations of dielectric properties, it is possible to calculate the electrical properties of microcoaxial cables. We have found good agreement for

analytical calculations of capacitance and characteristic impedance with VNA measurements and circuit simulations; however, calculating inductance proves to be challenging. It appears likely that inductance is more heavily influenced by the substrate and ball bonds in ways that are challenging to model.

From RF results with and without de-embedding, we conclude that the capacitance of the substrate is small compared to the capacitance of microcoax. For wires made with 100 nm of HfO2 dielectric and 1.0 µm parylene C dielectric the difference in average capacitance with and without de-embedding was 6.0 pF/mm and 0.30 pF/mm respectively. The inductance of the substrate, however, may prove to be comparable to microcoax. Differences in inductance with and without de-embedding were ~150 pH/mm for wires with HfO2 dielectric and ~120 pH/mm for wires with 1.0 µm parylene C. This difference in inductance is also seen in measurements of characteristic impedance for signal coax. The difference in characteristic impedance with and without de-embedding was 20 Ω.

Additionally, we have also shown that microcoax is better isolated to adjacent wires compared to bare Au wires. At 1 GHz cross-talk for bare Au wires is -32 dB, whereas cross-talk for signal micro coax with a 38 µm dielectric is -62 dB. At 1 GHz transmission loss for power coax with 1.0 µm of parylene C dielectric is -3 dB. This shows that there is enough transmission throughout the cable for cross-talk to exist. In fact, at 1 GHz cross-talk for power coax with 1.0 µm dielectric is -50 dB; about 18 dB lower than cross-talk for bare Au wires. At 1 GHz transmission loss for power coax with 100 nm HfO_2 dielectric is -40 dB. This loss is sufficient for there to be little to no transmission throughout the HfO_2 during the cross-talk test. As a result cross-talk reported in Figure 4-17 is

most likely due to cross-talk of the substrate which is low at -82 dB at 1 GHz. Overall, there is an advantage of using micro-coaxial shields as it lowers cross-talk compared to standard wires as desired. We have also shown in both the 2 Port and 4 Port RF tests that we have achieved significantly lower impedances, compared to a 50 Ω standard, that is desired for power distribution, achieved using thin dielectric coax.

4.8 *Future Work*

Inductance may be better measured by improving circuit simulations. Better modeling iterations of the substrate may improve de-embedding by investigating its contributions to inductance. Measuring the substrate directly still proves to be challenging, but better control of fabrication and masking probing locations of the board may help to improve access for direct de-embedding. Electromagnetic simulations of the board is another outlet to investigating substrate effects. Additionally, modeling other inductance effects such as the inductance of the ball bond and wedge bond joints may improve circuit simulations. Other improvements include modeling the wire with discrete elements rather than lumped components. Further analysis on these substrate effects will also allow us to gather insight on the different resonances that have been observed at higher frequencies than 10 GHz.

5 Conclusions and Future Work

In this chapter I will highlight in more detail some of the major conclusions found in this work. I will refrain from repeating too much text from the conclusions in Chapter 3 and Chapter 4. I will also highlight in each section future work that can be used to improve results.

5.1 *PDN*

A PDN model is key to determining microcoaxial geometry for power distribution. In Chapter 3 the PDN model used was a simplified model. Future work should be spent on adding more components to a PDN. The electrical contributions from package leads, substrates, or attachment points may add electrical resonance that will limit impedance requirements further. A critical feature in PDN design as described in [21] [39] is the Bandini Mountain. It is a peak resonance formed by the package lead inductance, and can be a challenge for PDN designers.

5.2 *Inductance and Resistance*

Inductance and resistance are major contributors to impedance in a PDN. Inductance should be limited as much as possible as it introduces resonances at higher frequencies that will bring the system above necessary power requirements. For microcoax one of the most effective methods to lowering inductance is minimizing dielectric thickness. One topic not explored in detail in this thesis is the frequency dependence of resistance and inductance. Future work should be spent on characterizing dielectric and conductive losses and its effects on resistance and inductance. Some parameters for loss gathered from transmission line modeling can be seen in Appendix A. These parameters were also variables during fitting and are a first attempt at characterizing dielectric and conductive loss. Also included in this thesis are frequency dependent equations for resistance and inductance derived from [23]. They can be seen in Appendix B. These skin effects will either limit

bandwidth performance, or limit impedance requirements further. At high frequencies (>1 GHz) resistance can triple, as shown in Appendix B, due to the skin effect.

5.3 *Microcoax Fabrication*

Vapor coatings and ALD are great films for creating microcoax with very thin or thick dielectrics. It is worth considering CVD metal coatings to see how conformal they are compared to sputtering. A conformal metal adhesion layer is key to a conformal shield. Shown in Appendix C is an image of an asymmetric shield due to an asymmetric adhesion layer formed via thermal evaporation. Sputtering can be nearly conformal but requires at least two runs or proper fixturing. It may be possible to incorporate a fixture within the stage rotation mechanism of a sputter tool to rotate the wires during the process.

In addition to a conformal metal coating, the quality of the adhesion layer will affect the quality of electroplated metal. Good control of the electroplating bath is necessary. In this work I did note some film quality variation from board to board as shown in Appendix D. Shield quality may affect the electrical properties and cross-talk of microcoax. This is largely due to the dependence of resistance on the resistivity of both the core and shield conductors and the effect of resistivity on the magnetic fields produced by the wires [26]. A future experiment may include further characterization of fabrication methods to metal film quality and dielectric film quality.

Another challenge in fabrication was masking or laser etching dielectric material. For the thin dielectrics it was possible to mask the probing locations with polyimide tape, but for the thicker dielectrics this was more difficult, as shown in Appendix E. A solution to this was to mask only the adhesion layer and plated metal after depositing dielectric with polyimide tape and laser etching

the thick parylene to expose GSG pads after fabrication. However, one issue with laser etching thicker dielectrics is redeposition of material onto the surface as well as poor heat conduction through the dielectric and poor heat spreading due to the high laser intensity. For the thicker dielectrics this was indicated by black residue as shown in Appendix F. The thick dielectrics required a higher number of pulses (>400) at a power of 0.22 W which is enough to cause localized heating of the dielectric. Because the thick Parylene C dielectric is a polymer it has a poor thermal conductivity, in both the transverse and lateral directions, and thus more prone to overheating. There are existing methods to clean this residue but it can be damaging to the board as most methods require solvent cleaning or ablating residue from the surface. It is worth optimizing laser parameters further to reduce damage and investigate cleaning techniques for this process.

5.4 *De-Embedding*

De-embedding was a major challenge to the study in chapter 4. For the in-situ fabrication process masking material from depositing on any other surfaces other than the wire was difficult. This added material altered substrate properties. Typically the s-parameters of the RF test fixture are measured before fabrication or attachment and later used to de-embed the substrate from the device under test. However, the board before and after this in-situ process has different properties.

One solution may be to measure the substrate s-parameters by removing the wires, after measuring their s-parameters with the board, and re-measuring with the board only. An advantage to this is that the effects of the board can be better studied and compared to ADS models of the substrate as shown in Chapter 4. The one issue of this , and the reason it was not done in this thesis, is that this process is destructive to the wires. Another solution may be to compare those measurements or ADS circuit models to electromagnetic simulations of the substrate. Substrate models of this in-

situ process can be seen in [11]. One thing that was noted in [11] via electromagnetic simulations was that adding more grounded locations along the surfaces of the substrate improved performance.

Unfortunately we did not have time to run electromagnetic simulations otherwise these simulations would have been a nice comparison to make to my circuit models. Ultimately de-embedding is necessary to report on microcoaxial properties, but studying the effects of the substrate and added material may be key to understanding how the entire system effects performance.

5.5 *VNA*

Taking VNA measurements was a central part of this thesis. I have a few recommendations for future use of a VNA probe station. Probing can vary from person to person as it is very sensitive to how you land probes onto the substrate. Being consistent is key. I tend to calibrate (using a SOLT calibration substrate) each time I approach the VNA, in some cases the calibration needs to be done multiple times, test as many wires as possible, and take note of the date the measurements and calibration was made. Calibration substrates can degrade in performance over time. This will affect your measurements from the first day you used the substrate compared to subsequent days. It is worth tracking performance by date and noting the quality of the calibration board. To insure you have a good calibration you can always probe for example onto a "short" on the calibration substrate and see if it aligns on the left hand of the Smith chart.

The wires that lead from the probes to the VNA as well as their connectors can also effect performance. Short length wires, short distance of the VNA from the device under test, and probe quality can improve results and make calibration easier. Poor experiment set up can introduce

unwanted resonances at high frequencies. Another thing to note are some connectors are better used for certain frequency sweeps. SMA connectors are best up to 26.5 GHz while K-connectors are best for going to higher frequencies up to 40-50 GHz [6]. Additionally, I did not used an average voltage sweep. I only used a linear sweep with IF bandwidth of 10 kHz. It would be worth studying in more detail the effects of averaging or other VNA capabilities.

5.6 *ADS Modeling*

Future modeling work for the study introduced in Chapter 4 would be to compare those lumped component circuit models to the quasi-distributed model in Chapter 3. For transmission line modeling and for the substrate models , limiting the number of variables is key. Often times there were too many variables during optimization. This is another reason why direct measurement of the substrate can be helpful, as well as electromagnetic simulations.

5.7 *Transmission Line Theory*

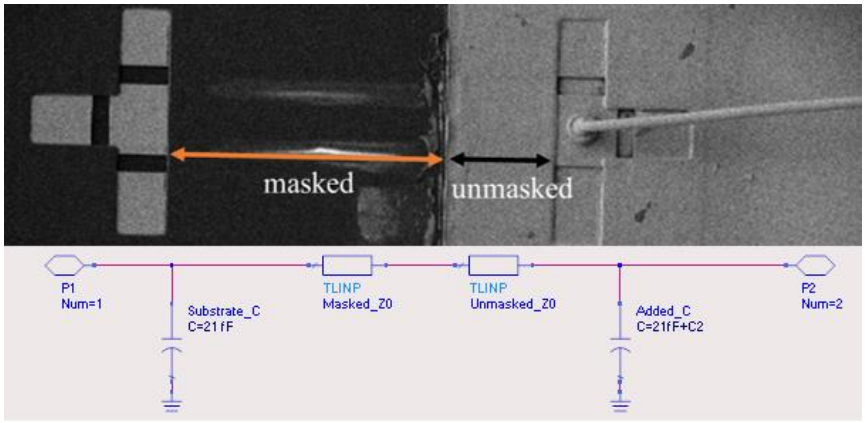
Another topic I did not consider until later in my studies are the varying modes of a coaxial transmission line. The primary mode of interest is the Transverse Electro-Magnetic Mode of a cable. This mode assumes that the electric and magnetic fields are orthogonal to each other [6]. In the TEM mode characteristic impedance is constant over a wide band of frequencies, however, at higher frequencies other modes may be excited within the cable and may alter electrical performance. Future work should include a modal analysis to determine at which frequency bands these wires perform under a TEM mode.

Appendix

A – ADS Transmission Line Model Fit Parameters

"Sub"- represents the substrate
"Masked" – represents the masked area of the substrate
"Unmasked" – represents the exposed substrate areas to added material
"K " – represents the effective dielectric constant of the substrate or coax
"A" – represents the attenuation constant in Nepers/m (conductive loss due to skin effect) of the substrate or coax
"TandD" – Loss tangent of dielectric in Nepers/m (dielectric loss) of the substrate or coax

Substrate Model



TLM Parameters Gathered from Wires

Board	Z_0 Coax (Ω)	K Coax	A Coax	TanD Coax	Z_0 Masked Sub (Ω)	K Masked Sub	A Masked Sub	TanD Masked Sub	Z_0 unmasked Sub (Ω)	K unmasked Sub	A unmasked Sub	TanD unmasked Sub	Notes
Power Parylene (MMS003)	4.21	3.80	236.3	0.0005	53.60	4.22	5.46	0.3462	51.07	8.21	306.16	0.0384	All values Avg out of 13 Wires
Power HfO2 (MMS004)	0.120	20.82	0.2	0.1	42.18	5.27	40.8	0.2333	49.59	5.92	19	0	All values Avg out of 3 Wires
Signal Parylene (MMS007)	63.2	2.69	11.8	0.0005	91.83	1.61	7.19	0.0409	61.60	3.25	22.30	0.0039	All values Avg out of 9 Wires

B – Frequency dependence of R and L

Parameter	Value	Units
r_c	Core Radius	m
t_d	Dielectric thickness	m
t_s	Shield thickness	
ρ_c	Core Resistivity	Ωm
ρ_s	Shield Resistivity	Ωm
μ_0	Magnetic Permittivity Free Space = $4\pi \cdot 10^{-7}$	H/m
μ_r	Magnetic Permittivity Constant = 1	
ε_0	Electric Permittivity Free Space = $8.85 \cdot 10^{-12}$	F/m
ε_r	Dielectric Constant	
f	Frequency	Hz
σ_c	Core Conductivity	S/m
σ_s	Shield Conductivity	S/m
ℓ_{wire}	Wire Length	m

Resistance at DC contributions of core and shield:

$$\frac{R_{low\_freq}}{l} = \frac{R_{core}}{l} + \frac{R_{shield}}{l} = \frac{\rho_c}{\pi r_c^2} + \frac{\rho_s}{\pi \left[(r_c + t_d + t_s)^2 - (r_c + t_d)^2 \right]}$$

Resistance at high frequency with skin effect onset:

$$\frac{R_{high\_freq}}{l} = \frac{R_{core}}{l} + \frac{R_{shield}}{l} = \frac{1}{2\pi r_c}\sqrt{\frac{\pi f \mu_0}{\sigma_c}} + \frac{1}{2\pi (r_c + t_d)}\sqrt{\frac{\pi f \mu_0}{\sigma_s}}$$

Inductance due to magnetic field within conductor (L_{core} and L_{Shield}) and between conductors ($L_{external}$):

$$\frac{L}{l_{wire}} = \frac{L_{External}}{l_{wire}} + \frac{L_{core}}{l_{wire}} + \frac{L_{shield}}{l_{wire}}$$

$$\frac{L_{core}}{l_{wire}} = \frac{\mu_0}{8\pi}$$

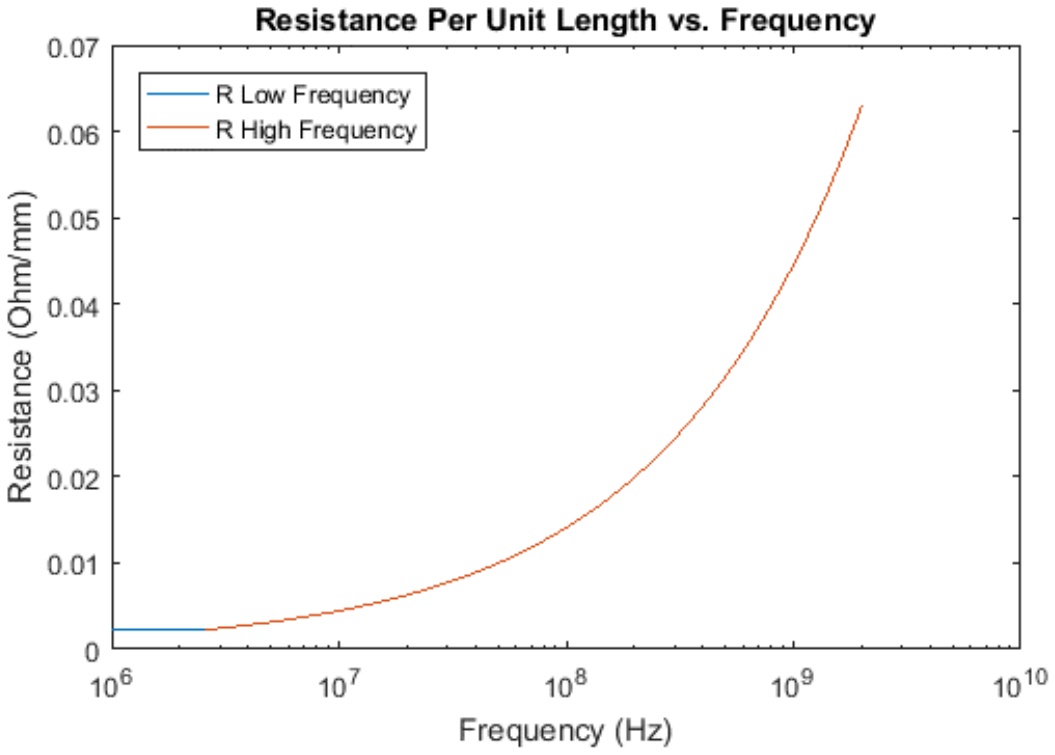
$$\frac{L_{shield}}{\ell_{wire}} = \frac{\mu_0}{8\pi}\left[\frac{(r_c + t_d + t_s)^4 \ln\left(\frac{r_c + t_d + t_s}{r_c + t_d}\right) - (r_c + t_d + t_s)^2\left[(r_c + t_d + t_s)^2 - (r_c + t_d)^2\right] + \frac{1}{4}\left[(r_c + t_d + t_s)^4 - (r_c + t_d)^4\right]}{\left[(r_c + t_d + t_s)^2 - (r_c + t_d)^2\right]^2}\right]$$

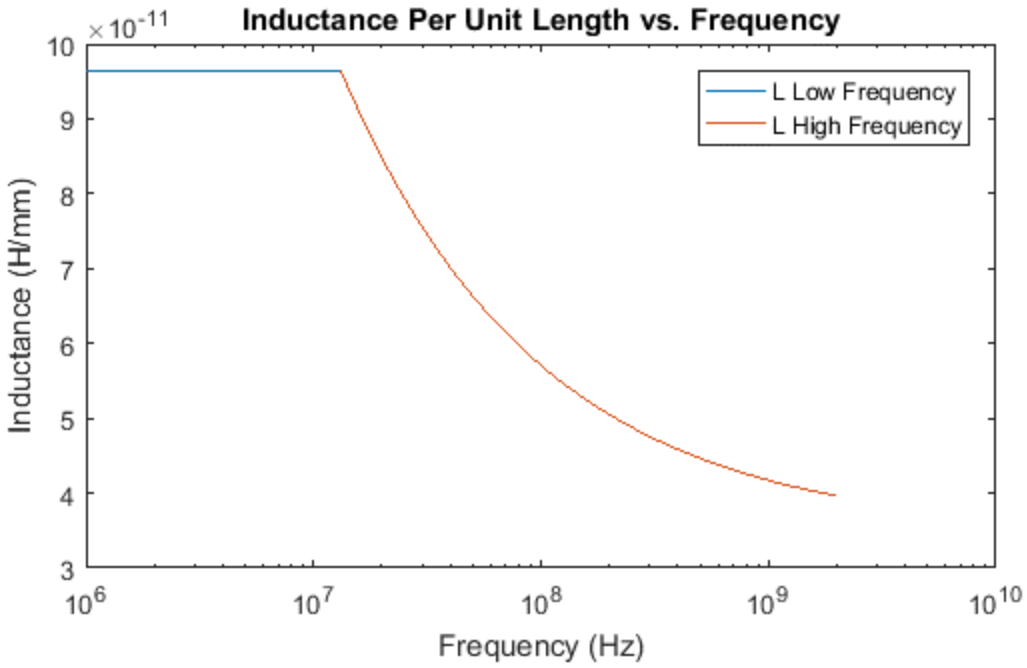
$$\frac{L_{External}}{\ell_{wire}} = \frac{\mu_0}{2\pi}\ln\left(\frac{r_{core} + t_d}{r_{core}}\right)$$

Inductance due to skin effect. L_{core} and L_{shield} approach zero at higher frequencies as current is driven to the surface of the conductor thus minimizing the magnetic field within the conductor. $L_{external}$ remains the same:

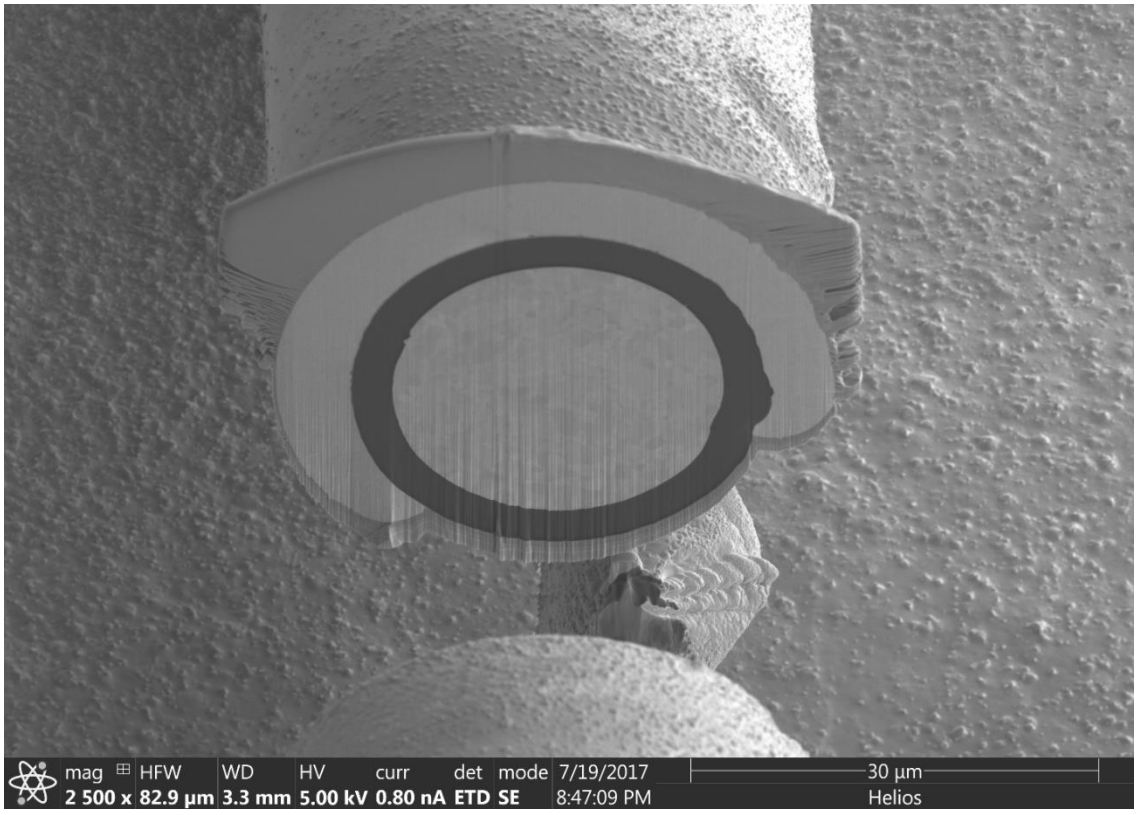
$$\frac{L_{core}}{\ell_{wire}} = \frac{\sqrt{\mu_0}}{2\pi r_{core}\sqrt{4\pi f \sigma_{core}}}$$

$$\frac{L_{shield}}{\ell_{wire}} = \frac{\sqrt{\mu_0}}{2\pi (r_c + t_d)\sqrt{4\pi f \sigma_{shield}}}$$

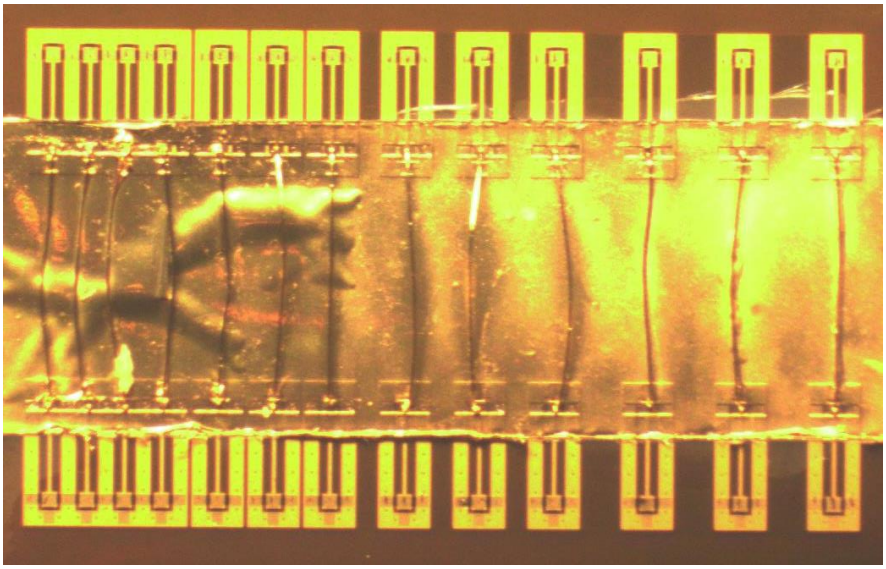


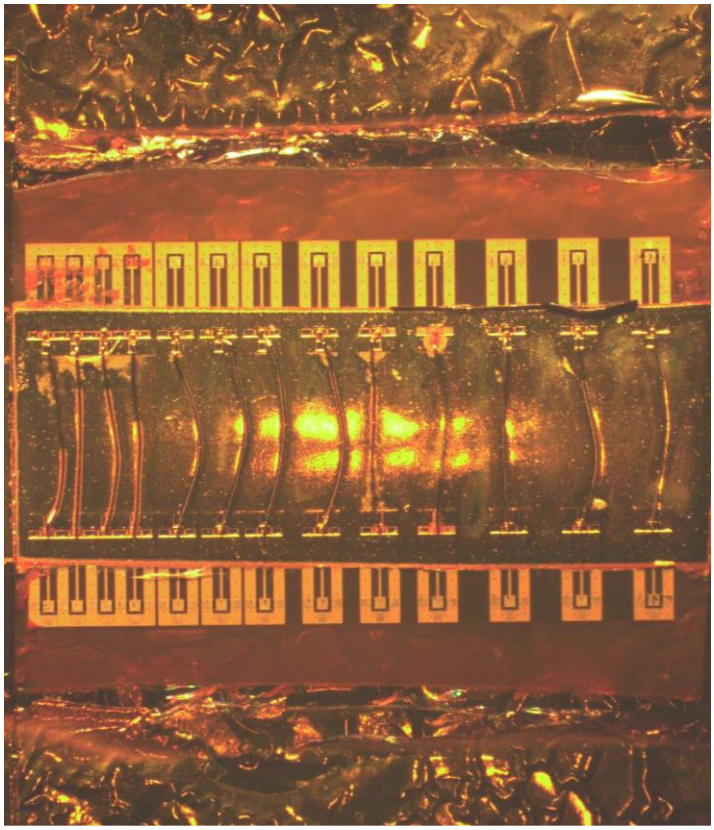


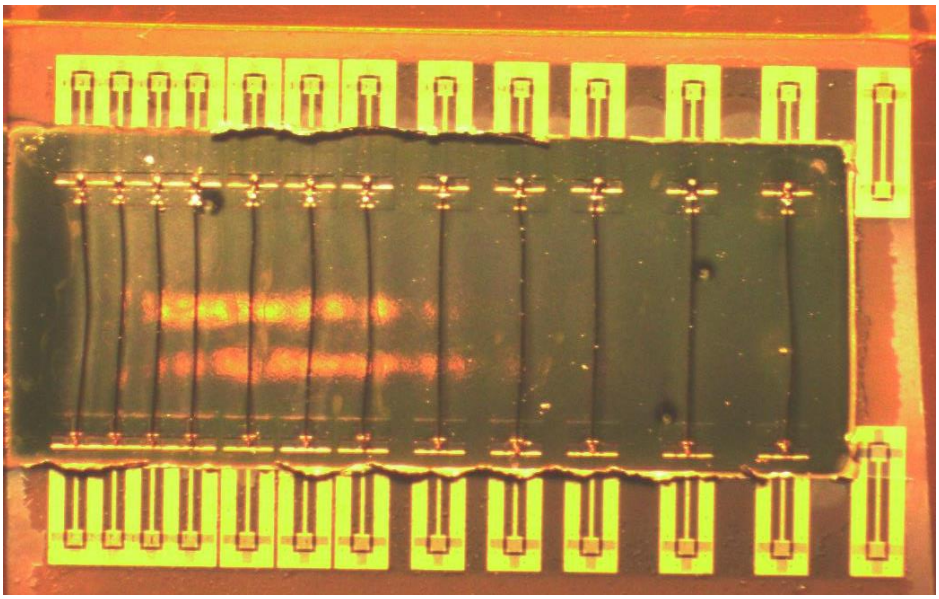
C – FIB with 25.4 µm diameter core, 3.0 µm Parylene C dielectric, Evaporated Ti/Cu (30nm/150nm) Seed Layer, and 5.0 µm of Au plated metal.



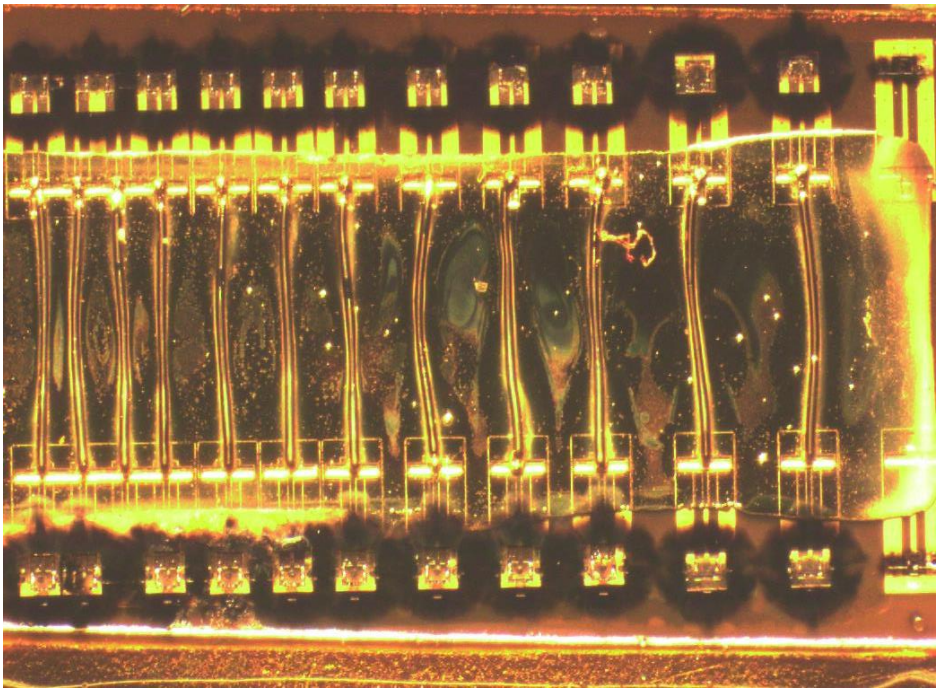
D – Variation in Au plating Quality on Different RF Boards







E- Laser Etching of Thick Dielectric to Access GSG Probe Locations



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