Development of LED Driver Circuit Architectures for Future Generation Visible Smart Lighting Networks, Combining High-Speed Data Communication and Illumination Control

A dissertation submitted by

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Advisor: Prof. Valencia Joyner Koomson

For my parents

Abstract

With the development of semiconductor-based light generated by light-emitting diodes (LEDs), the second generation of lighting known as solid state lighting (SSL) has been shown to provide greater energy efficiency compared to the conventional incandescent light bulb. The vision for SSL technology is to attain the full potential of light by capitalizing on energy efficiency, long lifetime, and improved sustainability. The light modulation capability of LEDs has produced considerable interest in the use of solid-state illumination systems for data communication. Visible light communication (VLC) has a number of unique advantages from ecological and human health perspectives; and the optical range is free from regulation, resulting in high data rate channels. Dual-purpose indoor LED lighting systems providing illumination control and data communication requires novel LED driver circuit architectures to realize the plethora of VLC-based applications envisioned for future lighting networks. This thesis presents research on novel driver circuit architectures for VLC applications. The driver circuit architecture presented in this work overcomes the modulation bandwidth limitation by providing a feedback control loop to maintain the DC-DC converter output voltage independently of the LED drive signal to control data modulation and dimming. The main challenge of implementing a fast link in VLC networks is emanated from the inherent bandwidth limitations of LEDs. In this work the conventional methods of extending the bandwidth of LED drivers are reviewed and proposed topologies are introduced. Seven distinct methodologies of negative impedance converter (NIC), equalization techniques, pulse shaping, peaking, pole-zero cancellation, time-interleaved LEDs, and 16-level PAM are presented. The concept of NIC is reviewed and two different modes of

fixed and floating structures with their corresponding proposed LED drivers are introduced. Pre- and post-equalization techniques are analyzed such as multiple resonant, and active and passive equalizations are methods, which compensate the roll-off in the transfer function of raw-LED, leading to bandwidth extension. An LED driver based on a pulse shaping circuit topology is presented which enhances the overall bandwidth of the VLC link by shortening the rise and fall times. The next method for bandwidth enhancement is peaking. Different peaking techniques such as shunt, series, (bridged) shunt-series and triple resonant peaking techniques are reviewed and a new technique called bridged-shunt-zero peaking is proposed. A peaking technique called bridged-shunt-zero peaking is presented in this work, which is suitable for incorporation into the LED driver circuit design. An LED driver with enhanced bandwidth using the pole-zero cancellation methodology is presented to overcome the inherent bandwidth limitation of LED device. Time-interleaved LEDs is yet another trend in compensating the low bandwidth of LEDs. In this method each binary input is sent with a fixed delay and it can be detected by processing the received signals. Finally, an LED driver that implements 16-level PAM signaling using a 4 x 4 array of LEDs is described, yielding an increase in the data transmission rate by 4 times.

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Chapter 1

Introduction

1.1 Motivation

Electrical lighting has revolutionized society over the last century, and today electrical lighting is on the verge of yet another revolution. Energy bills legislation, introduced in 2007 by Congress, has banned the use of incandescent light bulb by the year 2014 [1]. With the development of semiconductor-based light generated by light-emitting diodes (LEDs), the second generation of lighting known as solid state lighting (SSL) has been shown to provide greater energy efficiency compared to the conventional incandescent light bulb. SSL technology has shown great promise in providing multiple benefits such as improved health and safety to the society, energy efficiency, and improved productivity. This lighting technology evolution has not only proven to be a suitable replacement for incandescent light bulbs, but has also provided enhancements in each beneficial area while establishing the prominent core competencies for this new age of lighting. The full potential of SSL technology, however, has not yet been fully achieved. The SSL technologys vision has been to ultimately attain the full potential of light by capitalizing on energy efficiency and improve sustainability.

The white LED stands at the threshold of a new era of energy-efficient lighting bringing revolutionary advances in the use of light for illumination and a host of other applications, including sensing, navigation, and communications.

With the increasing global demand for anywhere, anytime connectivity to mobile devices, there is a growing need to develop wireless access technologies that are broadband, interference-resistant, reliable, and cost-effective [2]. The major step towards the vision of ubiquitous wireless connectivity and the development of green, environmentally-friendly wireless networks is using white LEDs. We have witnessed the tremendous capacity provided by optical signals in telecommunications networks and the emergence of the white LED presents an opportunity to extend the reach of optical signals in free-space. This vision leads to a special case of optical wireless which is called visible light communication (VLC), where an additional advantage lies in simultaneous use of light sources as illumination and communication. The realization of visible light networks combining both illumination control and high-speed wireless connectivity to computers, peripheral components, and mobile devices presents a number of new challenges at all levels of system development. One of the grand challenges is bidirectional/uplink transmission in a visible light network. Hybrid RF/LED program considers the growing interest in hybrid communication systems as a viable system topology for indoor visible light communication [3]. A hybrid system combines the advantages of unlimited bandwidth free - space optical (FSO) signaling and high mobility RF wireless transmission to extend the bandwidth, reduce power consumption, lower cost, and provide high adaptability to dynamic operational environment. For indoor visible light communication, a combined hybrid RF/LED link improves reliability and bit error rate performance; and provides greater immunity to blocking. To capitalize on large - scale energy savings of solid-state lighting, hybrid system realization requires advanced integration and packaging techniques that take advantage of low - cost, commodity silicon micro-fabrication processing (CMOS) which has been advanced over the past decades. Furthermore, novel approaches to device integration are necessary to account for several order dimensional discrepancy between antenna geometries measured in millimeters at microwaves and typical submillimeter dimensions of active optical components.

Here we have presented the concurrent combination of data signals with dimming control signals. Two methods of digital and analog generation of PWM signals and its combination with data signals in $0.5\mu m$ and $180nm$ CMOS technology are developed, respectively. The main challenge of implementing a fast link in VLC networks is emanated from the inherent bandwidth limitations of LEDs. The typical 3dB frequency bandwidth of white LEDs is in the range of 5-12MHz. To alleviate this challenge a number of bandwidth enhancement techniques are proposed, designed, and manufactured. The first one is called negative impedance converter (NIC) which generates a negative capacitance used to cancel out the parasitic capacitance of LED and hence increase the overall bandwidth. Then different equalization methods are reviewed and pulse shaping circuit which increases the bandwidth by shaping the LED current signal to have smaller rise and fall times is presented. The other method is the high speed design using peaking and equalization techniques where it enhances the overall bandwidth by generating peaking in the frequency response. The next method covered here is the pole-zero cancellation and can be applied to both digital and analog modulation techniques. After that, the time interleaved technique is introduced which is a mechanism of sending data with some fixed delays in order to increase the total number of bits per second. Finally, the pulse amplitude modulation which uses 16-level resolution is presented; 16-level PAM is capable of increasing the data rate by four times.

1.2 Thesis Organization

Chapter 2 provides an introduction to the visible light communication networks, and its analysis. It also takes a look at the LED as a source and discuss its transient and frequency behavior.

Chapter 3 focuses on the conventional LED driver circuit architectures. Amplitude and PWM driving modes are reviewed and then Linear as well as the switching regulators for implementing in LED drivers are discussed in this chapter.

Chapter 4 presents a novel LED driver circuit architecture design enabling concurrent data transmission and dimming control for VLC. It introduces a digitally-controlled bi-level LED driver analysis and design. In addition, it introduces the digital combination of data signals with dimming controls generated using the analog dimming signal. It also contains the discussion of design and implementation of a novel two-stage OTA designed to be used in the feedback loop control of the LED driver.

Chapter 5 covers novel and distinct types of bandwidth enhancement techniques which composed of negative impedance converter, high speed design using equalization, pulse shaping circuit, peaking, pole-zero cancellation, time interleaved LEDs, and 16-level pulse amplitude modulation.

Chapter 6 presents the experimental demonstrations developed to prove the concept of the VLC system design. The transmission of digital signals using the software defined rasio (SDR) setup, and transmission of OFDM analog signals using the MATLAB/Simulink setup are explained in this chapter.

Chapter 7 summarizes and concludes the contribution of this thesis. Future work that would further enhance the bandwidth of the system are also suggested.

Chapter 2

Visible Light Communication using White LEDs

2.1 Introduction

LED is more advantageous than the existing light sources like incandescent in terms of long life expectancy, high tolerance to humidity, low power consumption, and minimal heat generation lighting. White light can be generated by mixing three primary colors of red, green and blue. The other way is combination of blue LED with the coating of phosphorus. This white LED is considered as a strong candidate for the future lighting technology. Compared with conventional lighting methods, white LED has lower power consumption and lower voltage, longer lifetime, smaller size, and cooler operation. Even though the LED entitles the aforementioned features, this device put some restrictions in terms of its inherent bandwidth. LED devices have inherent bandwidth limitations which limit data transmission speeds in future visible light communication networks. In this chapter first we review the VLC system and its analysis. And then the LEDs, which are going to be used in this VLC system for translating the modulation and illumination control signals into the light are reviewed in terms of its transient and frequency response.

2.2 Visible Light Communication (VLC)

Visible light communications (VLC) is the latest optical wireless communications technologies that uses low-power light emitting diodes, or LEDs, not only to provide light but also to broadcast data. LEDs are extremely energy-efficient and predicted to become widespread in general lighting application. Because LED is a solid-state lighting device, it can be modulated at high-speed compared with other lighting sources. VLC uses LEDs, which send data by flashing light at speeds undetectable to the human eye. It is expected that LED market will reach $29 billion in 2017 that is comparable to today's NAND and DRAM markets [4]. The pioneer of VLC using LEDs is Professor Masao Nakagawa of Keio University. His first paper on this subject appeared in the early 2000, together with his successor Prof. Shinichiro Haruyama [5]. Later in 2003, he formed Visible Light Communication Consortium (VLCC).

Widespread use of LEDs in traffic applications and growing interest in intelligent transport system (ITS) presents an opportunity for VLC. In 2006 Siemens launched VLC project. Later in 2008, European Commission established OMEGA project with a consortium of 20 European partners from industry and the scientific community. Meanwhile, in 2008, the US national science foundation (NSF) has approved a grant of $18.5 million to help establish and the engineering research center (ERC) focuses on VLC. The members of the center include the Rensselaer Polytechnic Institute (RPI), Boston University (BU) and the University of New Mexico (UNM). The University of California also have launched five-year research project starting from 2009, called the Ubiquitous Communication by Light (UC-Light) that is founded with $3.5 million from the University [4]. VLC is in the process of standardization by the IEEE 802.15 TG7 and VLCC as well as other standard organizations.

The IEEE 802.15.7 standard was approved to define PHY and MAC layer protocols for short-range free-space optical communication using visible light. As a result of concurrent illumination control and data transmission within a visible light network, luminaires will be able to wirelessly communicate with each other and coordinate their appropriate functionality. The light will also be able to deliver data to mobile users, without relying on increasingly congested radio frequency (RF) wireless channels. Recent advancements in biochemical sensing, will enable the network to monitor biohazardous materials, and when appropriate, destroy the biohazards by activating deep ultra-violet (UV) LEDs. Moreover, even with these advanced capabilities, the VLCs smart lighting has substantiated its utilization to be more energy-efficient than current lighting systems by combining more efficient, properly designed, color-tunable LED systems with advanced adaptive control networks. The energy conserved from smart lighting, according to the electrical energy savings forecast by the department of energy (DOE), will be doubled by the use of white LED systems. The additional electrical energy savings is roughly equivalent to the elimination of over 300 coal-fired power plants accompanied by large reduction in greenhouse gas emissions. VLC offers several potential advantages over RF communications. It can provide more secure communications over a shorter range because walls and curtains can easily block light signals, whereas potential eavesdroppers can easily detect RF signals from outside buildings. The technology could be useful in factories and hospitals, in which radio transmissions are either impossible or limited owing to concerns about RF interference with critical equipment. The new technology's main limitation is that it is primarily envisioned as one-way broadcast technology. Bidirectional communications would have to occur over a different technology such as Wi-Fi. Several efforts are under way to develop VLC standards. In the next section the analysis of VLC system is described.

2.3 Fundamental Analysis for VLC

The advancement of LED efficiency can be compared to the advancement made in silicon integrated circuits where the performance increase versus time has been characterized by Moore's law which states that the performance of silicon integrated circuits doubles approximately every 18 months. The historical development of the luminous efficiency of visible-spectrum LEDs is shown in Figure 2.1 [6]. The chart illustrates the modest beginnings of visible-spectrum LED technology which started in the 1960s. If the progress from 1960 to 2000 is assumed to be continuous, then the LED luminous efficiency has doubled every 4 years. In order to introduce the VLC analysis, it is needed to have a better understanding of the photometric units used to characterize the light intensity. The definitions and descriptions of the system in this regard is summarized in the following sections [6].

2.3.1 Basic Photometric Units

The physical properties of electromagnetic radiation are characterized by radiometric units. Using radiometric units, we can characterize light in terms of physical quantities; for example, the number of photons, photon energy, and optical power. However, the radiometric units are irrelevant when it comes to light perception by a human being. For example, infrared radiation causes no luminous sensation in the eye. To characterize the light and color sensation by the human eye, different types of units, called photometric units, are needed.

2.3.1.1 Luminous Flux, Luminous Intensity, and Illuminance

Although the term brightness is frequently used, it lacks a standardized scientific definition. The frequent usage is due to the fact that the general public can more easily relate to the term brightness than to photometric terms such as luminance or luminous intensity [6].

The luminous flux represents the light power of a source as perceived by the human eye. The unit of luminous flux is lumen (lm), which is defined in international system of units (SI unit).

The luminous flux, Φ_{lum}, is obtained from the radiometric light power using the Equation (2.1).

$$\Phi_{lum} = 683\frac{lm}{W}\int_{\lambda} V(\lambda)P(\lambda)d\lambda \tag{2.1}$$

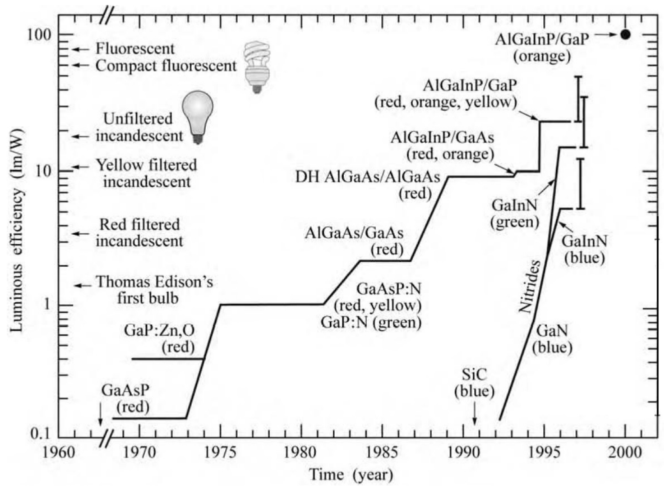


Figure 2.1: Luminous efficiency of LEDs and other sources vs. time

where $V(\lambda)$ is luminous efficiency function or eye sensitivity function, $P(\lambda)$ is the power spectral density, *i.e.* the light power emitted per unit wavelength, and the prefactor 683 lm/W is a normalization factor.

Luminous intensity which is used for expressing the brightness of an LED, represents the light intensity of an optical source, as perceived by the human eye. The luminous intensity is measured in units of candela (cd), which is a base unit of the SI. This luminous intensity is given as Equation (2.2).

$$I = \frac{d\Phi_{lum}}{d\Omega} \tag{2.2}$$

Where Ω is the spatial angle, and Φ_{lum} is the luminous flux.

The illuminance is the luminous flux incident per unit area and it is measured in Lux (lm/m^2). It is an SI unit used when characterizing illumination conditions. This is the main unit which can be used to measure the light intensity over an arbitrary area using the Lux meter. Being commercially available, Lux meter is used to characterize the light source. We have used Lux meter to verify the linear change of light over different dimming scenarios explained in more detail in Chapter 4.

The luminance of a surface source is the ratio of the luminous intensity emitted in a certain direction (measured in cd) divided by the projected surface area in

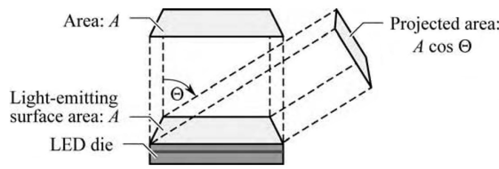


Figure 2.2: Area of LED, A, and projected area, A $\cos\Theta$ used for the definition of the luminance of an LED

Photometric unit	**Dimension**	**Radiometric unit**	**Dimension**
Luminous flux	lm	Radiant flux (optical power)	W
Luminous intensity	$lm/sr = cd$	Radiant intensity	W/sr
Illuminance	$lm/m^2 = lux$	Irradiance (power density)	W/m^2
Luminance	$lm/(srm^2) = cd/m^2$	Radiance	$W/(srm^2)$

Table 2.1: Photometric and corresponding radiometric units

that direction (measured in m^2). The luminance is measured in units of cd/m^2. In most cases, the direction of interest is normal to the chip surface. In this case, the luminance is the luminous intensity emitted along the chip-normal direction divided by the chip area. The projected surface area mentioned above follows a cosine law, *i.e.* the projected area is given by $A_{projected} = A_{surface} \times \cos\Theta$, where Θ is the angle between the direction considered and the surface normal. The light-emitting surface area and the projected area are shown in Figure 2.2. The luminous intensity of LEDs with lambertian emission pattern also depends on the angle according to a cosine law. Accordingly, the luminance of lambertian LEDs is a constant, independent of angle. Photometric units are summarized in Table 2.1.

Brightness is an attribute of visual perception and is frequently used as synonym for luminance. To quantify the brightness of a source, it is useful to differentiate between point and surface area sources. For point sources, brightness can be approximated by the luminous intensity (measured in cd). For surface sources, brightness can be approximated by the luminance (measured in cd/m^2).

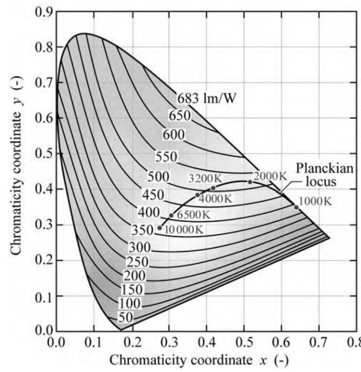


Figure 2.3: Relation of maximum possible luminous efficacy and chromaticity

2.3.1.2 Luminous Efficacy and Luminous Efficiency

This section describes the luminous efficacy as well as luminous efficiency which are the main two photometric units known to public showing the efficiency of the LED lamps.

The luminous efficacy of optical radiation (also called the luminosity function), measured in units of lumens per watt of optical power, is the conversion efficiency from optical power to luminous flux. The luminous efficacy is defined as

$$\frac{\Phi_{lum}}{P} = \frac{683\frac{lm}{W}\int_{\lambda} V(\lambda)P(\lambda)d\lambda}{\int_{\lambda} P(\lambda)d\lambda} \tag{2.3}$$

For strictly monochromatic light sources, the luminous efficacy is equal to the eye sensitivity function $V(\lambda)$ multiplied by 683 lm/W. However, for multicolor light sources and especially for white light sources, the luminous efficacy needs to be calculated by integration over all wavelengths.

The luminous efficacy is shown on the right-hand side of Figure 2.3. The luminous efficiency of a light source, also measured in units of lm/W, is the luminous flux of the light source divided by the electrical input power, *i.e.* $\Phi_{lum}/(I \times V)$, where the product $(I \times V)$ is the electrical input power of the device. In the lighting community, luminous efficiency is often referred to as luminous efficacy of the source. The luminous efficiency is the product of the luminous efficacy and the electrical-to-optical power conversion efficiency. Table 2.2 summarizes frequently used figures

Figure of merit	Explanation	Unit
Luminous efficacy	Luminous flux per optical unit power	lm/W
Luminous efficiency	Luminous flux per input electrical unit power	lm/W
Luminous intensity efficiency	Luminous flux per sr per input electrical unit power	cd/W
Luminance	Luminous flux per sr per chip unit area	cd/m^2

Table 2.2: Summary of photometric performance measures for LEDs

of merit for LEDs.

The optical power emitted by a light source is then given by

$$P_t = \int_{\lambda} P(\lambda) d\lambda \tag{2.4}$$

This power indicates the total energy radiated from an LED. This formula is used in characterizing the received power of light which is discussed later in section 2.3.3.

In analyzing the VLC system it is required to have a good understanding of the optical power, the channel behavior and the received optical power (either the direct detection or its reflected one). In the following a brief definition of these quantities are given.

2.3.2 Illuminance of LED Lighting

A horizontal illuminance, Ehor, at a point (x, y) is given by:

$$E_{hor} = I\left(0\right) \cos^m\left(\phi\right) / D_d^2 \times \cos\left(\psi\right) \tag{2.5}$$

Where $I\left(0\right)$ is the center luminous intensity of an LED, ϕ is the angle of irradiance, ψ is the angle of incidence, and D_d is the distance between an LED and a detector's surface. For these formulas it is assumed that the LED chip has a Lambertian radiation pattern. Here m is the order of Lambertian emission, and is given by the semi-angle at half illuminace of an LED $\Phi_{1/2}$ as $m = \ln 2 / \ln\left(\cos \Phi_{1/2}\right)$.

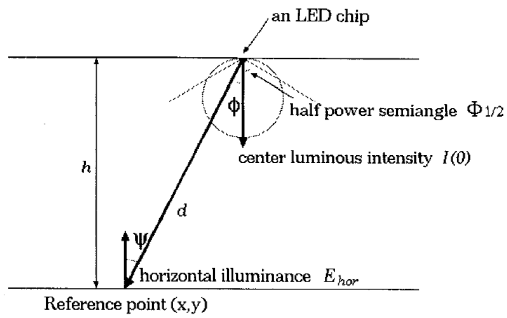


Figure 2.4: Horizontal illuminance of LED

2.3.3 Received Power from LED Lights

In an optical channel, the DC gain is given as

$$H\left(0\right)=\begin{cases}\frac{(m+1)A}{2\pi D_d^2}\cos^m\left(\phi\right)T_s\left(\psi\right)g\left(\psi\right)\cos\left(\psi\right) & 0\leq\psi\leq\Psi_c,\\ 0 & \psi>\Psi_c,\end{cases}\tag{2.6}$$

where A is the physical area of the detector, D_d is the distance between a transmitter and a receiver, ψ is the angle of incidence, ϕ is the angle of irradiance, $T_s\left(\psi\right)$ is the gain of an optical filter, $g\left(\psi\right)$ is the gain of an optical concentrator, and Ψ_c denotes the width of the field of vision at a receiver.

The optical concentrator $g\left(\psi\right)$ is given as:

$$g\left(\psi\right)=\begin{cases}\frac{n^2}{\sin^2\Psi_c} & 0\leq\psi\leq\Psi_c,\\ 0 & 0\geq\Psi_c,\end{cases}\tag{2.7}$$

where n denotes the refractive index. The received optical power P_r is derived by the transmitted optical power P_t as follows:

$$P_r=H\left(0\right)\times P_t\tag{2.8}$$

where P_t is the average transmitted optical power and is given as $P_t=\lim\limits_{T\to\infty}\frac{1}{2T}\int_{-T}^{T}X\left(t\right)dt$.

2.3.4 Received Power of Reflected Light

Here the reflective effect of light by walls is also considered. The received power is given by the channel DC gain on directed path $H_d(0)$ and reflected path $H_{ref}(0)$.

$$P_r = \sum \left\{ P_t H_d(0) + \int_{walls} P_t dH_{ref}(0) \right\} \tag{2.9}$$

The channel DC gain on the first reflrection is as follows:

$$dH_{ref}(0) = \begin{cases} \frac{(m+1)A}{2\pi^2 D_1^2 D_2^2} \rho dA_{wall} \cos^m(\phi) \cos(\alpha) \cos(\beta) T_s(\psi) g(\psi) \cos(\psi), & 0 \le \psi \le \Psi_c, \\ 0 & \psi > \Psi_c, \end{cases} \tag{2.10}$$

Where D_1 is the distance between an LED chip and a reflective point, D_2 is the distance between a reflective point and a receiver, ρ is the reflectance factor, dA_{wall} is a reflective area of small region, ϕ is the angle of irradiance, α is the angle of irradiance to a reflective point, β is the angle of irradiance to the receiver, ψ is the angle of incidence.

2.3.5 Optical Wireless Channel

It is assumed that the noise in optical channel is an AWGN (additive white Gaussian noise). The dominant source of noise in optical channel is known to be shot noise. A typical transmitted signal contain a time varying shot noise process which has an average rate of 10^4 to 10^5 photons per bit. It is probable that in an optical channel model the intense light striking the detector leads to a steady shot noise which has a rate of order of 10^7 to 10^8 photons per bit and as a result the shot noise caused by signals can be neglected. With this assumption the ambient-induced shot noise can be modeled as a Gaussian process. Also when little or no ambient light is present, the dominant noise source is receiver noise, which is also signal independent and Gaussian. All things considered, the optical wireless channel model is expressed as:

$$Y(t) = \gamma X(t) \oplus h(t) + N(t) \tag{2.11}$$

where $Y(t)$ represents the received signal current, γ is the detector responsivity, $X(t)$ represents the transmitted optical pulse, $h(t)$ is the impulse response, $N(t)$ represents the AWGN, and the symbol $\oplus$ denotes convolution. In VLC, the LEDs which have the function of communication have a wide irradiance angle because they also used for function of lighting equipment. As a result a non-directed LOS path is assumed.

It has been mentioned that VLC is a promising technology which takes advantage of LED devices. Study and analysis of LEDs is an essential part of VLC system design. In the following section of this introduction, after describing the operation of LED lamps and its different types the white LEDs, modulation characteristics as well as transient and frequency response of LEDs are explained in detail. This analysis offers vital clues in alleviating the low bandwidth limitation of white LEDs. These clues, indeed, open the doors to the invention of state of the art LED driver circuit design for high speed data transmission and dimming control.

2.4 White LED

LED is an optoelectronic device which generates light. It contains a P-N junction, through which an electric current is sent. In the heterojunction, the current generates electrons and holes, which release their energy portions as photons when they recombine. Two basic types of semiconductor optical sources exist: The LEDs and laser diodes (LD). Laser diodes are used for long distance, high data rate transmissions, while LED devices are used for shorter distance, lower data rate transmission. LED operation is based on spontaneous emission, while the laser operation is based on stimulated emission. In general, for both devices, the principle of operation is based on the interaction of light and matter with a semiconductor material.

Since, the incandescent lamp was invented by Edison in 1882, artificial lighting has passed through three phases incandescent lamp, neon light, and discharge lamp, and has been advancing towards the fourth phase of semiconductor lighting, especially white LEDs. In well under a decade, LEDs have expanded their role from

Material	Typical emission wavelengths
InGaN / GaN, ZnS	450 530 nm
GaP:N	565 nm
AlInGaP	590 620 nm
GaAsP, GaAsP:N	610 650 nm
InGaP	660 680 nm
AlGaAs, GaAs	680 860 nm
InGaAsP	1000 1700 nm

Table 2.3: Semiconductor materials and emission wavelengths

little red spots to brilliant white light sources capable of illuminating a room or lighting the road ahead.

Practical white LEDs were made possible by work with GaN semiconductor materials in the 1990s by Dr. Shuji Nakamura at Nichia Corporation in Japan. He first achieved blue and green LEDs. Nakamura's next step was placing a novel phosphor over his blue chip to get a white light, and finally he worked on the blue laser.

The center wavelength and thus the emission color of an LED are largely determined by the bandgap energy of the semiconductor material used. Essentially the whole visible wavelength region can be covered with LEDs, although the achievable power output and efficiency is not equally high for all wavelengths.

Table 2.3 shows the semiconductor materials and emission wavelengths. White light can be generated either by mixing the outputs of *e.g.* red, green and blue LEDs, or by using a single blue LED and some phosphor, which converts part of the blue light into a light with longer wavelengths.

2.4.1 Types of White LEDs

Two types of white-light LEDs used in lighting:

- Devices that use separate red green blue (RGB) emitters.
- Those that use a blue emitter in combination with a phosphor that emits yellow light.

The color of white LEDs comes from the narrow-band blue naturally emitted by GaN LEDs, plus a broad spectrum yellow generated by a phosphor coating on the die which absorbs a proportion of the blue and converts it to yellow. GaN die are InGaN hetero-structures, which can produce operational wavelengths from green to ultra-violet by varying the relative amounts of indium and gallium during production. Although this blue die plus yellow phosphor approach yields light which appears white, it has little green and almost no red content leading to inferior color rendering compared with incandescent bulbs and even tri-phosphor florescent tubes. Warm white LEDs, which include a red-producing phosphor, are an attempt to improve this situation as well as make LEDs illumination more acceptable in living spaces.

2.5 LED Modulation Characteristics

LEDs are the most commonly used light sources for local-area communication systems operating from very short ($< 1m$) to medium distances ($5km$). Typical bit rates are tens of Mbps up to about 1Gbps. LEDs are non-linear devices and as such the series resistance, shunt resistance, and capacitance depend strongly on the applied voltage. A thorough analysis must take into account these non-linearities. However, much can be learned by considering the LED as a linear device, even though some important aspects of the LED modulation behavior cannot be inferred from the linear model. In this section, we first analyze LEDs as linear devices and subsequently discuss modulation characteristics, including some non-linear modulation characteristics [6].

2.5.1 Rise and Fall Times, and Bandwidth

In this section, the rise and fall time and the frequency response of a linear RC system is explained. A simple RC circuit is shown in Figure 2.5(a). When subjected to a step-function input pulse, the output voltage increases according to (2.12).

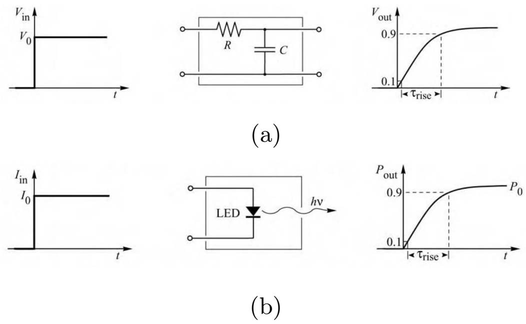


Figure 2.5: (a) Illustration of a linear RC system response, (b) Illustration of light output power

$$V_{out}(t) = V_0[1 - e^{\frac{-t}{\tau_1}}] \tag{2.12}$$

where $\tau_1 = RC$ is the time constant of the RC circuit. When the input voltage returns to zero, the output voltage decreases according to

$$V_{out}(t) = V_0 e^{\frac{-t}{\tau_2}} \tag{2.13}$$

For an RC circuit, $\tau_1 = \tau_2$. The rise and fall times are defined as the time difference between the 10% and 90% points of the voltage, as shown in Figure 2.5(a). The rise and fall times of the signal are related to the time constants τ_1 and τ_2 by

$$\tau_r = (\ln 9)\tau_1 \approx 2.2\tau_1, \tau_f = (\ln 9)\tau_2 \approx 2.2\tau_2 \tag{2.14}$$

The voltage transfer function $H(\omega)$ is given by (2.15).

$$H(\omega) = (1 + j\omega\tau)^{-1} \tag{2.15}$$

The bandwidth of the system corresponds to the frequency at which the power transmitted through the system is reduced to half of its low frequency value. This condition can be written as $|H(2\pi f)|^2 = 1/2$. As a result, the bandwidth of the RC circuit is given by (2.16).

$$f_{3dB} = \frac{1}{2\pi\tau} \approx \frac{0.70}{(\tau_r + \tau_f)} \tag{2.16}$$

The bandwidth is also called the 3dB frequency, since the power transmitted at this frequency is reduced by 3dB compared with its low frequency value. As a step function input current is applied to the LED, the optical output power increases according to (2.17).

$$P_{out}(t) = P_0[1 - e^{\frac{-t}{\tau_r}}] \tag{2.17}$$

The rise time τ_r is illustrated in Figure 2.5(b). In analogy to Equations (2.12) and (2.15), the power transfer function is given by (2.18).

$$H^2_{LED}(\omega) = (1 + j\omega\tau)^{-1} \tag{2.18}$$

The absolute value of the power transfer function is reduced to half at the 3dB frequency of the LED. Thus the 3dB frequency of an LED is given by (2.19).

$$f_{3dB} = \frac{\sqrt{3}}{2\pi\tau} \approx \frac{1.2}{(\tau_r + \tau_f)} \tag{2.19}$$

As a practical rule, the numerical factor 1.2 in the numerator of Equation (2.19) can vary between 1.0 and 1.5.

2.6 LED Transient and Frequency Response

As mentioned before, the limiting factor in achieving the high data rate communication link is the LED. So it is worth reviewing the LED performance, and its model. In this section after introducing the different capacitances associated with the LED, the transient and frequency behavior of LED is analyzed. This analysis shows that the LED has an inherent limitation that comes from the recombination carrier life time. When a diode changes from reverse biased to forward biased the charge being stored near and across the junction changes. Part of the change in charges is due to the change in the width of the depletion region and therefore the amount of immobile charge stored in it; this is the space-charge capacitance (C_s). An additional change in the charge storage is necessary to account for the excess of minority carriers close to the depletion region edges required for the diffusion current to exists. This component is modeled by another capacitance, called the diffusion capacitance (C_d). The total capacitance of a forward biased diode is the sum of the diffusion capacitance C_d and the depletion capacitance C_s, *i.e.* $C_{total} = C_d + C_s$.

2.6.1 Diffusion Capacitance C_d

The excess hole charge stored in the N region is given by $Q_p = I_p\tau_p$, and similarly, the excess electron charge stored in the P region is $Q_n = I_n\tau_n$. This leads to the total excess minority carrier charge of $Q_d = Q_p + Q_n = I_p\tau_p + I_n\tau_n$. $I_n(I_p)$ and $\tau_n(\tau_p)$ are the current in the N (P) region and the transient time of electrons (holes), respectively. Since the diode current is $I_d = I_p + I_n$, it is more convenient to express the excess charge as $Q_d = I_d\tau_s$, where τ_s is called mean transit time, also known as recombination lifetime. The following shows the derivation of this capacitance.

$$
\begin{aligned}
C_d = [\frac{dQ_d}{dV_d}] = \frac{d(\tau_s I_d)}{dV_d} &= \tau_s[\frac{d(I_d)}{dV_d}] \\
&= \tau_s[\frac{d(I_s.(e^{\frac{V_d}{V_T}} - 1))}{dV_d}] = \tau_s[\frac{I_s e^{\frac{V_d}{V_T}}}{V_T}] \\
&= \tau_s[\frac{I_d + I_s}{V_T}] \sim \tau_s[\frac{I_d}{V_T}]
\end{aligned}
$$

This shows that the diffusion capacitance is proportional to the diode current as well as recombination lifetime.

2.6.2 Frequency Response of a Forward Biased LED

In evaluating the overall frequency response of the VLC system, it is needed to have a good understanding of the frequency response of LED. The frequency response of a forward biased LED can be described by (2.20) [7].

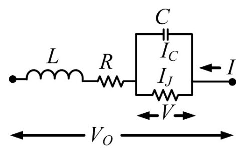


Figure 2.6: Equivalent circuit of a forward biased LED

$$P_s = \frac{P_o}{\sqrt{(1+\omega^2\tau_s^2)}} \tag{2.20}$$

where P_s, is the optical output power, ω is the angular frequency of the (constant amplitude) applied current, τ_s is the recombination lifetime, and P_o is the output power of the dc biased LED with $\omega = 0$. This indicates that the optical output power of diode decrease with both of ω and τ_s.

In the following we looked at different methods for deriving the transient response of white LEDs. Some of the methods neglects the diffusion capacitance and other neglects the depletion capacitance. The accurate model, however, should consider both and based on that a reliable model can be derived.

2.6.3 Response Time of LED Neglecting C_d

To analyze the response of an LED, we assume the equivalent circuit for forward-biased operation, shown in Figure 2.6 with a voltage-dependent capacitance C and a nonlinear resistive current I_J. The resistance R represents the sum of the resistance of the external circuit and the excess series resistance of the diode. The inductance L is mainly due to the lead wire [8].

The capacitance C_s of the diode due to the depletion layer is given by

$$C_s = \frac{C_0}{(\Phi - V)^n} \tag{2.21}$$

where C_0 is the total zero-bias capacitance, Φ denotes the diffusion potential (barrier voltage), V is the net voltage at the junction, and n is a number depending on the impurity profile of the junction. In general, the capacitance due to diffusion current also may contribute to the forward-biased diode capacitance. This contribution is ignored according to the following estimation. The upper bound of the diffusion capacitance C_d is given by its value at the low-frequency limit and at the highest diffusion current. C_d due to electron diffusion at the low-frequency limit is given by $(e/2kT)(eL_n n_{po})e^{eV/kT}$, where L_n, is the electron diffusion length and n_{po} is the injected electron density at the P region. C_d can be expressed as $eI_d\tau_n/2kT$, where τ_n is the lifetime of the electron, using the Equation (2.22).

$$I_d = ({}^{eL_n n_{po}}/_{\tau_n})e^{eV/kT} \tag{2.22}$$

On the other hand, the depletion-layer capacitance is much larger, at a particular current level, and the diffusion current I_d decreases super linearly with the decrease of the total current. The total current I through the diode is the sum of the reactive current I_C through the capacitance and the resistive junction current I_J. The latter current I_J is composed of the diffusion current I_d,which is responsible for the light emission, and the recombination in depletion layer current I_r, which is presumed to be non-radiative. The equations for all these currents are given in (2.23) to (2.26).

$$I = I_C + I_J \tag{2.23}$$

$$I_J = I_d + I_r \tag{2.24}$$

$$I_d = Ae^{\frac{eV}{kT}} \tag{2.25}$$

$$I_r = Be^{\frac{eV}{mkT}} \tag{2.26}$$

where m is a number depending on the recombination mechanism. The differential equation for the net junction voltage V in the equivalent circuit, for $V_o(t)$ applied at the terminals given in (2.27).

$$-LC\frac{d^2V}{dt^2} + (RC - L\frac{dI_J}{dV}) + L\frac{dC}{dV}(\frac{dV}{dt}) + RI_J + V = V_o(t) \tag{2.27}$$

Since the light emission from the junction is proportional to the diffusion current I_d , the transient behavior of the light intensity for any time-dependent applied voltage $V_o(t)$ can be obtained by solving Equation (2.27) for $V(t)$ and substituting this into Equation (2.25).

It is estimated [8] that the effect of the inductance on the transient response is very small compared to that of the capacitance except in the very short time interval, $t \leq 1ns$. Hence the responses of $V(t)$ and I_d are mainly governed by the depletion layer capacitance and the effective resistance of the circuit. It is concluded in [8] that the current-dependent delay times are mainly due to the voltage-dependent capacitance and resistance of the diode, as well as to the external series resistance. Accordingly, in order to realize the inherent fast response of the LED, reduction of the external impedance is needed. Reduction of the light-emitting area, increase of the operating current density, and superposition of a dc bias voltage are also effective.

2.6.4 Response Time of LED Considering both C_d and C_s

For an ideal LED, if the injected carriers arrive instaneously at the recombination (diffusion) region, the rise time of the spontaneous emission is governed by the recombination time of the carriers. However, in driving a practical diode, the junction capacitance and the stray capacitance cause delay in the arrival time of the injected carriers at the recombination region. Thus, the rise time of the spontaneous emission in an LED would be either (1) material-limited by the spontaneous recombination time τ_s or (2) ciruit-limited by the time constant t_c of the driving circuit with including the junction capacitance of the diode [9]. These results are considered in the design procedure of LED drivers in Chapter 5.

In practical applications for high modulation rates, a combination of the following techniques can be used: (1) constructing diodes to have low capacitance, (2) employing drivers with low output impedance in order to match the diode impedance and (3) properly shaping the driving current pulse.

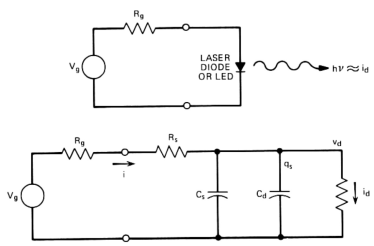


Figure 2.7: The diode equivalent circuit

2.6.4.1 Description of the Diodes and the Equivalent Circuit

Figure 2.7 shows the equivalent circuit for the study of the transient behavior of diode. A nonlinear resistor respresents the I-V characteristic of the diode, described by $I_0]e^{\frac{qv_d}{nkT}} - 1]$ where v_d is the junction voltage. The factor n is unity for ideal diode diffusion current and for a heavily doped P-N junction n is approximately 2. In the transient case, part of the injected carriers will recharge the carriers that recombine, and the rest will build up as stored charges. Thus, the stored charges will increase as $(1 - e^{-t/\tau_s})$, where the time constant τ_s is the carrier recombination time. This is equivalent to a capacitance, C_d, whose charge, $q_d(t)$, is equal to the stored charge and whose instantaneous charge-voltage relationship satisfies $q_d = Q_0[e^{\frac{qv_d}{nkT}} - 1]$, where v_d is the instantaneous junction voltage, and $Q_0 = I_0\tau_s$. And the diffusion capacitance is calculated as $C_d = \frac{dq_d}{dv_d} = \tau_s \frac{di_d}{dv_d}$, and calculated in 2.6.1. In addition to the diffusion capacitance, there is the space-charge capacitance of the depletion layer. The space-charge capacitance, in parallel with C_d, is given by 2.21.

Referring to Figure 2.7, resistance R_s in the equivalent circuit accounts for the series resistance of the bulk material as well as the contact resistances. The driver output impedance is represented by R_g, and V_g is a rectangular voltage pulse amplitude. The following circuit equations can be used for finding the LED current formula.

$$i = \frac{V_g - v_d}{R_g + R_s} \tag{2.28}$$

$$i_c = i - i_d \tag{2.29}$$

$$v_d = \int \frac{i_c}{C_s + C_d} dt. \tag{2.30}$$

Since the spontaneous emission is proportional to the diffusion current, the time dependence of emission can be found from the time response of i_d.

2.6.5 Transient Behavior: Closed-form Calculation

In last two sections, the methods for calculating the transient behavior of LED considering diffusion capacitance, C_d, and depletion capacitance, C_s, are discussed. In this section this analysis continues to derive an appropriate formula for the transient response of LED. Transient behavior of LED is derived based on the assumption of current-independent space charge capacitance. The results of this section is a good reference in designing high bandwidth LED drivers [10, 11]. One specific technique called pulse shaping which explained in more detail in chapter 5 is based on the results of this section. A closed-form expression relating the source rise time to the parameters of the LED and the current would therefore be of value in engineering analyses of optical communications systems. The diode is driven by a current step function of amplitude I_T. This current is divided into a diffusion current I_d and a capacitive current I_c which flows through the parallel combination of the space-charge capacitance C_s and the diffusion capacitance C_d. The basic assumption is that C_s is a slowly varying function of current with respect to C_d and can be considered constant. In such devices, only a small part of the space-charge capacity is modulated because the junction voltage is high only near the contact. The differential equation describing the current flow through the diode is

$$\frac{dI}{d\tau} = \frac{\beta\tau_s I_0 (I+1)(I'_T - 1)}{C_j + \beta\tau_S I_0 (I+1)} \tag{2.31}$$

in which I_0 is the saturation current, $\beta = q/2kT$, τ_S is the lifetime, $\tau = t/\tau_s$, $I = I_d/I_0$, and $I'_T = I_T/I_0$. The integral of Equation (2.31) is

$$\tau = \frac{C_j}{\beta\tau_s I_T}\ln I + (\frac{C_j}{\beta\tau_s I_T} + 1)\ln(1 - \frac{I_d}{I_T})^{-1} \tag{2.32}$$

where it has been assumed that $I \gg 1$ and $I'_T \gg 1$.

From Equation (2.32), the rise time to a current of ηI_T, $0 < \eta < 1$, is

$$t(\eta) = \frac{C_j}{\beta I_T}\ln(\frac{\eta}{1-\eta}\frac{I_T}{I_0}) + \tau_s\ln(\frac{1}{1-\eta}) \tag{2.33}$$

and the rise time between currents of $\eta_1 I_T$ and $\eta_2 I_T$ is

$$t(\eta_2) - t(\eta_1) = \frac{C_j}{\beta I_T}\ln(\frac{\eta_2(1-\eta_1)}{\eta_1(1-\eta_2)}) + \tau_s\ln(\frac{1-\eta_1}{1-\eta_2}) \tag{2.34}$$

Since the power out is proportional to the diffusion current, these expressions also give the rise time of the power. From Equation (2.33), the rise time of the half current and, hence, half power point is given by (2.35).

$$t_{1/2} = \frac{C_j}{\beta I_T}\ln(\frac{I_T}{I_0}) + \tau_s\ln 2 \tag{2.35}$$

From Equation (2.34), the 10-90% rise time is

$$t_r = (\frac{2C_j}{\beta I_T} + \tau_s)\ln 9 \tag{2.36}$$

These expressions predict a decrease in rise time with increasing current and an increase in rise time with an increase in space-charge capacitance as well as with temperature. In the limit of high current, the rise time depends only on the minority-carrier lifetime τ_s. These expressions show that in order to achieve high-frequency operation with an LED, its C_s must be minimized, its τ_s must be reduced, and an I_T as high as practical must be used. The lifetime τ_s can be reduced by doping the active layer and by reducing the active-layer width to enhance nonradiative recombination at the junction.

Current peaking, which also serves to reduce the rise time, can also be analyzed with this model. The solution for the $10-90\%$ rise time t_r for a staircase excitation current, $I_T = I_a$, $0 \leq t \leq t_a$, and $I_T = I_b$, $t > t_a$, is

$$t_r = \frac{C_s}{\beta I_a} \ln 9 + (\frac{C_s}{\beta I_a} + \tau_s) \ln \frac{1-(I_b/10I_a)}{1-(9I_b/10I_a)} \tag{2.37}$$

where it has been assumed that t_a is the time required for the diffusion current to reach I_b ($I_a > I_b$), *i.e.*,

$$t_a = t(I_b) = \frac{C_s}{\beta I_a} \ln \frac{I_b}{I_a - I_b} \frac{I_a}{I_0} + \tau_s \ln(1 - \frac{I_b}{I_a})^{-1} \tag{2.38}$$

As an example of the possible reduction in rise time, if $I_a = 2I_b$ and I_a is assumed to be in the high-current limit, $t_a \cong \tau_s \ln 2$ and $t_r \simeq 0.55\tau_s$, considerably less than the value of $2.2\tau_s$ which is the minimum t_r without current peaking [10,11].

2.6.6 Low-Frequency Response of LED

The assumption in characterizing of the LEDs that the frequency response is flat from DC till the 3dB frequency of the LED, is not valid. As explained here, LED's frequency response drops at lower frequencies. This reduction has been verified throughout the characterization process of the LED drivers populated for this work as well.

The output power P of an LED is linearly proportional to the forward current I. However, with increasing current, the output is saturated due to junction-heating effects. Figure 2.8 shows a comparison of modulations at the lower and higher frequencies. The solid line in Figure 2.8 represents the I-P characteristics at dc, indicating reduced output power at high currents [12].

This is caused by a reduction of internal quantum efficiency by thermal effects, such as the temperature dependence of the recombination constant, interfacial recombination, and carrier leakage through the heterojunctions. The modulation on this curve corresponds to a low frequency. Therefore, the output power contains significant distortion as shown in Figure 2.8(c), and is actually reduced in amplitude.

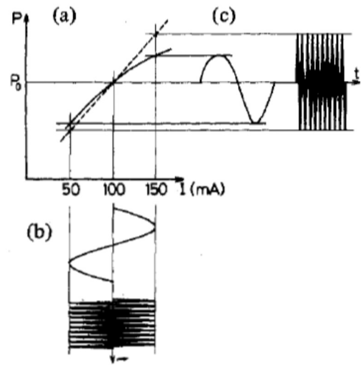


Figure 2.8: Low-frequency response (a) Power vs. current (b) Current signal (c) Modulated optical signal

The broken line in Figure 2.8(a) represents output power versus current at constant junction temperature. At a higher frequency comparable with the thermal time constant of an LED, a signal is modulated on this curve, and the distortion of the output is less than that at the lower frequency. Consequently, the low-frequency response is limited and the modulated output power is reduced at a lower frequency owing to the large distortion.

2.7 Conclusion

LEDs are at the advent of a big revolutionary transfer. Sooner or later, they are going to be known not only as a unique source of indoor and outdoor lighting, but also as an access point for transferring packets of data through the free space medium and using the visible light communication. As a result of concurrent illumination control and data transmission within a visible light network, lamps will be able to wirelessly communicate with each other and coordinate their appropriate functionality. In this regard, the big advantageous lies under the huge savings of energy granted due to optimum usage of LEDs instead of other sorts of conventional lamps. In this chapter, after introducing the VLC, the basic analysis of the system in terms of the optical channel, transmit and received power are reviewed. It has mentioned that the bottleneck of achieving the high speed in the VLC networks comes from the source, LED, itself. To better understand this problem, the LED model and its transient and frequency response calculation and analysis are discussed. It turns out that the parasitic capacitance of LED as well as its carrier recombination life time induces the major participation in the rise and fall tiems of the LEDs. The final results of the closed form calculation of LED rise and fall time enlighten the path through finding a solution for this big limitation of LEDs.

Chapter 3

Linear and Switch-mode Regulator for LED Drivers

3.1 Introduction

The growing adoption of LEDs as a lighting source in different applications has simultaneously driven the demand for LED driver ICs to power them. To understand the obstacles for the design and manufacturing of these LED driver ICs, it is necessary to understand what a white LED requires in order to produce light. A White LED must be driven by a constant current source so that the white point of the light does not shift. In general, the LED current is controlled using PWM, dc current or the combination of the two. In this regard, pure dc driving is the cheapest and easiest method and superimposing a small ripple has no significant influence on the luminous efficiency. However, peak emission wavelength of LEDs tends to shift with the forward current causing the change of color with dimming. Consequently, the PWM-dimming is preferred upon dc driving. In PWM driving method the efficiency stays at the same level for all dim levels and it maintains better chromaticity control and flexibility for dimming. Furthermore, since the white LED is a diode, its internal forward voltage (V_f) varies with the current rating of the white LED and will also change with temperature. A typical $20mA$ white LED has a V_f that varies between $2.5V$ and $3.9V$ over the entire operating temperature range. Consequently a way of regulating the LED current should be utilized. Either of linear or switching regulators can be used. In this chapter both of these two approaches are reviewed. The efficiency is one of the top priorities for the design of LED driver and this constraint put a limit on using the linear regulators due to their poor efficiencies compare to the switching regulators.

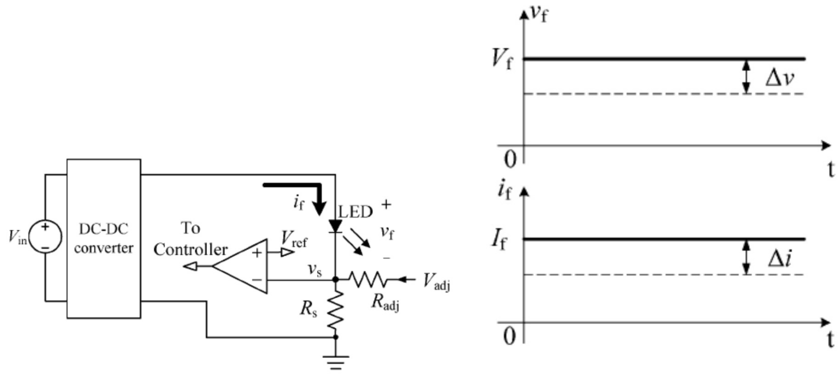
3.2 LED Driving Techniques

The most common ways of driving the LEDs are amplitude-mode and PWM-mode techniques. These two techniques together with a combinational driving technique, called bilevel driving technique, which takes advantages of both amplitude and PWM mode techniques are explained in the following section.

3.2.1 Amplitude-Mode Driving Technique

Since LEDs are current-driven devices, the luminous intensity of LEDs is typically controlled by controlling the forward current flowing through the LED. The default method for driving LEDs is by using a constant dc, commonly known as amplitude-mode driving technique. However, this is reported that the peak emission wavelength of LEDs tend to shift with the forward current, which can lead to color variations at different luminosity levels [13], [14]. This makes the amplitude-mode driving technique unsuitable for use in dimming LEDs as the forward current must be continuously adjusted for various luminosity levels. Even when operated without dimming, the small dynamic resistance of LEDs generates some ripples which can also lead to the same color variation problem.

A constant forward current must be maintained for driving an LED with this driving technique. A typical setup is illustrated in Figure 3.1(a), where current regulation is achieved by sensing the LED current using resistor R_s, and the voltage across the sense resistor is fed to an error amplifier or controller that adjusts the output voltage of the DC-DC converter to a value that supplies the required current.



(a) schematic representation (b) driving waveforms

Figure 3.1: Conventional amplitude-mode driving

In order to control different brightness, an external voltage V_{adj} is used for varying the voltage across R_s. To ensure a reliable control of the LED current, a highly stable output voltage from the DC-DC converter is required. For better regulation, the shunt resistor typically used for sensing the LED current can be replaced by linear current regulator, and the voltage drop of the linear regulator is used to control the output dc voltage to the desired value. In this topology, dimming is commonly achieved by varying the reference voltage to which the sensed voltage is compared. Figure 3.1(b) shows the change of LED current I_f according to the LED voltage, V_f chantge.

Multiple LED lamps are usually connected in parallel for obtaining enough lighting levels. In addition, dimming control is often needed to regulate lighting levels for human needs. A conventional linear current-regulator method, as shown in Figure 3.2, has simple circuit configuration. It is widely used for dimming applications by modulating the current amplitude of the parallel-connected LED lamps [15].

In this circuit due to the negative feedback composed of opamp, MOSFET and the sensing resistor, the Dimming Signal sets the constant current of LEDs.

3.2.2 PWM-Mode Driving Technique

This is a method by which the LED is switched on and off at high frequency and the luminous intensity is controlled by adjusting the duty cycle. Since the peak cur-

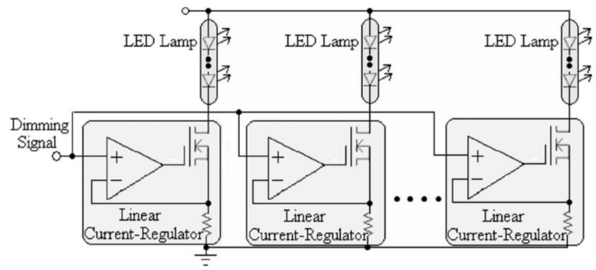
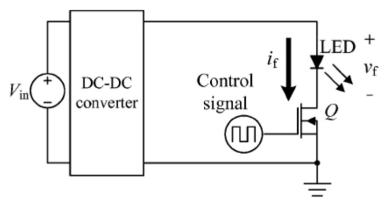
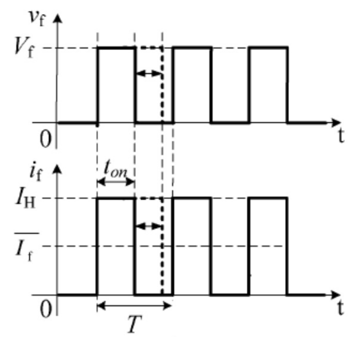


Figure 3.2: Conventional linear current-regulator method for multiple LEDs



(a) schematic representation



(b) driving waveforms

Figure 3.3: Conventional PWM-mode driving

rent level is kept constant during the switching, the control of luminosity level by dimming will not shift the color wavelength and consequently the light chromaticity is improved [16]. Despite improved chromaticity and flexibility for dimming, the PWM drivers are inherently more complicated since a combination of dc power source and switching network is usually needed, which increases the driver complexity. Based on [17], the reliability of LEDs is highly sensitive to the peak current level, and the stresses induced by higher peak current levels typically lead to faster performance decay or device failure. Since LEDs show extremely fast response to the driving current, this characteristic makes them suitable for use with the PWM driving technique. As shown in Figure 3.3, the current flowing through the LED is periodically switched between a high and zero level by a switch connected in series with the LED. With PWM mode, the average LED current is given by $\overline{I_f} = DI_f$, and $D = t_{on}/T$, where I_f is the high-level PWM current, D is the duty cycle, and t_{on} and T are the turn-on time and the switching period of switch Q, respectively.

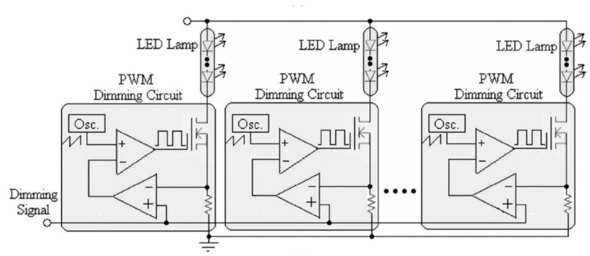


Figure 3.4: Conventional PWM-mode driving technique using multiple LEDs

Since the peak current level in PWM driving technique is fixed and dimming is achieved by varying the duty cycle, the stability of luminous intensity and color will depend on the accuracy of the peak current level and duty cycle. Therefore, the luminous intensity and color could still vary when ripples are present in the output current although the problem is less severe compared to the amplitude-mode driving due to the duty-cycle-averaging action in the PWM case.

As mentioned earlier, the amplitude-mode dimming is not recommended at currents lower than the test conditions because it may produce unpredictable results and may be subjected to variation in performance. As shown in Figure 3.4, a PWM dimming method can be used to dim the LED lamp by modulating its pulse current width [15].

Similar to the circuit of Figure 3.2, the control is achieved by the negative feedback. However, here the dimming is done based on the PWM method and the Dimming Signal sets duty ratio of the PWM signal at the gate of MOSFET.

3.2.3 Bilevel Current Driving

The control of LED operation mainly involves monitoring and regulating the average forward current flowing through the device. The luminous intensity of LEDs tends to saturate at high forward currents. This feature gives rise to different luminosity levels when the LED is driven by dc and PWM currents of the same average value. In general, for a given average forward current, the amplitude mode always produces a higher luminous intensity compared to the PWM-mode driving technique. The reason is that the latter operates at higher peak current level where less light is produced due to the saturation phenomenon. When linearly averaged by the duty cycle, this results in a lower luminous intensity. However, with better chromaticity and flexibility for dimming, the PWM-mode driving technique is preferred and more often used in practice where dimming is required at the expense of poorer luminous efficacy. In [18], a combinatory approach is developed to harvest the relative advantages of the two conventional driving techniques described before. For having the color stability and dimming flexibility, PWM mode is employed to switch the LED current between two levels, which forms the dominant current component of the device. In bilevel design for compensating the degradation in the luminous intensity due to duty-cycle averaging in the PWM mode, the lower level of the PWM current is raised above zero. As a result, the higher current level can be lowered accordingly for a given average current. As the modified PWM current waveform starts to deviate from the simple on-off pulses toward a dc by having the two current levels approaching each other from opposite directions, the detrimental effect of the duty-cycle averaging in simple PWM mode can be gradually compensated and higher luminosity is obtained. The highest illuminance can be obtained by driving the LEDs with dc but the requirements on the power sources stability and control precision are rather stringent; consequently the PWM driving technique is preferred option. The bilevel technique makes a balance between their relative advantages and disadvantages of amplitude and PWM mode driving techniques. It has been demonstrated that the illuminance efficacy of LEDs can be improved by introducing a dc-offset component into the PWM current [18], [19] . For this manner, periodic switching of the LED current between two levels, I_H and I_L is chosen in [18] as shown in Figure 3.5. With a conventional PWM driving technique, I_L is set to zero and corresponds to the off period of the current. This causes I_L to make no contribution to the light generation, but nevertheless contributes directly to the overall illuminance through an averaging step.

It has mentioned that irrespective of using either amplitude-mode or PWM mode, the current regulation methods should be hired. To achieve this goal either the linear regulator or switching DC-DC converters which has internal voltage or current

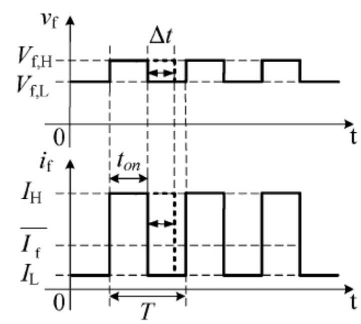
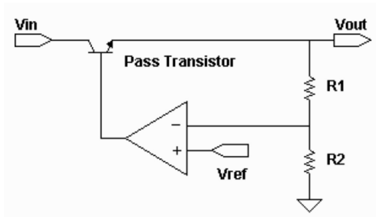


Figure 3.5: The LED current and voltage waveforms of bilevel current driving

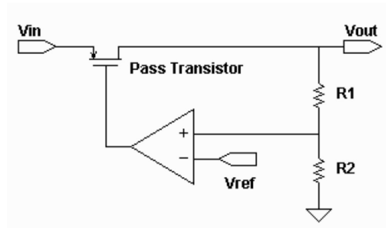
mode control should be utilized. In the following section a brief review of linear regulators and switching DC-DC converters are described. Linear voltage regulators come in two different topologies: conventional linear regulators and LDO voltage regulators [20]. In some designs it is needed to implement the current regulation using both of the linear regulators as well as switching regulators [21].

3.3 Linear Regulator

The linear regulator is very simple and cost effective to provide current source for driving LEDs. It also has the advantage of current sharing capability for multiple LED string configurations by using current mirror. Linear current sources are the most widely used current sources due to their small size and lack of a magnetic component, such as an inductor or transformer and their implementation is cost effective [22]. While there are many different ways to design a linear current source, one of the simplest and most robust methods is to use a circuit similar to Figure 3.6(a). This is composed of an opamp, a pass transistor and a current sensing resistor and a reference voltage. The main advantages of a linear current source are the low cost, and relatively small size. The main disadvantage of linear current sources is that they require greater headroom voltage and, therefore, dissipate more power than switching current sources. This power dissipation inherent to linear current sources limits them to lower power applications or applications that can tolerate large heat sinks and higher device junction temperatures [20].

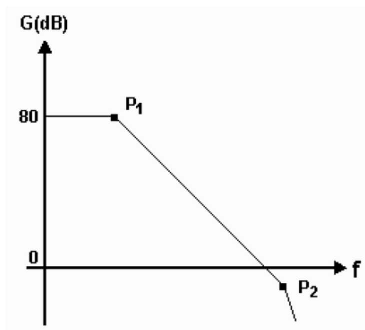


(a) Conventional linear regulator

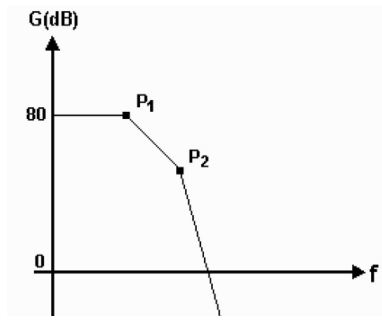


(b) LDO voltage regulator

Figure 3.6: Linear voltage regulator topologies



(a) Conventional regulator



(b) LDO regulator

Figure 3.7: AC pole locations without compensation

LDO regulators are an essential part of the power management system that provides constant voltage supply rails. They fall into a class of linear voltage regulators with improved power efficiency. Figure 3.6(a) shows a typical circuit schematic of the LDO. The only topological difference betweeen the voltage regulator and L-DO arises from the orientation of the pass element. The conventional linear voltage regulator uses a source follower. The LDO regulator on the other hand uses a single transistor in a common-source configuration operating in saturation. The two configurations are shown in Figure 3.6. The transistor orientation affects the stability of the regulator.

Typical small signal ac responses for both architectures are shown in Figure 3.7. The conventional linear regulator is inherently stable due to the low output impedance of the source follower. The first pole, P_1, acting as the dominant pole, is generated from the error amplifier output impedance. The output pole, P_2, moves with the load impedance but resides at much higher frequency. LDO voltage reg-

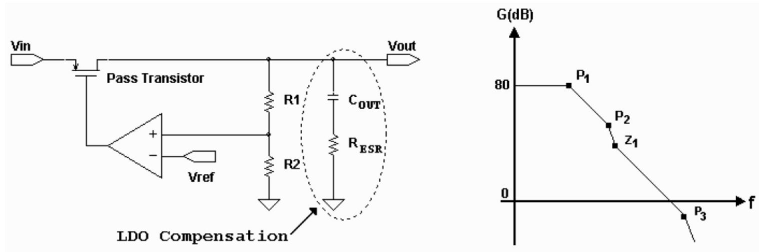


Figure 3.8: Conventional LDO regulator compensation

ulators can operate in low voltage applications, but they are inherently unstable. The large output capacitor and high output impedance generate the dominant pole, P_1. This dominant pole, however, is located in close proximity to the error amplifier output pole, P_2. Thus, the LDO regulators stability can not be guaranteed and will most likely be unstable. LDO regulators must be internally or externally compensated for guaranteed stability. Typical LDO regulators use the electro-static resistance (ESR) of the output capacitor to reach stability. The ESR generates a zero, that when placed in the vicinity of P_2, can add phase necessary to maintain stability. Figure 3.8 shows the use of capacitor ESR.

The ESR also generates a pole, P_3. The regulator stability depends heavily on the value of ESR. As ESR is decreased, the location of Z_1 moves to the right and consequently has no effect on phase margin. On the other extreme, when ESR is increased significantly, the associated pole, P_3, moves below the gain-bandwidth, and the LDO regulator becomes unstable. An LDO regulator must be given a range of stable capacitor ESR, otherwise the LDO regulator will be unstable.

Efficiency is improved over conventional linear regulators by replacing the common-drain pass element with a common-source pass element to reduce the minimum required voltage drop across the control device. Among all the power management systems, low-dropout voltage regulator (LDO) is the most preferable choice due to its advantages such as low power, small output ripple, no electromagnetic interference, and high power supply rejection ratio [23]. For different applications, LDO regulators should be able to support load current capacity from several hundred mA to A values. The internal blocks of an LDO regulator is shown in Figure

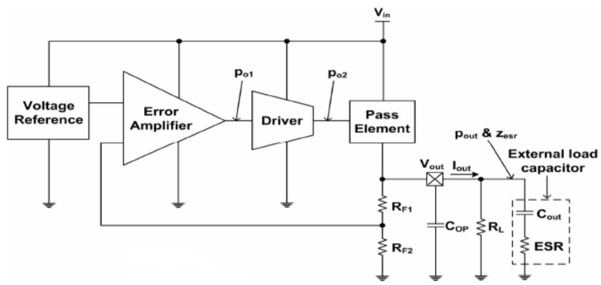


Figure 3.9: Internal block diagram of a conventinal LDO

3.9.

The LDO is connected in a closed loop system as shown in Figure 3.9. The feedback type is a series-shunt negative feedback to dynamically control the pass element. The pass element is usually a power PMOS transistor to reduce dropout voltage. Owing to the fact that the power PMOS must provide large transconductance and large load current, it is always designed to have a large size of even in the order of ten thousand μm. However, the gate capacitance of the power PMOS will contribute a parasitic pole located at low frequencies, and thus the stability of the system will be degraded. Furthermore, because the external load capacitor is very large as well, it will contribute another dominant pole. Therefore, the structure is intrinsically unstable because it has three low-frequency poles, which are generated at the outputs of the pass element, the driver, and the error amplifier, respectively.

As mentioned earlier in this section, with the series connection of the load capacitor and its ESR, it generates a zero and gives the required stability, as the solid line in Figure 3.9. If the loop gain is too high, as the dashed line in Figure 3.9, and P_{o2} locates before the unity-gain frequency, an even larger load capacitance is required to retain stability for the LDO regulator. This compensation method usually has a narrow bandwidth [24]. The values of the ESR differ by different materials of load capacitors, and even by different manufacturers, so it is very difficult to control the accurate value of capacitance and ESR. This ESR introduces a left-half plane (LHP) zero to the loop-gain transfer function which counteracts the additional negative phase shift introduced by one of the two dominant poles. Different solutions have proposed for the stability problems that occur when the LDO load varies widely. In [25] the LDO regulator adopts both a feed-forward path and a fast path to achieve fast load transient responses, small overshoots and undershoots. It utilized enhanced active feedback techniques and embedded RC blocks and can work under low load capacitance or even without external load capacitors. In [26] the proposed LDO does not require compensation capacitors, and it is stable for a wide range of load capacitors, which are also a part of the frequency compensation. The LDO circuit becomes a single-pole system with the pole defined by the gate capacitance of the pass transistor. In this design, the current operational amplifier allows acheiving high loop gains, wide bandwidth and fast transients. In [27] nested Miller compensation (NMC) with active capacitor and resistor is used to control the damping factor and reduce the required Miller capacitance. In NMC, a capacitor is connected from output of first g_m stage (or error amplifier) to the drain of PMOS and one capacitor from output of second g_m stage (driver or output stage) to the drain of the PMOS pass transistor. A proposed solution to control the damping factor and reduce the area of the compensation capacitor on chip is the NMC technique with active capacitor and resistor which is called an NMCACR LDO. This technique can resolve the trade-off between the dc loop gain and the damping factor. Another robust frequency compensation is reported in [28] which generates a zero internally instead of just relying on the zero generated by the load capacitor and its ESR.

In [23] a new topology which is based on three-stage amplifier combined with a transient response enhancement network is proposed. As shown in Figure 3.10, transient enhancement network and pole-splitting configuration are added to the traditional LDO to ensure the stability and fast transient response without the large output capacitor. This is based on the architecture of nested Miller compensation three-stage amplifier and transient enhancement network. In [27], the pole-splitting and the transient enhancement shown in Figure 3.10 are replaced by just two active capacitors.

One of the big concerns in the design of the LED driver is the efficiency. Regarding this parameter, the trend toward the current regulation is using the DC-

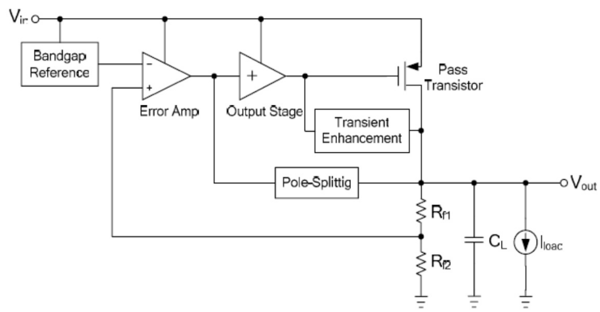
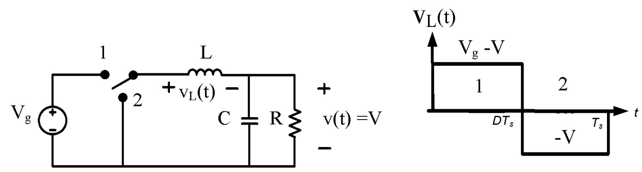


Figure 3.10: LDO with enhancement transient response

DC power converters due to their high efficiencies. In the following a brief review is presented with the focus on the buck converter.

3.4 Swithing Mode Regulator

Another widely used type of LED driver, the switch mode regulator, can provide independent accurate current control and achieve high efficiency as well. The LED driver is required to operate at high switching frequency for reducing the required values of passive components. However, cost of this LED driving solution is high, especially for large LED luminaries in which multiple switch mode LED drivers are needed. DC-DC power converters are employed in a variety of applications such as power supplies for personal computers, telecommunications equipment, and battery chargers to name a few. The input to a DC-DC converter is an unregulated dc voltage V_g. The converter produces a regulated output voltage V. The ideal DC-DC converter exhibits 100% efficiency; in practice, efficiencies of 70% to 95% are typically obtained. This is achieved using switched-mode circuits whose elements dissipate negligible power. PWM allows control and regulation of the total output voltage [29]. For efficiency reasons, LED strings cannot be supplied via series resistors but need switched mode power drivers with current control. In order to avoid high losses in a series resistor, power LEDs have to be supplied by switched mode power supplies. DC-DC converters are typically designed to stabilize their output voltages, while LEDs require a stabilized output current. By adding a shunt resistor R_s in series to the LEDs, the current can be measured via the voltage at the shunt



(a) schematic (b) switch voltage waveform

Figure 3.11: The buck converter consists of a switch network and a low-pass filter

R_s, so that standard circuit topologies and control schemes can be applied [30–32]

A large number of DC-DC converter circuits are known that can increase or decrease the magnitude of the dc voltage and/or invert its polarity. Here the focus is on the buck DC-DC converter; its circuit is depicted in Figure 3.11. The switch position varies periodically, such that $v(t)$ is a rectangular waveform having period T_s and duty cycle D. The duty cycle is equal to the fraction of time that the switch is connected in position 1, and hence $0 \leq D \leq 1$. The switching frequency f_s is equal to $1/T_s$. In practice, the SPDT switch is realized using semiconductor devices such as diodes, power MOSFETs and BJTs. The average value of $v(t)$ is given by DV_g. In addition to the desired dc voltage component V, the switch waveform $v(t)$ also contains undesired harmonics of the switching frequency. In most applications, these harmonics must be removed, such that the converter output voltage $v(t)$ is essentially equal to the dc component V. A low-pass filter is employed for this purpose. The converter of Figure 3.11 contains an LC low pass filter. The filter has corner frequency f_0 given by $f_0 = 1/(2\pi\sqrt{LC})$. The conversion ratio $M(D)$ is defined as the ratio of the dc output voltage V to the dc input voltage V_g under steady-state conditions; $M(D) = V/V_g$. For buck converter $M(D) = D$.

Increasing switching frequency allows pushing the unity GBW of the converter to higher frequency which helps achieving fast transient response and also reducing the size of the compensator. As an example, a 20MHz voltage mode DC-DC buck converter fabricated in $0.5\mu m$ Bi-CMOS technology. The input voltage range of the IC is 2.7-5.5 V with loading current of maximum $600mA$ [33].

Figure 3.12 illustrates one way of realizing the switch network in the buck

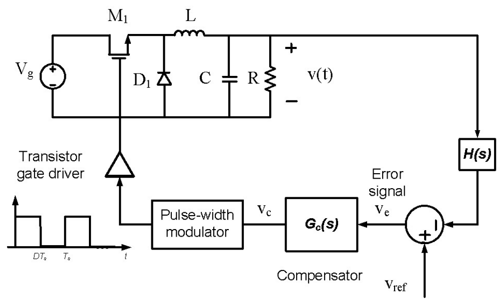


Figure 3.12: Realization of the ideal switch using a transistor and freewheeling diode

converter, using a power MOSFET and diode. This figure depicts the realization of the ideal SPDT switch using a transistor and freewheeling diode. In addition, a feedback loop is added for regulation of the output voltage. A gate drive circuit switches the MOSFET between the conducting (on) and blocking (off) states, as commanded by the Transistor gate driver.

Since the converter output voltage $v(t)$ is a function of the switch duty cycle D, a control system can be constructed that varies the duty cycle to cause the output voltage to follow a given reference v_{ref}. Figure 3.12 illustrates the block diagram of a simple converter feedback system. The output voltage is sensed using a voltage divider, and is compared with an accurate dc reference voltage v_{ref}. The resulting error signal is passed through an opamp compensation network. The analog voltage v_c is next fed into a PWM block. The modulator produces a switched voltage waveform that controls the gate of the power MOSFET M_1. The duty cycle D of this waveform is proportional to the control voltage v_c. If this control system is well designed, then the duty cycle is automatically adjusted such that the converter output voltage v follows the reference voltage v_{ref}, and is independent of variations in V_g or load current. The MOSFET and diode here are the switches used for this buck converter. In voltage mode feedback control, the $H(s)$ is just a resistor dividing branch which sample a portion of output voltage V and equate it to v_{ref} for normal operation. For current control, this $H(s)$ can monitor the current through the LEDs by putting a series resistance with the LEDs [29], [31]. In [31] a buck-boost DC-DC converter for LED drivers is reported. This LED driver is capable of delivering

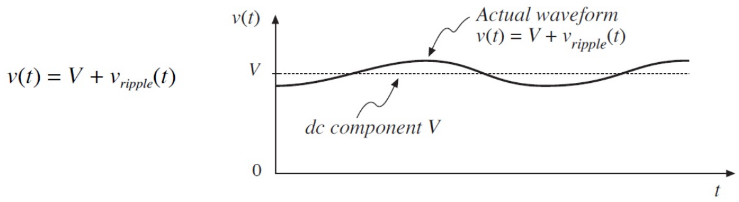


Figure 3.13: Small ripple approximation

an output current ranging from 0.1 to 2 A and a variable output voltage ranging between 2 and 5 V at $0.18\mu m$ CMOS technology. The feedback is taken from the voltage across the cathode of the LED.

Under steady-state conditions, the voltage and current waveforms of a DC-DC converter can be found by use of two basic circuit analysis principles. The principle of inductor volt-second balance states that the average value, or dc component, of voltage applied across an ideal inductor winding must be zero. This principle also applies to each winding of a transformer or other multiple winding magnetic devices. Its dual, the principle of capacitor amp-second or charge balance, states that the average current that flows through an ideal capacitor must be zero. Hence, to determine the voltages and currents of DC-DC converters operating in periodic steady state, one averages the inductor current and capacitor voltage waveforms over one switching period, and equates the results to zero. The equations are greatly simplified by use of the small ripple approximation. The inductor currents and capacitor voltages contain dc components, plus switching ripple at the switching frequency and its harmonics. In most well designed converters, the switching ripple is small in magnitude compared to the dc components and can be ignored. This effect is illustrated in Figure 3.13 and for small ripple approximation $v_{ripple}(t) \ll V$.

As an example, output voltage V of the buck converter shown in Figure 3.11(a) is calculated here. Typical inductor voltage and capacitor current waveforms are sketched in Figure 3.11(b). By use of the small ripple approximation, $v(t)$ can be replaced by V. When the converter operates in steady state, the average value, or dc component, of the inductor voltage waveform $v_L(t)$ must be equal to zero which yields to Equation (3.1).

$$(V_g V)DT_s + (-V)(1 - D)T_s = 0 \tag{3.1}$$

This is equivalent to $V = DV_g$. To design the control system of a converter, it is necessary to model the converter dynamic behavior. These difficulties can be overcome through the use of waveform averaging and small signal modeling techniques. Since all PWM DC-DC converters perform similar basic functions, the equivalent circuit models have the same form. Consequently, the canonical circuit model of Figure 3.14 can represent the physical properties of PWM DC-DC converters. The primary function of a DC-DC converter is the transformation of dc voltage and current levels, ideally with 100% efficiency. This function is represented in the model by an ideal dc transformer, denoted by a transformer symbol having a solid horizontal line. The dc transformer model has an effective turns ratio equal to the quiescent conversion ratio $M(D)$. It obeys all of the usual properties of transformers, except that it can pass dc voltages and currents. Small ac variations in the source voltage $v_g(t)$ are also transformed by the conversion ratio $M(D)$. Hence, a sinusoidal line is added to the dc transformer symbol, to denote that it also correctly represents how small-signal ac variations pass through the converter. The way it works is by ignoring the switching ripples and switching harmonics. Then, by averaging all the waveforms, the switching harmonics will be removed. To remove the switching ripples it is suffice to average the waveform over one switching period.

Linearization and constructing a small-signal converter model is the approach to avoid solving the nonlinear equations. The canonical model is a general model that can be used for representing the DC-DC converter modeling. This is a small-signal equivalent circuit that models dc-dc converter dynamics and transfer functions and it is shown in Figure 3.14.

Small ac variations in the duty cycle $d(t)$ excite ac variations in the converter voltages and currents. This is modeled by the $e(s)d$ and $j(s)d$ generators in Figure 3.14. In general, both a current source and a voltage source are required. Canonical

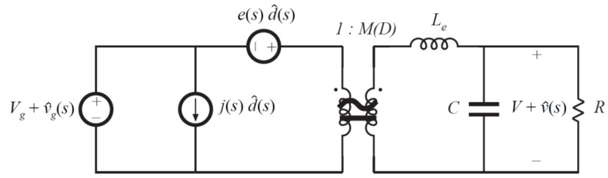


Figure 3.14: The canonical model for DC-DC converters

model parameters for the ideal buck converter are $M(D) = D$, $L_e = L$, $e(s) = V/D^2$, and $j(s) = V/R$. Using this model, the transfer function from input to the output can be calculated. And the stability of the feedback network can be analyzed based on this transfer function as well. In addition, this is used for designing the lead/lag compensation networks of the feedback loop [29]. The details of this approach is described in Chapter 4.

It is worth mentioning that the switching power supplies work in two distict modes of operationss: Contunuous conduction mode (CCM), and discontinuous conduction mode (DCM). For each specific desing and based on a desired application, the circuit should only work under one of these two modes of operation. Here in this work the assumption is that the converter works in CCM.

3.4.1 Voltage Mode vs. Current Mode

Current-mode control has been widely used in the power converter design. The fundamental difference between voltage-mode control and current-mode control is the PWM modulation. In voltage mode control, as shown in Figure 3.15, a fixed external ramp is used to compare with the control signal v_c to generate the duty cycle in the PWM modulator. However, in current-mode control, as shown in Figure 3.16, the sensed inductor-current ramp is used in the PWM modulator. Here two-loop structure has to be used in current-mode control.

There are many different ways to implement current-mode control. The active switch current which is part of the inductor current is sensed usually with a current transformer or resistor in series with the active switch. During the on-time period, the active switch current is the same as the inductor current, so peak current

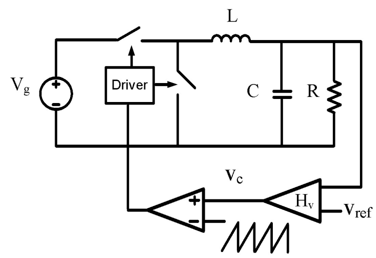


Figure 3.15: Voltage-mode control structure

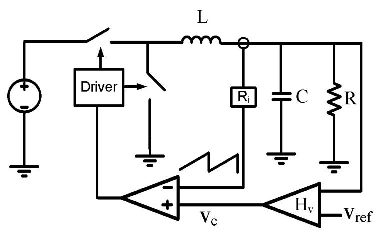


Figure 3.16: Current-mode control structure

protection can be achieved by the limited value of the control signal v_c. Different modulation schemes in current-mode control were summarize in [34–37], including peak current-mode control, valley current-mode control, constant on-time control, constant off-time control, and hysteretic control, average current-mode control. Here in this work, the other consideration lies on the inclusion of data transmission to the system. So a feedback mechanism is needed to attain the constant current while applying the data signals. As a result, the voltage mode control is hired for monitoring the voltage across the LEDs and a peak current control mechanism is utilized for controlling and regulating the current through the LEDs. The details of this is explained in more details in next chapter.

3.5 Conclusion

Amplitude-mode and PWM-mode are the two common trends in driving the LEDs. In amplitude-mode, a constant current is flowing through the LED and the dimming is achieved by tuning this constant current. The issue in using amplitude-mode is color shift and the PWM-mode is preferred to avoid color variation at different dimming levels. As the peak current is fixed in the PWM-mode and the dimming is done by tuning the duty ratio, the LED color is not affected. Using either amplitude-mode or PWM mode, it is needed to stabilize the LED current by implementing current regulation and either the linear regulator or switching DC-DC converters can be used. In the design of a regulator, it is important to find an appropriate solution and to meet performance requirements, including high efficiency, accurate output regulation, and fast transient response. Depending on the specific application, either a linear regulator or a switching mode regulator can be used. The linear regulator has been widely used by industry for a very long time. A major drawback of using linear regulators can be the excessive power dissipation in the pass transistor. LDOs are low noise, low cost, easy to use and provide fast transient response. If output voltage is close to the input voltage, an LDO may be more efficient than a switching regulator. However, efficiency is usually low when output voltage is much lower than input voltage. In general, linear regulators (or LDOs) have low voltage ripple and fast transient response. High efficiency as well as low power dissipation is the main reasons for selecting switching regulator instead of linear regulators or LDOs. In switching regulators, the transistor operates as a switch; therefore these regulators are usually much more efficient than linear regulators. However, the design and optimization of them are more challenging. The control method in switching regulator is based on either voltage mode or current mode control. In voltage mode control, only one control loop is used to regulate the output voltage. Current mode control uses two feedback loops; a voltage loop similar to the control loop of voltage mode, and a current loop that feeds back the current signal into the control loop. The current mode control scheme solution needs to sense the current precisely and is sensitive to switching noise. Selection of voltage or current mode control depends on the desired application.

Chapter 4

LED Driver Circuit Architecture Design Enabling Concurrent Data Transmission and Dimming Control for VLC

4.1 Intoduction

The emergence of the white LED presents an opportunity to extend the reach of optical signals for the VLC applications. The global quest towards energy-efficient solid-state lamps opens new possibilities for architectural lighting systems, consisting of networked solid-state lamps with multi-variable distributed control, adaptive features to alter color quality temperature, and high-speed data transmission.

The emergence of non-traditional, disruptive illumination applications for LEDs introduces new challenges in the development of driver circuits. For VLC, driver circuit compatibility with standard PWM dimming control methods plays a crucial role [38].

The light modulation capability of LED devices and its fast switching has produced considerable interest in the use of solid-state illumination systems for data communication. Achieving this goal is not possible without an optical transmitter, which has the capability of transmitting data while providing and maintaining user-defined brightness control. This chapter presents an LED driver design suitable for data transmission and dimmable illumination control [39–41]. In this chapter we have presented two distinct methods of data modulation and dimming control. First one is digital dimming presented in section 4.3 in which dimming is achieved using the binary bit settings and we have used the $0.5\mu m$ CMOS process for digital multiplication of these dimming signals with modulation signals. The second method is analog dimming which is designed and implemented in $180nm$ CMOS process and presented in section 4.4. In this method, we have used the analog dimming for generating the PWM dimming signals to be digitally combined with the base-band (digital) modulation signals. Moreover, this analog dimming method provides better and more precise control of data in the off-time of the PWM dimming signal.

4.2 Commercial LED Driver's Conflict with VLC

The growing adoption of LEDs as a lighting source has driven the great demand in a design of efficient integrated LED driver. To comprehend the obstacles of designing an LED driver chip, it is needed to understand the key requirements of LEDs operation. LED's forward voltage needs to be monitored due to its variation with current and temperature. Off-the-shelf LED drivers are unable to transmit data signals in the VLC system due to their large footprint of passive components and bandwidth limited control loops used for current regulation. The conventional LED driver design incorporates circuitry to provide a constant supply voltage and current regulation of LED devices. The most common method for this regulation is applying the DC-DC switching power supply to the LED driver circuitry which not only drives the biasing needs of LEDs but also takes care of its current regulation. The DC input-output voltage relationship for the LED driver, then, is related to the duty ratio of the applied switching signal; a small change in this ratio will be seen as a large change in the output voltage. A control mechanism, as a result, is needed to compensate this issue and provide the constant output voltage; utilizing the negative feedback loop allows a dynamic change in the switching signals duty ratio for getting a constant output. This control method works for lighting, but it introduces some constraints for communication purposes. First, there is a constraint on the switching frequency (f_s) due to the fact that the higher the switching frequency the higher the switching losses and the lower the efficiency. Second, the circuit formed by the DC-DC converter elements introduces a resonant frequency (f_0) that should be kept lower than the switching frequency for feedback loop stability. This resonant frequency which is determined by the passive components has the approximate value in the kHz range due to the large values of inductor and capacitor. These values need to be large enough to suppress the fluctuations in the inductor current and capacitor voltage. The third aspect of this constraint is that the feedback control loops bandwidth is set to be a fraction of the resonant frequency. Based on these three facts, the overall bandwidth of the feedback loop is limited. Using the compensator circuit design such as lead or lag or any other advanced compensating methods, the bandwidth of the feedback loop can be extended to some extent, but as mentioned earlier it cannot go beyond is the switching frequency [29].

Assuming an acceptable compromise, this rigid trade off among bandwidth, switching loss and ripple rejection, restricts applying this structure into the VLC systems and this low bandwidth limits the data modulation rate of VLC transmitters using commercial LED driver architectures. This limit, indeed, comes from applying the negative feedback in order to achieve a constant output voltage. Having some other formats of controlling and regulating the output voltage might not introduce this firm constraint; applying the feed forward method is one possible solution which can turn the bandwidth problem around at the expense of introducing sophisticated and expensive control methods. The proposed methodology is based on finding a solution with a minimum expense and maximum efficiency. The LED driver board designed to address these considerations is presented in section 4.4.

As stated above, LEDs are current driven devices and luminous intensity of LEDs is typically controlled by its forward current. As mentioned in chapter 3, the peak emission wavelength of LEDs tends to shift with the forward current, which can lead to color variations at different dimming levels. This makes the amplitude-mode diming method unsuitable as the forward current needs to be modified for grasping various dimming levels. In PWM, on the other hand, since the peak current level is kept constant, the control of dimming level does not affect the LEDs color. With better chromaticity control and flexibility for dimming, the PWM dimming technique is preferred where dimming is required at the expense of poorer luminous efficiency [42, 43]. In addition to the dimming capability, an LED driver to be used for the VLC systems has to support the data transmission capability as well. The combination of data transmission with the dimming control is implemented in the digital and analog domain which are described in details in the following sections.

4.3 A Digitally-controlled, Bi-level CMOS LED Driver Circuit

This section presents a novel LED driver circuit architecture incorporating digitally-controlled analog circuit blocks to deliver concurrent illumination control and serial data transmission. To achieve this goal, a bi-level pulse-width modulation (PWM) driving scheme is applied to enable data transmission during the off period of the LED drive current. With 3-bit PWM dimming resolution, the driver circuit enables linear luminous intensity control from 5% to 100%. Psuedo-random binary sequences (PRBS) are generated to compare circuit performance for various data modulation formats. The LED driver circuit is simulated in a $0.5\mu m$ CMOS process and exhibits a worst-case power consumption of $100mW$ with $33mA$ peak PWM current. The novel LED driver circuit architecture presented in this work performs concurrent illumination control and data transmission based on 3-bit PWM digital control signal. Uninterrupted serial data transmission is enabled during the PWM off-time by implementing a bi-level drive current scheme [39].

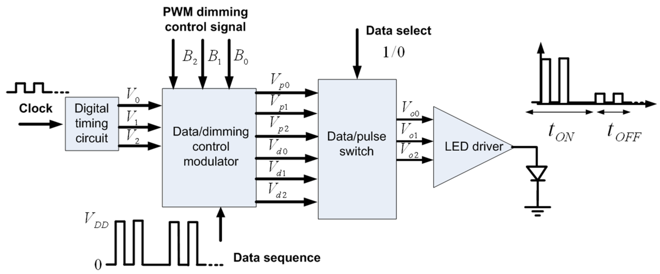


Figure 4.1: A digitally-controlled LED driver circuit block diagram

4.3.1 Analysis and Design of LED Driver Architecture

Figure 4.1 shows the schematic of the proposed design, which is composed of digital and analog circuit blocks. The circuit is controlled by a 3-bit PWM dimming control signal (B_0, B_1, B_2), which sets the degree of brightness.

The PWM symbol 001 corresponds to the lowest illumination level and symbol 111 corresponds to maximum brightness. The digital timing circuit block generates three reference pulse waveforms (V_0, V_1, V_2) to enable 8 levels of PWM modulation based on the input clock signal frequency. The data/dimming control modulator circuit block generates voltage waveforms combining a modulated data sequence with the PWM dimming control signal. This circuit block also generates a scaled data sequence during the PWM pulse off-times (t_{off}) in order to enable uninterrupted data transmission. The digital timing circuit and data/dimming control modulator circuit are both digital blocks, composed of logic gates, switches, buffers, and delay circuits. The outputs of the data/dimming control modulator circuit are divided into two different groups of waveforms based on the presence of an input serial data sequence. The first group (V_{d0}, V_{d1}, V_{d2}) is a set of dimming waveforms generated when the "Data select" signal is enabled; and the second group (V_{p0}, V_{p1}, V_{p2}) for "Data select" disabled. The output signals from the data/ pulse switch (V_{o0}, V_{o1}, V_{o2}) circuit block drive an analog LED driver stage, which generates variable current pulses to control the LED average forward current.

4.3.2 Digital Timing Circuit

This digital unit generates three distinct digital reference pulse waveforms (V_0, V_1, V_2) with different duty ratios based on the 3-bit PWM dimming control signal (B_0, B_1, B_2). In PWM mode, the average LED current is given by 4.1

$$\overline{I_f} = DI_H = \frac{t_{ON}}{T} I_H \tag{4.1}$$

where $\overline{I_f}$ is the average forward current , D is the duty cycle, ton is turn-on time and T is the switching period. The LEDs luminous intensity is proportional to the average current. The equivalent duty cycle D is given by (4.2).

$$D = \frac{1}{2^3}(2^0 B_0 + 2^1 B_1 + 2^2 B_2) \tag{4.2}$$

The duty cycle for each reference pulse waveform V_0, V_1 and V_2 is derived from the PWM control bits B_0, B_1 and B_2, respectively. Expressions for waveforms V_0, V_1 and V_2 are given in Equations 4.3, 4.4 and 4.5, where $\oplus$ is the symbol for the XOR function. *Clockdelays* 1, 2 and 3 are set to achieve a desired on-time period for each waveform as shown in Figure 4.2. The Delay signal in Equation 4.4 is used for pulse timing synchronization of V_1 relative to V_0 and V_2.

$$V_0 = (clock \oplus clockdelay1) \tag{4.3}$$

$$V_1 = (clock \oplus clockdelay2) + Delay \tag{4.4}$$

$$V_2 = (clock \oplus clockdelay3) \tag{4.5}$$

In this design, the delay pulses are generated using a cascade of inverter stages. In Figure 4.2, t_d is the period of the reference clock signal.

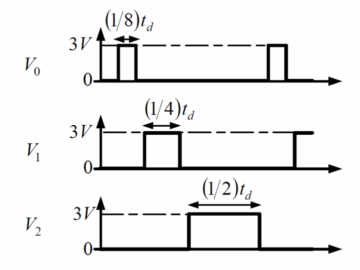
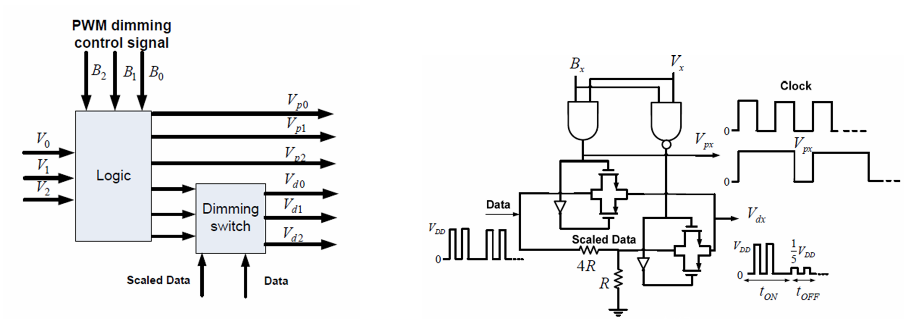


Figure 4.2: Output waveforms of the digital timing circuit

4.3.3 Data/Dimming Control Modulator

Figure 4.3 presents the data/dimming control modulator circuit. This circuit block is composed of logic circuits and CMOS switches as shown in Figure 4.3(a). The schematic view of a single branch is shown in Figure 4.3(a). Signal B_x represents the 3-bit PWM control signal (B_0, B_1, B_2) and V_x, V_{dx} and V_{px} are signal waveforms corresponding to input and output signals for each identical branch of the circuit. A dimming switch is implemented using the parallel combination of NMOS and PMOS transistors and two resistors are used to pass data during the PWM off-time period. The logic unit is composed of AND and NAND gates. The AND gate generates PWM waveforms with varying duty cycles based on the PWM control bits. The reference timing signal (V_x) passes through the switch if the corresponding dimming control bit is set HIGH. Thus, PWM signals corresponding to the predefined values of B_0, B_1, and B_2 will appear at the output of the AND gate. To generate a PWM waveform combining modulated data, the circuit generates a scaled version of the input data sequence using a resistor-divider network, as shown in Figure 4.3(b). The NAND gate enables a scaled version of the input data sequence to pass through the switch during the PWM off-time period. The resistors are implemented using gate-controlled transistors operating in linear-mode, enabling variable control of the scaled data voltage amplitude. The resulting drive signal waveform consists of the data pulses with maximum amplitude during the PWM on-time and scaled amplitudes during the off-time. The scaled amplitudes are set to achieve an adequate signal level to drive the final analog driver stage. The minimum signal amplitude



(a) block diagram

(b) circuit schematic for one branch

Figure 4.3: Data/dimming control modulator circuit

is a function of the threshold voltage of the input transistor in the following stage. The data/pulse switch circuit is composed of three switches. This unit will pass V_{dx} waveforms to the output only if the data select signal is set High.

The final stage is an analog LED driver circuit composed of three identical NMOS transistors (M_{n0}, M_{n1}, M_{n2}) and a current mirror circuit (M_{P1}, M_{P2}), as shown in Figure 4.4. The NMOS transistors generate current waveforms (I_{d0}, I_{d1}, I_{d2}) proportional to the voltage waveforms V_0, V_1, and V_2, produced by the data/dimming control modulator circuit. The three parallel, current waveforms are summed at the transistor drain node and mirrored to form the LED forward current given by Equation (4.6).

$$I_{LED} = \frac{(\frac{W}{L})_{MP2}}{(\frac{W}{L})_{MP1}}(I_{d0} + I_{d1} + I_{d2}) \tag{4.6}$$

where $\frac{W}{L}$ is the aspect ratio of the transistor. The transistor current is given by (4.7).

$$I_{dx} = \frac{1}{2} g_{mx}(V_{ox} - V_{th}) \tag{4.7}$$

where g_m is the transistor transconductance, and V_{th} is the threshold voltage. The resulting LED current waveform is linearly proportional to sum of the driving voltage waveforms.

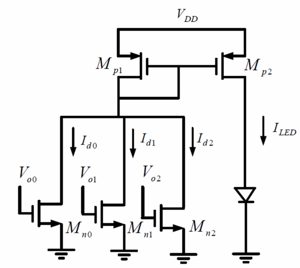


Figure 4.4: Analog circuit schematic of digitally-controlled LED driver

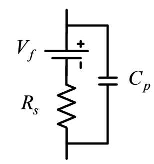


Figure 4.5: LED electrical model

4.3.4 Simulation Results of Digitally-Controlled LED Driver

For simulation results, the electrical equivalent model of the LED is used, as shown in Figure 4.5. In this model, the series voltage is $1.5V$, the series resistance is 10Ω, the shunt parasitic capacitance is $10pF$ and the supply voltage (V_{DD}) is $3V$. This series resistance was calculated using the I-V characteristic of a typical LED at a particular LED forward voltage. For simulation, the input PWM control bits are set to $B_0 = 1$, $B_1 = 0$, $B_2 = 1$ to achieve a brightness level of approximately 70%.

In order to simulate the effect of the data modulation scheme on the average LED current, a $2^{31} - 1$ PRBS is generated in MATLAB. The bit pattern was modulated using three different schemes: Non Return-to-zero (NRZ), Return-to-zero (RZ), and Manchester coding. The MATLAB-generated bit pattern was imported into the Cadence integrated circuit design tool for circuit simulation using 0.5μm CMOS transistor model files. Figures 4.6 - 4.9 present the input data waveform and resulting LED current for each data modulation scheme. The resulting waveform corresponding to the absence of an input data sequence is shown in Figure 4.9 for comparison.

The Table 4.1 shows the summary of the designs specifications. A data rate

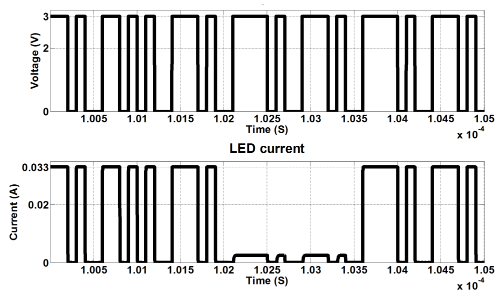


Figure 4.6: LED current waveform for NRZ data modulation

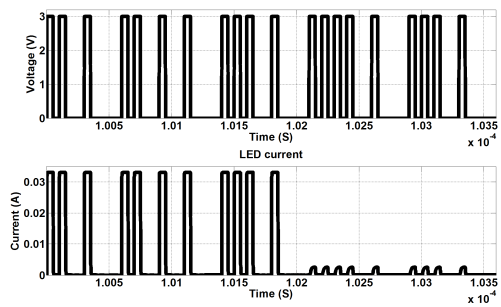


Figure 4.7: LED current waveform for RZ data modulation

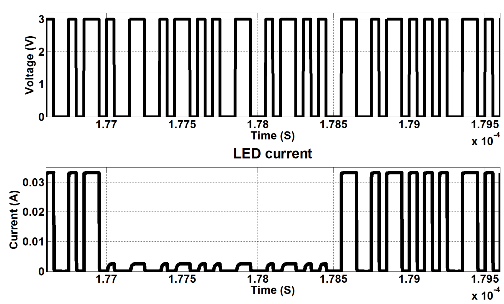


Figure 4.8: LED current waveform for Manchester coding

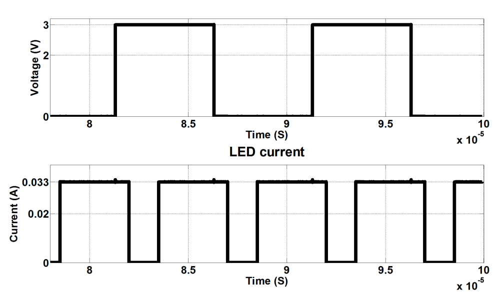


Figure 4.9: LED current with no data

Specifications of bi-level LED driver			
Resolution	Pulse frequency	Data rate	Power
3 Bits	100kHz	10Mbps	100mW

Table 4.1: Summary of proposed design

LED average current in different schemes mA				
Bits	NRZ	RZ	Manchester	No Data
111	17.17	8.69	16.51	32.57
110	15.05	7.58	14.34	28.02
101	12.69	6.36	12.06	23.19
100	10.57	5.26	9.86	18.65
011	7.85	3.90	7.64	14.01
010	5.69	2.79	5.45	9.37
001	3.37	1.57	3.18	4.64
000	1.21	0.46	0.98	0

Table 4.2: LED average current in different schemes

of 10Mbps was chosen for initial demonstration of the circuit functionality. With CMOS device transition frequencies reaching well beyond 100GHz, the speed of this driver circuit implementation is only limited by the inherent bandwidth limitation of the LED device. In Table 4.2, the average LED current is compared for each modulation scheme for all combinations of dimming control bits B_0, B_1 and B_2.

Figure 4.10 plots the average LED current versus the duty cycle for each modulation scheme. As expected, RZ coding drastically reduces the average current. Manchester coding exhibits the highest degree of linearity versus duty cycle. As the scaled data is sent during the PWM off-time, the scaled-data amplitude limits the lowest brightness control during off-time. In this design according to the results of Table 4.2, the brightness control is variable from 5% to 100%. For a peak current of 33mA, the worst-case circuit power consumption is only 100mW from a 3V power supply [39].

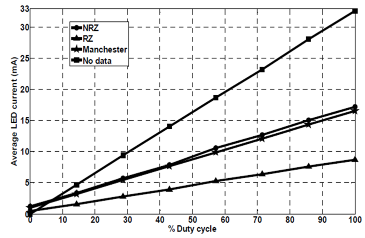


Figure 4.10: Average LED current versus duty cycle

4.4 LED Driver Circuit Architecture Utilizing Analog Dimming

This section presents an LED driver circuit architecture, incorporating analog and digital circuit blocks to deliver concurrent dimming control, and data transmission. This is achieved by independent control of output voltage and current using buck converter and current control loops, respectively. This is a design than can be applied to transform off-the-shelf LED drivers into optical transmitter circuits for VLC applications. It also has the capability of sending data signals in the format of NRZ, PPM and PWM and concurrently providing dimming control from 10-90%. Operation is linear and flicker-free by implementing a negative feedback loop to control the maximum amount of current passing through the LEDs. Control blocks are integrated in a $1.5{\times}1.5mm^2$ integrated circuit implemented in a $180nm$ CMOS process. The overall control circuit power consumption is $5mW$ and does not significantly degrade the overall driver efficiency. The driver efficiency is 89% at an LED driver current of $120mA$.

4.4.1 Introduction

This integrated system incorporates the feedback mechanisms to provide uniform light output together with the peak current control, which also prevents flickering. The proposed architecture is flexible enough to take any digital base band modulation format. Designed and implemented in a $180nm$ CMOS process, it provides linear $10\% - 90\%$ dimming control while transmitting data. It also introduces a

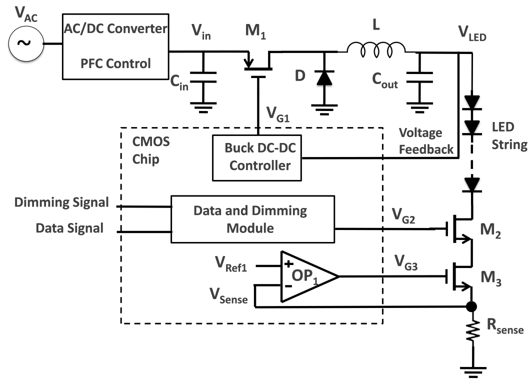


Figure 4.11: Block diagram of LED driver utilizing analog dimming

mechanism which can be applied to the off-the-shelf LED drivers and make them applicable for the VLC applications. The power consumption of on-chip circuitry, is negligible compared to the overall power consumption which yields an efficiency of 89% at $120mA$ of load current. The measured bit error rate (BER) varies from 10^{-6} at the data rate of 2.5Mbps to 10^{-3} at the data rate of 5Mbps. All control functions integrated on-chip with the total power consumption of $5mW$ [40].

In the design of LED drivers for VLC applications, the capability of sending data while maintaining the luminous control is a necessity. Two methods of PWM and changing modulation depth can be used for brightness control to have both dimming and data communication. Variable pulse position modulation (VPPM) is another candidate; VPPM symbols are determined by their positions and for dimming purposes the duty cycle of each symbol will be modified accordingly [44]. All these methods are under the definition of base band or line code modulation formats. Sending data while providing the appropriate dimming level is the main challenge regarding the design of the LED driver circuit. The proposed design depicted in Figure 4.11, is capable of taking any of these data formats and applying the dimming control as well. According to the bandwidth discussion of the DC - DC converter based driver, the commercial LED drivers have not yet been customized to be used for the VLC applications. According to the frequency response of the switching power supplies and due to the low 3dB bandwidth of the control loop, data cannot be transmitted through the feedback loop.

4.4.2 Buck Converter Design

The buck converter is a DC-DC converter used to step down the voltage and provides a regulated dc voltage. For the design of the proposed LED driver, the buck converter is used for the DC-DC conversion mainly due to the fact that for most VLC applications the input power comes from the mains and in the case of low voltage high current LEDs, a high to low power conversion is needed. Based on the Figure 4.11, this buck converter is composed of switches (MOSFET M_1 and schottky diode D) and passive components (L and C_{out}). The steady state output voltage of the buck converter for a given duty ratio (D_r) of the PWM signal (V_{G1}), is calculated as:

$$V_{out} = D_r V_{in} \tag{4.8}$$

A feedback mechanism is needed to compensate for changes in D_r to guarantee a constant output voltage. To meet this goal, an on-chip buck controller circuit is implemented as shown in Figure 4.11. The transistor-level schematic of the buck controller circuit depicted in Figure 4.12(a) includes voltage dividing resistors, R_{F1} and R_{F2}, to map the desired output DC voltage to the fixed reference voltage, V_{Ref2}. The negative feedback loop ensures that the output voltage is regulated based on the value of resistors R_{F1} and R_{F2}. The compensator circuit shapes the frequency response of the voltage feedback loop to maintain stability. The comparator block compares the output voltage of the error amplifier OP_2, V_O, with a 300kHz ramp signal, $Ramp_1$, to produce the buck converter control signal, V_{G1}, which has a P-WM waveform shape. As the buck converter output voltage, V_{LED}, swings above the reference voltage V_{Ref2}, the comparator output voltage falls, generating a PWM signal with smaller duty cycles. This duty cycle variation will affect the average time that the power MOSFET M_1 is turned on. This action forces the buck converter output voltage, V_{LED}, to drop until it reaches the desired value of $20V$. The circuit operates in a similar manner when the output voltage swings below the reference voltage. The buck converter is designed to provide $120mA$ of current at the regulated output voltage of $20V$, with settling time of $120\mu s$. The open loop gain of the buck converter can be written as (4.9).

$$T(s) = G_c(s)\frac{1}{V_M}G_{vd}(s)H(s) \tag{4.9}$$

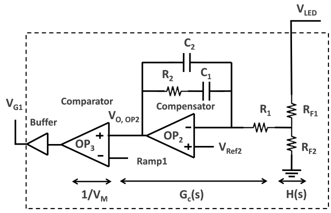
In equation 4.9, $G_c(s)$ is the transfer function of the compensator;($\frac{1}{V_M}$) is the gain of the pulse width modulator; V_M is the peak value of the ramp signal applied to the input of comparator; $G_{vd}(s)$ is the transfer function of power section; and $H(s)$ is the sensor gain, as shown in Figure 4.12(a). The transfer function of the power section composed of L, C_{out} and the load is calculated as (4.10).

$$G_{vd}(s) = \frac{1}{1 + \frac{s}{Q\omega_0} + (\frac{s}{\omega_0})^2} \tag{4.10}$$

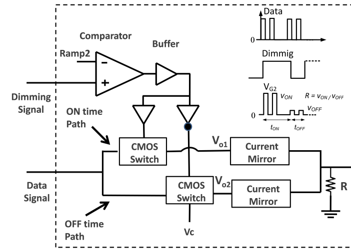
where $\omega_0 = (\frac{1}{\sqrt{LC_{out}}})$, $Q = R\sqrt{(C_{out}/L)}$, R is the equivalent load defined as (V_{LED}/I_{LED}), and $H(s)$ is a fixed value proportional to the values of R_{F1} and R_{F2}. With the assumption of no compensating circuit, the open loop gain of Equation (4.8) can be rewritten as (4.11).

$$T(s) = \alpha\frac{1}{1 + \frac{s}{Q\omega_0} + (\frac{s}{\omega_0})^2} \tag{4.11}$$

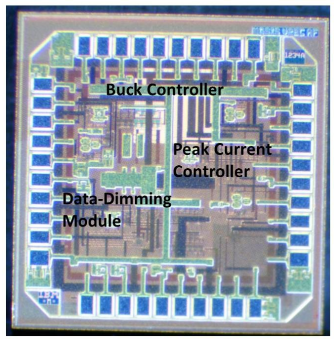
where α is a constant and is the multiplication of pulse width modulator and sensor gain. Values of α, Q, and ω_0 are selected in order to provide appropriate filtering and satisfy ripple requirements needed for the LED supply voltage, V_{LED}. It also forces the bandwidth of this transfer function, $T(s)$ in Equation (4.11), to be limited in the kHz range due to the large values of L and C_{out}. The phase margin of this open loop transfer function is low based on the selected values of α, Q, and ω_0 and this loop is prone to instability [29]. To avoid reaching instability, a compensation method is required, such as dominant pole, integrator, lead, or lag compensation. The compensator based on integrator and lead method, shown in Figure 4.12 and Figure 4.12(c) , is proposed for this work and its transfer function is given by (4.12).



(a) Buck DC-DC controller block diagram



(b) Data and Dimming block diagram



(c) Chip micrograph

Figure 4.12: Chip block diagrams and its micrograph

$$G_c(s) = \frac{1 + s(R_2C_1)}{sR_1C_1(1 + \frac{C_2}{C_1} + s(R_2C_2))} \tag{4.12}$$

In this proposed compensator, the system zero $(1 + s(R_2C_1))$ is set equal to the resonant frequency $f_0 = (\omega_0/2\pi)$, to achieve a high phase margin. Also the pole corresponding to C_2 is set to diminish the gain of the $G_c(s)$ at high frequencies by choosing the ratio of $C_2 \cong C_1/10$.

The LED driver circuit presented in this work overcomes the aforementioned bandwidth trade off by utilizing the independent control of the DC - DC converter output voltage and the data-dimming signal to control LED current. The key design feature presented here involves isolating the data signal from this voltage feedback loop, and apply it independently. The circuit components highlighted in the dotted region of the proposed LED driver in Figure 4.11 are implemented in a custom integrated circuit utilizing a $180nm$ CMOS process. The peripheral components are designed to be off-chip and a power factor correction (PFC) unit might be added to suppress the total harmonic distortions as well.

4.4.3 Data-Dimming Multiplication Method

In the proposed design, as shown in Figure 4.11, the control of the LED power supply voltage is achieved by the buck converter circuit block while a separate data-dimming circuit module provides control signals for LED current waveform shaping for data transmission. This technique can be hired for applying to the off-the-shelf commercial LED drivers and make them suitable for operating in the VLC systems. The data-dimming module shown in Figure 4.11 takes the dimming signal and generates its corresponding PWM signal. A digital multiplication method is employed to combine the PWM signal with the NRZ modulated data signal. The operational amplifier (Opamp) circuit OP_1, transistor M_3, and sensing resistor R_{sense}, in Figure 4.11, provide local feedback to maintain a constant average current through the LED for a given dimming level. This feedback also prevents flicker by controlling the amplitude of the LED's current. The amplitude is limited to a fixed value of V_{Ref1} divide by R_{sense}. The opamp circuit is the most energy hungry element of the driver circuit. To improve driver efficiency, a novel on-chip compensation technique for the opamp is implemented. This compensator provides a high phase margin and extends the 3dB bandwidth of the amplifier. This is achieved by generating the left hand plane (LHP) zero using the passive R-C network in the two stage trans-impedance amplifier. The combination of amplifier with its compensation design leads to a high gain-bandwidth, high slew rate design with the power consumption on the order of a few milliwatts ensuring the transmission of high data rate signals. The data and dimming module as depicted in Figure 4.12(a), is responsible for combining the PWM and data signals. The dimming signal sets the brightness level of the light. This dimming signal corresponds to a knob (dimmer) by which the user can set the dimming level. The PWM dimming signal is generated by the comparison of dimming signal dc voltage with a 100kHz ramp signal "$Ramp2$". The PWM dimming signal passes through the buffer and will be multiplied digitally with the incoming data signals utilizing CMOS switches (parallel combination of

NMOS and PMOS transistors). Here, as shown in Figure 4.12(b), two distinct sets of switches are employed, one of which operate over the on-time and the other over the off-time. Due to the nature of the PWM signal, where its value is zero in the off-time, data will be lost during this time. To prevent this destructive accident from happening, an uninterrupted data transmission technique is chosen to allow data transmission during the PWM off-time; this is done by implementing a two-level drive current scheme such that the LEDs do not turn off completely in the off-time of PWM signal and some fraction of data will be injected in this off-time; the amplitude of the signal in the off-time is smaller than the one in the on-time in order to provide the appropriate dimming levels. The ratio of this on-time signal to off-time signal is called R and the measurement results for different values of R are shown in the measurement results section. Selecting appropriate values for R is dependent on the dynamic range of the receiver and also the desired communication link range. Compared to the approach presented in [39], the circuit architecture presented in this work enables bi-level amplitude control, which is achieved with an external pin, V_c, as shown in Figure 4.12(b). This feature adds one degree of freedom to the circuit control by making the ratio of PWM on time signal to off time signal, R, under the user control. The output of the CMOS switches in both on and off-times will be converted to a current signal with the help of current mirrors and eventually this signal, V_{G2}, will be applied to the external MOSFET M_2 to drive the LEDs. The chip micrograph is shown in Figure 4.12(c) which is composed of buck converter controller, data-dimming module, and peak current control. Using this method data can be detected at all the times in the receiver while the dimming capability is in place. The components used for the efficiency calculation are listed in Table 4.4.

4.4.4 High Gain-Bandwidth and High Slew-Rate Two-Stage OTA

Opamps have found extensive applications in analog circuits and systems for communications, consumer electronics, controls and signal conversion. Two-stage Opamps with frequency compensation are popular for driving capacitive loads while ensuring sufficient gain and stability. Frequency compensation techniques have been evolving over the last decades in distinct applications. In particular, power-and-area-efficent two-stage Opamps capable of driving a wide-range capacitive load are demanded for low-dropout regulators (LDOs) or LCD-panel drivers. Capacitor multiplers (CMs) have emerged as one of the best solutions to implement such kind of Opamps [45]. In this section, a passive frequency compensation method is presented for the first time, which can be applied to two/multi- stages operational transconductance amplifier (OTA) designs, to achieve high gain-bandwidth (GBW) and high slew- rate with no increase in the overall power consumption. A nulling resistor with series compensating capacitor is applied in the first stage and extends the GBW by introducing a left-hand plane (LHP) zero. This design is implemented in a $0.18\mu m$ CMOS process and the measured results show a GBW of 100MHz and average SR of $60V/\mu s$ with a power consumption of $1.7mW$. A high figure of merit (FoM) of $94.7GHz.pF.V/\mu s/mA$ is achieved.

4.4.4.1 Compensation Techniques for Two and Three Stage Opamps

Opamps have been at the core of a wide range of analog circuits such as analog-to-digital converters, LDOs and active filters. Portable systems, as the wireless transceivers, integrate most of these functions, appealing for more high-performance Opamps to meet the increasingly tight power and area budgets. The conventional multi-stage Opamp topology (gain stages ≥ 3) does not appear as a wise choice since the frequency compensation leads to large reduction of the gain-bandwidth (GBW) product, and almost none of the published topologies are suitable for driving a wide range of capacitive load with low power consumption. On the other hand, a two-stage Opamp topology [Figure 4.13(a)] is selected as it exhibits more sensible and simpler tradeoffs among the DC gain, GBW, quiescent power and output swing. Two-stage Opamps also require frequency compensation to obtain a stable closed-loop operation. Four compensation schemes shown in Figure 4.13(b)(e) have been introduced mainly with the aim of eliminating the right-half-plane (RHP) zero as shown in Figure 4.13(a), rather than handling highly variable capacitive loads. To

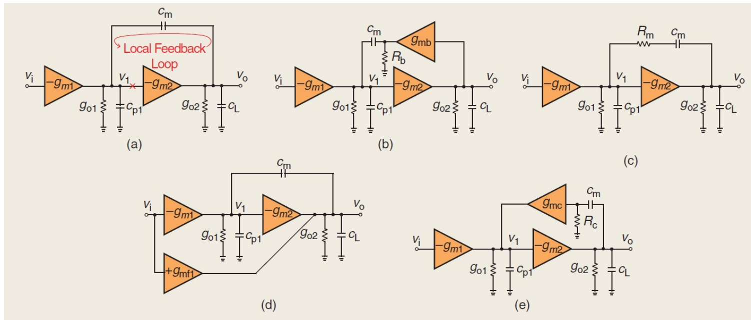


Figure 4.13: Compensation schemes for two stage OpAmps: (a) Simple Miller compensation (SMC), (b) Miller compensation with voltage buffer (MCVB), (c) Miller compensation with nulling resistor (MCNR), (d) Miller compensation with feedforward transconductance (MCFT), and (e) Miller compensation with current buffer (MCCB).

choose an optimum topology, the local feedback loops of these circuit structures can be interpreted as being able to cut the loops according to that in Figure 4.13(a). Comparing them, SMC, MCVB, MCNR, and MCFT have the same unity-gain frequency (UGF), while the UGF of MCCB is C_m/C_{p1} times higher than them under the same configuration of circuit parameters. High UGF of MCCB topology can be used to trade for small power and area. Therefore, MCCB is essentially more power-and-area efficient than other compensation schemes, though the capability of driving small capacitive loads is limited by the parasitic pole $(C_L + C_m)/(R_c C_L C_m)$ generated by the current buffer. Another issue associated with MCCB is related with the fact that when the capacitive load is heavy, in the order of hundreds of pF, the compensation capacitor C_m must be set to a large value for driving the load, and more importantly maintaining a reasonable gain of the first stage. Moreover, large C_m not only occupies a great amount of silicon area but significantly lowers the Opamp's slew rate. A feasible solution to overcome this difficulty utilizes capacitor multipliers (CMs), since CMs minimize the physical size of the capacitors while retaining the effective capacitance required. Many effective CMs have been proposed as well [45].

The operational transconductance amplifier (OTA), the basic building block in analog/mixed-signal VLSI systems, presents several design challenges to satisfy performance gain, bandwidth and power consumption tradeoffs. The OTA can be realized using a cascode topology where one or two transistors stack together in series to increase the overall output resistance and further increase the overall gain. As the supply voltage in advanced silicon processes continues to scale, this traditional cascode topology suffers from voltage headroom constraints that limit the overall dc gain. Multiple cascaded amplifier gain stages can be implemented to achieve both high gain and voltage swing. However, this design methodology is prone to instability. Indeed, each stage introduces a low-frequency pole which causes the easy reduction in the phase margin and pushing the amplifier to unstable region. Alleviating this problem comes with the cost of appropriate compensation techniques to guarantee the stability under the frequency range of interest. Miller compensation techniques are used to provide stability in closed-loop conditions. The original Miller compensation approach was based on placing a capacitor across the input and output of the second stage. This forward path connecting output of the first stage to the output of the second stage produces a right-half-plane (RHP) zero in the open-loop gain, which is an undesirable effect degrading the overall phase margin. Solutions that prevent the occurrence of a RHP zero have been proposed both for two-stage and three stage CMOS OTAs [46]. A systematic design procedure for compensation method is proposed in [47] which can achieve an efficient power optimized design. Most of the published compensating techniques in the literature are based on the Miller, nested Miller or reversed nested Miller compensation [46–52]. The two-stage OTA presented in this section, for the first time introduces a method of OTA compensation by placing a compensation network across the first stage. The proposed frequency compensation technique presented in this work introduces a LHP zero without consuming additional power. Designed and fabricated in a $0.18\mu m$ CMOS process, the simulation and measurement results together with a comparison summary are presented.

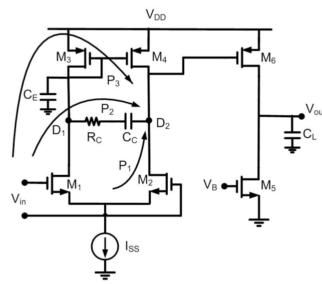


Figure 4.14: Circuit diagram of OTA with its proposed compensation method.

4.4.4.2 Design of compensation network

The circuit diagram of the proposed two-stage OTA is shown in Figure 4.14. The first stage of this OTA is composed of NMOS transistors M_1 and M_2, together with PMOS transistors M_3 and M_4 and the second stage is a common source (CS) amplifier composed of NMOS transistor M_5 and PMOS transistor M_6. In this figure, C_E is the equivalent capacitance at node D_1, C_L is the load capacitance; V_B and I_{SS} are bias voltage and current generated by the on-chip reference circuit. As depicted in Figure 4.14, there are three paths by which the signal can travel from input to the output, resulting in zeros in the transfer function. By placing the nulling resistor, R_C, in the second path, P_2, in series with capacitor C_C, a LHP zero is generated, which can be represented as (4.13).

$$Z_1 = \frac{1}{R_C C_C} \tag{4.13}$$

This LHP zero is used in this design to get a desired phase margin and to extend the GBW. The zero related to the third path, P_3, is a LHP zero represented as $Z_2 = 2g_{m3}/C_E$, where g_{m3} is the transconductance of transistor M_3. There is also one RHP zero due to the second stage equal to $Z_3 = g_{m6}/C_{gd6}$, where g_{m6} is the transconductance of transistor M_6. Both of these Z_2 and Z_3 zeros are high enough that their effect on the frequency response can be ignored. In order to see the effect of the zero introduced by path P_2, the following inequality should be met:

$$C_C > C_E \tag{4.14}$$

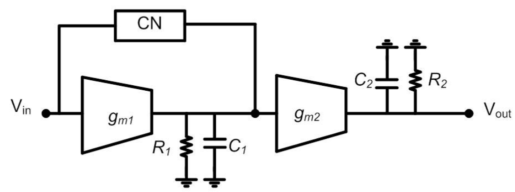


Figure 4.15: Block diagram of OTA with two distinct compensation networks

Considering the fact that the C_C and C_L capacitances are higher than all other parasitic capacitances, the voltage gain of the circuit is given as (4.15).

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}g_{m6}R_I R_L(1+sR_C C_C)}{(1+sR_L C_L)(1+sC_C(\alpha+R_C))} \tag{4.15}$$

where g_{m1} is the transconductance of transistor M_1; R_I is the equivalent resistance at the output of first stage at node D_2 in Figure 4.14, R_L is the equivalent resistance at the output node in parallel with the load, and α is given as $((1+2g_{m3}R_I))/g_{m3}$. Based on Equation (4.15), the dominant pole, at node D_2, is equal to $1/((C_C(\alpha+R_C)))$ and the pole at the load can be cancelled by the zero with correct tuning of $R_L C_L = R_C C_C$. It is worth mentioning that the exact matching of this equality is not required as long as the phase margin is more than 45^o. In this proposed design no compensation network (CN) is placed across the second stage. Figure 4.15 presents a block diagram view of the proposed two-stage OTA with a compensation network (CN) incorporated in both stages. The transconductance of the first and second stages is given as g_{m1} and g_{m2}, respectively. The CN can be implemented as a nulling resistor, voltage buffer or current buffer/amplifier. It is shown that the current amplifier and voltage buffer approaches are the best choice for moderate capacitive loads and higher capacitive loads, respectively [46]. In this work, a nulling resistor is employed as the CN of the first stage.

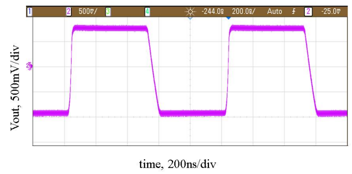
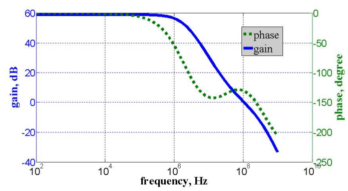
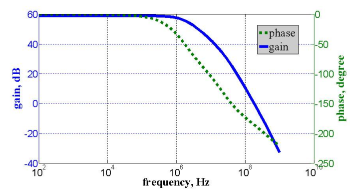


Figure 4.16: Experimental transient response with 15pF load.



(a) Result with compensation network composed of R_C and C_C



(b) Result without compensation network

Figure 4.17: Open-loop frequency response simulation results

4.4.4.3 Simulation and Measurement Results

The two-stage OTA with frequency compensation is designed and implemented in a $0.18\mu m$ CMOS process, which draws a total current of $950\mu A$ from a $1.8V$ supply. Figure 4.16 shows the transient response used to measure the slew- rate (SR). The average SR measured is $60V/\mu s$.

The measured gain and GBW are 60dB and 100MHz, respectively. The simulation results shown in Figure 4.17 are in agreement with the measured results.

The open-loop frequency response of OTA with frequency compensation is given in Figure 4.17(a) with the GBW of 100MHz and phase margin of 55^o. Figure 4.17(b) shows the open-loop frequency response without having the CN introduced by path P_2 in Figure 4.14. As depicted in this figure, the small phase margin moves the circuit into an unstable region. The chip microphotograph of this design is shown in Figure 4.18.

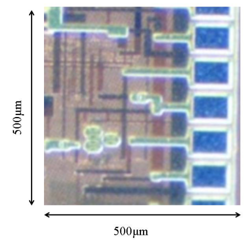


Figure 4.18: Chip microphotograph of the two-stage OTA.

4.4.4.4 Figure of Merit (FoM)

The two well-known FoMs presented in the literature are based on the product of GBW and C_L or the product of SR and C_L. In this paper FoM_1 is defined as $GBW.C_L/I_{DD}$, where I_{DD} is the dc supply current. To perform a comparison of various OTA compensation techniques independent of technology, a FoM which captures SR, GBW, C_L, and I_{DD} simultaneously is proposed as

$FoM_2 = GBW.SR.C_L/I_{DD}$. A comparison of the proposed circuit with state-of-the-art OTA designs is given in Table 4.3.

In summary, a novel compensation technique, based on passive frequency compensation of a two-stage OTA topology is presented to increase the GBW and slew-rate. The proposed design introduced a compensation network of series combination of R_C and C_C across the input and output of the first stage. A LHP zero is generated which helps to increase the overall GBW to 100MHz with the phase margin of 55^o at a load of $15pF$ and supply current of $950\mu A$. A new FoM is also introduced which is given by $GBW.SR.C_L/I_{DD}$. This proposed design has a superior FoM_2 of $94.7GHz.pF.V/\mu s/mA$.

4.4.5 Measurement Results of LED Driver with Analog Dimming

The LED driver should enable dimming control based on user settings, and also maintain communication link performance. The figure of merit (FOM) for this driver circuit is based on dimming linearity during data transmission. The data stream can take the form of any digital baseband modulation scheme, including

	[48]	[49]	[50]	[51]	[52]	**This work** [53]
GBW (MHz)	35	20	160	770	19.46	**100**
Gain (dB)	> 70	112	74	81	83.12	**60**
Phase margin (^{o})	> 45	58	NA	81	55.5	**55**
$I_{DC}(\mu A)$	91	491	201	2363	466	**950**
$C_L(pF)$	> 5.5	10	1.75	1	15	**15**
Average$SR(V/\mu s)$	19.5	17.5	26.8	NA	13.8	**60**
$FoM_1(MHz.pF/mA)$	2116	408	1393	326	627	**1578**
$FoM_2(GHz.pF.SR/mA)$	41.3	7.2	37.4	NA	8.7	**94.7**

Table 4.3: Performance summary comparison of different OTAs

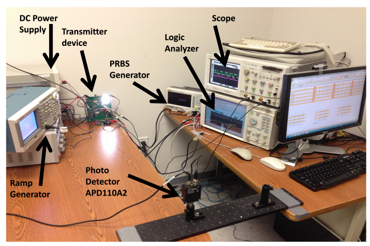


Figure 4.19: Measurement setup developed for optical characterization of the LED driver circuit

non-return-to-zero (NRZ), return-to-zero (RZ), Manchester coding, and pulse position modulation (PPM) signals. For the measurement purposes, a $2^7 - 1$ PRBS is generated and applied to the proposed LED driver. Dimming can be tuned based on the dimming signal input from 10% to 90%. Based on the measurement setup depicted in Figure 4.19, the measurements are performed at the link ranges of $30cm$, $50cm$, $70cm$ and $1m$. In Figure 4.19 which the link range is 1m, the VLC transmitter is biased using power supplies and the PRBS generator is connected to provide the appropriate signal which plays the role of data in this system. Moreover, this is used to measure the BER and to plot the eye diagram of the system, a mechanism commonly used to measure the speed of system.

A string of five LEDs (Cree $MLCAWT$) as the LED string in Figure 4.11, the control signals, LED current and the received signal, with the dimming ratio of %30 and link range of $30cm$, are depicted in Figure 4.20 together with its zoomed view of transient signals. The signal $V1$ and $V2$ are the V_{o1} and V_{o2} in Figure

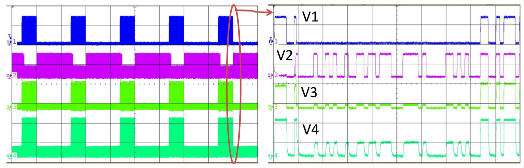


Figure 4.20: Transient analysis of the LED driver chip and its zoomed in view of transient signals with $2^7 - 1$ PRBS, NRZ modulated data signal and %30 dimming level. $V1$: is Vo1 in Figure 4.12(b), $V2$: is V_{o2} in Figure 4.12(b), $V3$: is Vsense in Figure 4.11 which is proportional to LED current, and $V4$: is the received signal using the $APD110A2$ commercial receiver

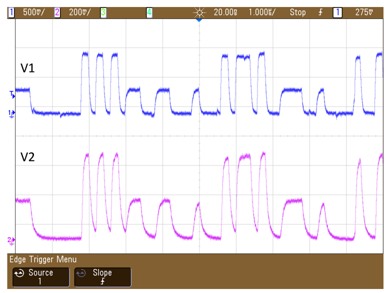


Figure 4.21: Measurement result at the link range of $50cm$ and dimming level of 60%, $V1$: V_{sense} in Figure 4.11 which is proportional to LED current, and $V2$: Output of commercial receiver, $APD110A2$

4.12(b), respectively. As it is shown in this figure, some portion of data is included in the off-time of the PWM waveform. Signal $V3$ is V_{sense} in Figure 4.11 which is proportional to the current through the LEDs. For this measurement a commercial Thorlabs $APD110A2$ photoreceiver is used. Signal $V4$ is the received signal detected using the $APD110A2$. These waveforms of Figure 4.20 for the link range of $50cm$ and the dimming ratio of 60% are depicted in Figure 4.21. As it is shown in this figure, the received signal resembles that of the transmitted data (proportional to the LED current), and consequently the data can be reconstructed as it is not lost during the off time of PWM signal.

The Agilent $16702B$ logic analysis system is used for calculating the BER of the system. The transmitted data sequence and the received signal at the output of the APD110A2 photoreceiver are both connected to the logic analyzer. The Sync output from the PRBS generator is also connected to the logic analyzer to provide a Clock signal. For measuring the BER, the digitized transmitted data and received

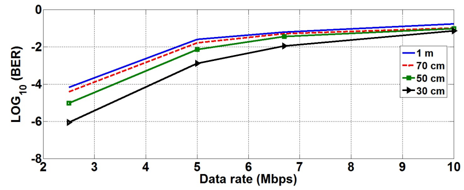
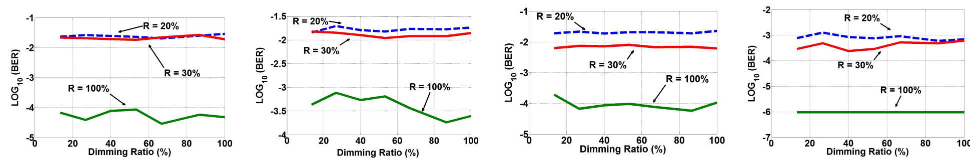


Figure 4.22: BER vs data rate for different link ranges



(a) (b) (c) (d)

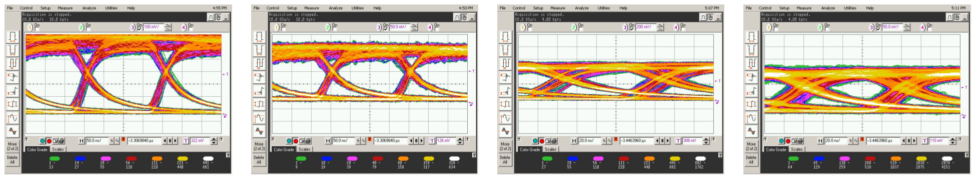
Figure 4.23: Variation of BER versus dimming ratio for 5Mbps data rate (R: ratio of on-time to off-time of PWM signal), (a) Link range of 100cm, (b) Link range of 70cm, (c) Link range of 50cm, (d) Link range of 30cm

signal are compared off-line for different values of data rates and different values of link ranges. The measured BER versus the data rate is depicted in Figure 4.22 for link ranges of 30cm, 50cm, 70cm and 1m. As shown in Figure 4.22, for the link range of 30cm, the BER varies from 10^{-6} at the data rate of 2.5Mbps to 10^{-3} at 5Mbps.

Figure 4.23 shows how the BER varies with the change in dimming ratio. In this figure R is the ratio of on-time to off-time of PWM signal. To have an uninterupted detection of data, some portion of data is placed inside the off-time of PWM signal to make it practical to detect data at all the times. There is a trade-off between BER, link range and brightness control based on the selection of R. In this design the value of 20% provides acceptable brighness control from 10%-90%.

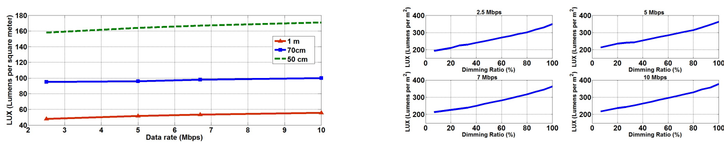
Figure 4.24 shows the eye diagram at data rates of 5Mbps and 10Mbps both for link ranges of 50cm and 1m.

While maintaining the data transmission, a LED driver should provide the uniform output light and a linear change of light based on the dimming levels. Figure 4.25 verifies this linear change of brightness level based on the dimming ratio and link range. Figure 4.25(a) shows the change of luminous flux (Lux) versus the data



(a) (b) (c) (d)

Figure 4.24: Eye diagrams: (a) Data rate of 5Mbps, link range of 50cm, (b) Data rate of 5Mbps, link range of 1m, (c) Data rate of 10Mbps, link range of 50cm, and (d) Data rate of 10Mbps, link range of 1m



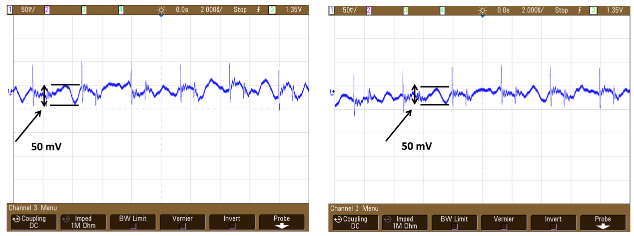
(a) (b)

Figure 4.25: Lux measurements: (a) Lux versus data rate (b) Lux versus the dimming ratio for different dara-rates at 30cm of link range

rate for link ranges of 50cm, 70cm and 1m. The inherent offset of Lux ($\cong$ 40Lux at 1m,$\cong$ 100Lux for 70cm and $\cong$ 160Lux for 50cm) is due to the non-zero value of PWM signal in the off-time of PWM signal. Figure 4.25(a) shows the change of Lux versus the dimming ratio. As it is depicted in this figure, the brightness varies linearly from 10%-90% for data rates of 2.5, 5, 7, and 10Mbps.

Figure 4.26 shows the fluctuations in the output voltage of the buck converter, V_{LED} (Figure 4.11). As it is shown in Figure 4.26(a) which shows the output voltage ripple at the dimming ratio of 30%, and in Figure 4.26(b) which shows the output voltage ripple at the dimming ratio of 70%, the peak-to-peak of this ripple is around 50mV. The tuned output DC of the buck converter is 20V. The resulting ratio of peak-to-peak ripple to the DC output voltage is 0.0025.

Table 4.4 summarizes the characteristics of the proposed LED driver. For efficiency calculation the losses due to the following components are considered: schottky diode (D), equivalent series resistance (ESR) of capacitor and inductor, MOSFETs, M_1, M_2 and M_3, (switching and conduction losses), series resistance of LEDs and sensing resistor (R_{sense}).



(a) (b)

Figure 4.26: Output voltage ripple: (a) 30% dimming level, (b) 70% dimming level

Chip performance					
Process	Area(mm^2)	On-chip consumption power(mW)	Dimming Ratio	Efficiency	Supply Voltage(V)
180nm CMOS	1.5 × 1.5	5	10%- 90%	89% @ $I_{LED} = 120mA$	1.8
Buck Converter performance					
LED	LED current(mA)	Settling time(μs)	$\frac{OutputRipple}{V_{LED}}$	Switching frequency (kHz)	$V_{in}/V_{LED}(V)$
Xlamp ML-C	120	120	0.002	300	25 V/20 V
R_1 ($M\Omega$)	R_2 ($k\Omega$)	C_1 (pF)	C_2 (pF)	R_{F1} ($M\Omega$)	R_{F2} ($k\Omega$)
1.2	128	100	10	2.12	100
M_1	M_2, M_3	R_{sense} (Ω)	L (μH)	D	C_{out} (μF)
$IRLMS5703PbF$	$2N7002$	5	33	$MSS1P5$	5

Table 4.4: Chip and buck converter perfomance

$$\eta = \frac{output\ power}{output\ power + totall\ losses} \tag{4.16}$$

The efficiency is calculated as output power to the summation of output power and the total losses as given in Equation (4.16).

The chip power consumption is also taken into account regardless of its negligible effect. Based on this calculation, the efficiency of the proposed LED driver is 89% at an LED drive current of $120mA$.

4.5 Conclusion

LED market has granted a great demand for the design of efficient integrated LED driver. Consequently, it is a necessity to make the Off-the-shelf LED drivers compatible with the data transmission capabilities in order for them to be used in various VLC based applications. The conventional LED driver design incorporates circuitry to provide a constant supply voltage and current regulation of LED devices. The design tradeoff between feedback loop bandwidth, switching losses, and ripple rejection put limitations on data modulation rates of VLC transmitters using commercial LED driver architectures. The driver circuit architecture presented in this chapter overcomes the modulation bandwidth limitation by providing a feedback control loop to maintain the DC-DC converter output voltage independently of the LED drive signal to control data modulation and dimming. The driver should be able to provide sufficient current and voltage levels and provide the dimming capability as well. In addition to the dimming capability, an LED driver to be used for the VLC systems has to support the data transmission as well. The combination of data transmission with the dimming control is implemented in the digital as well as analog domains and the details for both approaches are described in details in this chapter. Table 4.1 and 4.4 presents the summary of these two designs. Meeting the need of simultaneous data transmission and dimming control, it is always desired to achieve higher rates of data transmission. The following chapter presents a couple of bandwidth enhancement methodologies.

Chapter 5

Bandwidth Enhancement Techniques for VLC Networks

5.1 Introduction

LEDs are large area emitters and an array of them can be used for providing the required optical power. It is shown that the VLC channel has very high signal to noise ratio (SNR). Moreover, a level of illumination which is required for reading and writing ensures that the channel bandwidth is higher than the sources; thus the channel by itself does not limit the performance of the system [44]. The limiting factor, however, is the low bandwidth of LEDs as mentioned in previous chapters. This limitation is two sided; one is related to the optical and the other is related to the electrical domain. Rise and fall times are the two most significant factors contributing to the LED bandwidth limitations in the electrical domain, which in turn establish the maximum data rate the device is capable of handling. This electrical bandwidth limitation is emanated from the large value of parasitic capacitance of LED. Optical domain is the other side of LEDs bandwidth limitation. Total optical bandwidth is inversely proportional to the carrier lifetime or carrier recombination. This modulation bandwidth of an LED device can be increased by increasing the carrier concentration in the active region, with a simultaneous decrease of the carrier lifetime. This, however, has a negative effect on the LED overall optical output power. Therefore, a compromise between modulation bandwidth and power output must be reached during the design process. In a linear system or in a complex system with a built-in compensation network that the overall performance resembles a single pole system, the product of bandwidth and rise time is constant; analog or digital circuit design, then, can be used to shorten the rise or fall time and extend the overall bandwidth. Perhaps the simplest way of alleviating the low bandwidth problem of the transmitter which is due to the long decay time of the phosphor is to block its component at the receiver by using a blue filter; this can increase the bandwidth substantially with the cost of a small reduction in received power due to the filter losses. It is also possible to improve the overall optical response by using the transmitter or receiver equalization that can be used for compensating the rapid fall-off in response of the white LEDs at high frequencies; applying bandwidth-efficient modulation schemes that take advantage of the high available SNR is another approach [54]. In addition, for higher data rates it may be possible to use parallel data transmission from a number of LEDs. The concern in using the multilevel modulation techniques is LEDs nonlinear response. This nonlinear behavior is particularly important when analog modulating signal is used [55]. In most illumination applications many LEDs are used to provide the necessary lighting intensity; this offers the opportunity of transmitting different data on each device or on different groups of emitters. In order to implement this method, a detector array is required at the receiver, and this generates a multi-input multi-output (MIMO) system. Parallel communication which is known as optical MIMO, is yet another way of alleviating the VLC data rate challenge [56, 57]. There are different methods of increasing data rates, and a combination of these can be applied to get a better and more reliable performance. In this chapter the conventional methods of extending the bandwidth of LED drivers are reviewed and proposed topologies are introduced.

We have designed and implemented a number of bandwidth enhancement techniques to be used for the VLC applications. These techniques are negative impedance converter (NIC), equalization, pulse shaping, peaking, pole-zero cancellation, time-interleaved LEDs, and 4-level PAM. In this chapter these seven methodologies are described in detail and the measurment results are provided. In section 5.2, the concept of NIC is reviewed and two different modes of fixed and floating structures with their corresponding proposed LED drivers are introduced. Second method is explained in section 5.3; in this section a literature review about different equalization techniques such as multiple resonant, pre and post (as well as active and passive) equalization, and the role of complex modulations such as OFDM/DMT in enhancing bandwidth is presented and later on our work on first-order passive post-equlization implementation is described. Third method is pulse shaping prsented in section 5.4; in this section, the carrier sweep out technique for decreasing the rise and fall times is reviewed and our work on pulse shaping circuit is presented which enhances the overall bandwidth of the VLC link by shortening the rise and fall times. The fourth method is peaking presented in section 5.5; different peaking techniques such as shunt, series, (bridged) shunt-series and triple resonant peaking techniques are reviewed and then our work on developing a new peaking technique, bridged-shunt-zero peaking, along with an LED driver based on this proposed peaking is introduced. The fifth method is pole-zero cancellation described in section 5.6; in this section our work on using pole-zero technique for extending the bandwidth is explained and then the proposed LED driver with enhanced bandwidth using the pole-zero cancellation methodology is presented. Sixth method is time-interleaved utilized for compensating the low bandwidth of LEDs which is explained in section 5.7. In this method, we have developed a scheme in which each binary input is sent with a fixed delay and with processing the received signal a data rate of 100Mbps is achievable with low 10MHz LEDs. Finally, seventh method is 4-level PAM which is presented in section 5.8. We have shown that using 4×4 array of LEDs, the data rate can be increased by 4 times.

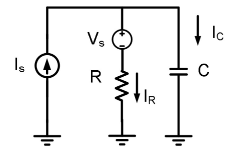


Figure 5.1: Simplified model of LED driven by a current I_s

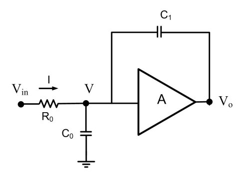


Figure 5.2: Negative capacitance bus terminator

5.2 Negative Impedanve Converter (NIC)

Electrical model of an LED in its simple format is composed of a series resistance with a voltage source, all in parallel with a parasitic capacitance. With the assumption of passing an electrical current through the LED, this current will be flowed in two branches, one through the resistor and the other one through the capacitor as shown in Figure 5.1.

The optical power is proportional to the current, I_R, passing through the resistor R. In order to achieve a good performance, a very small parasitic capacitance C in the order of pF is desirable. However, in most of the commercial LEDs this parasitic capacitance is in the order of nF. In ideal case, we want this parasitic capacitance to have a negligible effect on the frequency response and as a result it is desirable to ameliorate the performance by reducing or canceling its effect. One way is putting a negative capacitance in parallel with the LED. Even if this negative capacitance would not be the exact negative of parasitic capacitance, it still helps to reduce the overall equivalent parasitic capacitance.

The negative capacitors can be used to compensate for the loading effects of parasitic capacitors. The concept of negative capacitance is proposed in [58] for increasing the data transfer speed of a microcomputer bus. Figure 5.2 shows applying this concept to a bus terminal.

Based on this figure, current I can be calculated as (5.1) which means the

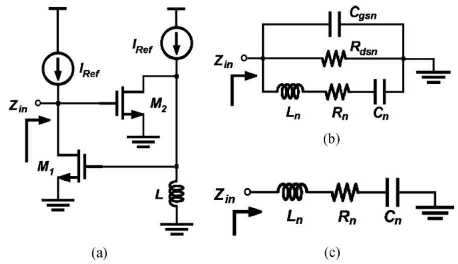


Figure 5.3: Negative capacitance cell: (a) Simplified circuit schematic, (b) Small signal equivalent circuit, (c) Simplified equivalent circuit

bus resistance is driving a single capacitance with the value of $C_0 - (A-1)C_1$. And if the $A > 1$, then it is driving a negative capacitance. Similar technique is used in [59] by connecting two cross coupled transistors to increase the bandwidth of the microstrip antennas.

$$I = C_0 \frac{dV}{dt} - C_1 \frac{d}{dt}(AV - V) = C_0 - (A-1)C_1 \frac{dV}{dt} \tag{5.1}$$

Negative impedance converter (NIC) circuits are widely exploited to generate negative resistance, inductance, or capacitance. As shown in Figure 5.3(a), two common-source transistors are connected in a way that a positive feedback loop is generated to convert the inductor load, L, to a negative capacitor [60].

Assuming both of transistors in Figure 5.3(a) are identical, the equivalent circuit is demonstrated in Figure 5.3 (b). If the operating frequency is much smaller than the cutoff frequency (f_T) of transistors, the influence of parallel elements (C_{gs}) and R_{ds} in Figure 5.3 (b) on the circuit performance is negligible, and the equivalent circuit can be reduced to a series RLC circuit as depicted in Figure 5.3 (c). The simplified expression for total input impedance of the circuit is given in (5.2).

$$Z_{in} = -\frac{1}{j\omega L g_{mn}^2} - j\omega \frac{C_{gsn}}{g_{mn}^2} - \frac{1}{g_{mn}^2 R_{dsn}} \tag{5.2}$$

The first term of this equation is a negative capacitance and its value is given by $C_n = -Lg_m^2$ and it is determined by the trans-conductance of transistors and the inductive load. The second term in this equation represents a negative

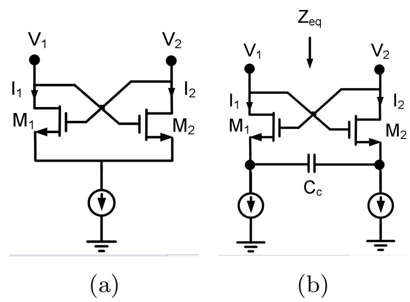


Figure 5.4: Circuit schematic of (a) Floating negative resistor, and (b) Floating negative capacitance

inductance that can be compensated by placing a proper inductor at the circuits input. Moreover, as represented by the third term in (5.2), this structure produces a negative resistance as well which is usually used to extend the bandwidth.

The typical way to generate a floating negative resistor and/or a negative capacitor is to use a cross-coupled pair of transistors to create positive feedback. Figure 5.4(a) and Figure 5.4(b) show the schematic diagram of a conventional negative resistance and a negative capacitance circuit, respectively [61–64]. As shown in Figure 5.4(b), M_1, M_2 and C_c introduce a negative capacitance.

The positive feedback loop formed by transistors M_1 and M_2 makes the difference in the output currents $(I_1 - I_2)$ to have an opposite polarity to the differential voltage $(V_1 - V_2)$. Thus, the equivalent output impedance (Z_{eq}) has a negative value [64]. According to [62], the equivalent output impedance of the negative capacitance circuit which is shown in Figure 5.4(b) is calculated as (5.3).

$$Z_{eq} = -\frac{1}{sC}\frac{g_m + s(C_{gs} + 2C)}{g_m} \tag{5.3}$$

The zero frequency in this equation used to boost the gain-frequency response at around $3dB$ frequency and extend the bandwidth of the circuit.

5.2.1 Accurate Formula for NIC

The more accurate value of the floating negative capacitance circuit depicted in Figure 5.4(b), redrawn in Figure 5.5(a), and Figure 5.5(b), is calculated here as it

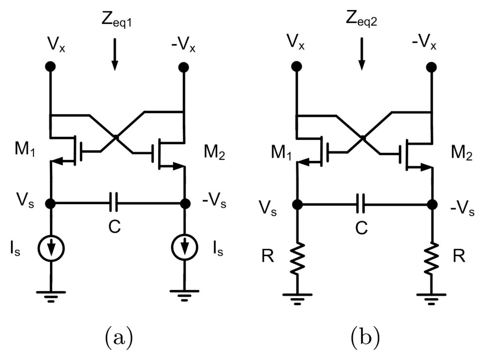


Figure 5.5: Calculating the accurate value of the floating negative C (a) Using current source, (b) Using resistor R

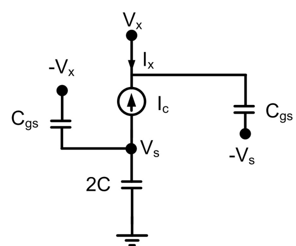


Figure 5.6: Equivalent of circuit shown in Figure 5.5(a)

is critical to have a good understanding of its value for different load values and at different frequencies.

To calculate the equivalent impedance, the simplified circuit for Figure 5.5(a) is shown in Figure 5.6, where I_c is calculate as Equatin (5.4).

$$I_c = g_m(V_x + V_s) \tag{5.4}$$

After doing some math, the Z_{eq1} is calculated as following which is more accurate than the one reported in [62].

$$Z_{eq1} = -\frac{1}{sC}\frac{g_m + s(C_{gs} + 2C)}{g_m - sC_{gs}} \tag{5.5}$$

And for the other one where the current sources are replaces by their output resistance shown in Figure 5.5(b), its equivalent model is depicted in Figure 5.7. Based on this figure Z_{eq2} is calculated as (5.6).

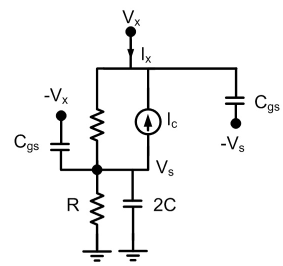


Figure 5.7: Equivalent of circuit shown in Figure 5.5(b)

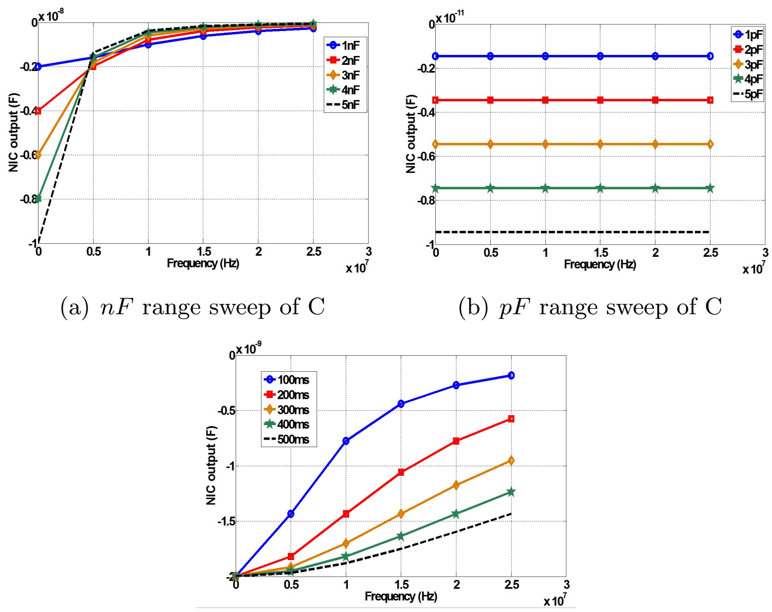
$$Z_{eq2} = \frac{g_m + s(C_{gs} + 2C) + (\frac{1}{r_o} + \frac{1}{R})}{\frac{1}{2r_o}(\frac{1}{R} + 2s(C + 2C_{gs})) + \frac{1}{2}(g_m - sC_{gs})(2sC + \frac{1}{R}))} \tag{5.6}$$

This can be modeled as a series combination of RLC circuit. To get an equivalent negative capacitance, the DC current sources I_s should have a large value which leads to a high g_m value for transistors. Using numerical analysis an optimum value for the design parameters can be derived. The following figure shows how different values of g_m leads to different equivalent capacitances. And in general to get a good performance using this structure, a high value of g_m is needed and the operating frequency should be limited to a fraction of its cut off frequency (f_T). As shown in this figure, at high frequencies the equivalent is no longer negative impedance, so the condition $f \ll f_T$ should be satisfied. In [65] the relation of single ended (half of differential) output impedance and equivalent negative output capacitance of the NIC network considering the effect of gate-drain capacitance are given in (5.7) and (5.8), respectively.

$$Z_{eq2} = \frac{g_m + s(C_{gs} + 2C)}{(g_m - sC_{gs})(2sC) - 4sC_{gd}[s(C_{gs} + 2C) + g_m]} \tag{5.7}$$

$$C_{in}(s) = -2C\frac{g_m^2 - \omega^2 C_{gs}(C_{gs} + 2C)}{g_m^2 + \omega^2(C_{gs} + 2C)^2} + 4C_{gd} \tag{5.8}$$

Based on this equation, with the assumption of $g_m = 125ms$, $C_{gs} = 450fF$, $C_{gd} = 140fF$, the sweep of C from $1nF$ to $5nF$, and from $1fF$ to $5fF$ are shown in Figure 5.8(a) and 5.8(b), respectively. As it is depicted here, this structure works



(a) nF range sweep of C

(b) pF range sweep of C

(c) g_m sweep

Figure 5.8: The sweep of C and g_m of floating NIC

great for small (around fF) input capacitances. However, for the large values of this capacitance, the equivalent output of the NIC is no longer negative. In the same manner, with the assumption of $C = 1nF$, the equivalent output capacitance of the NIC for the sweep of g_m from $100ms$ to $500ms$ is depicted in Figure 5.8(c) (these values are considered very large, and these values are selected just to show the need of high g_m for the case of large negative capacitance for this structure). Other words, the objective is that this structure is not suitable for large desired values of negative capacitance. This shows that for having a wide range NIC structure, the high g_m transistors are needed which is equivalent with having large bias currents.

5.2.2 Proposed LED Driver Based on the Floating Negative Capacitance

After analyzing the formula and operating conditions of the floating negative capacitance circuit, the proposed LED driver utilizing this concept is shown in Figure 5.9.

The input voltage, V_{in}, is converted to a current signal with the help of

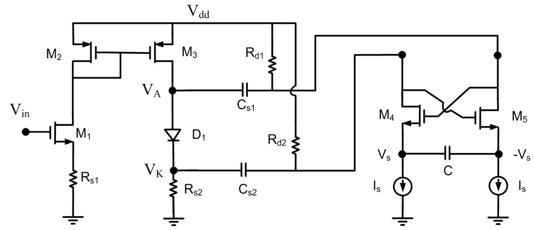


Figure 5.9: The proposed LED driver with floating negative C circuit

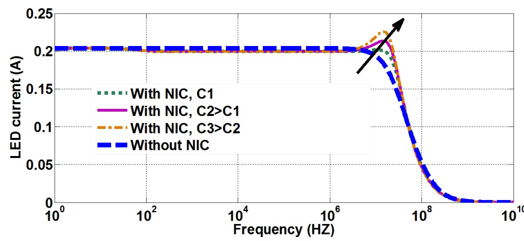


Figure 5.10: Frequency response of the circuit shown in Figure 5.9

degenerated common source composed of transistor M_1 and resistor R_{s1}. The overall trans-conductance of this voltage to current modification is given as $\frac{g_m}{1+R_{s1}g_m}$. The resistor R_{s1} helps to keep the operation in the linear region. Then, this current will be flowed into the LED, D_1, through the current mirror composed of transistors M_2 and M_3. The floating negative C section is composed of M_4, M_5 and C. The current sources I_s together with R_{d1}, R_{d2} are used to provide the DC biases. The objective of this architecture is to force the floating negative circuit to provide a negative C value close to the parasitic capacitance value of D_1. Figure 5.10 shows the frequency response of this proposed circuit with and without using the negative impedance converter (NIC) for three different values of C showed in Figure 5.9.

The same discussion is reported in [61] and it is shown how different values of C can lead to different responses. It is stated that the optimum value should be chosen which leads to a good performance. This structure helps to extend and flatten the frequency response as depicted in Figure 5.10. However, the big extension and improvement is not achieved which is mainly due to the fact that for this structure to produce a negative capacitance, a large current source is needed which put a limit on the maximum value of this current source due to the voltage headroom and power consumption. This might not be an issue in applications where the expected value

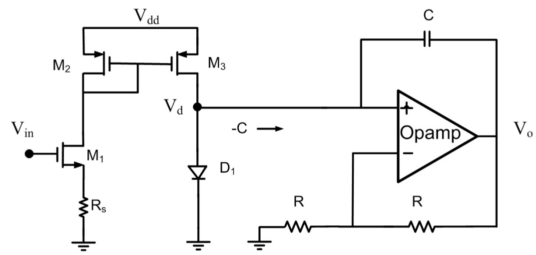


Figure 5.11: Schematic of the proposed LED driver utilizing the fixed negative C

of negative C is in the order of fF. As reported in [61] and [62], the lower the value of the negative C, the lower the value of the current source. Most of the commercial LEDs have the parasitic in the order of hundreds of pF for high voltage LEDs and nF for high current LEDs and seems this topology cannot play a significant role in canceling the parasitic capacitance of the LED. The next proposed driver is a better option for driving large parasitic capacitances.

5.2.3 Proposed LED Driver using Fixed Negative C Circuit

The schematic of the proposed circuit is shown in Figure 5.11. Voltage to current conversion together with the current mirror is the same as previous driver. In this circuit, the Opamp together with capacitor C and resistor R are used to provide a negative C value.

According to Figure 5.11, the V_o is two times of the voltage V_d, $i.e.$ $V_o = 2V_d$. So the gain from non-inverting pin to the output of the Opamp is equal to 2. Based on the Miller effect, the Miller capacitance at the input of the Opamp is calculated as $C_{eq} = C(1 - A_v) = C(1 - 2) = -C$.

And this negative C is placed in parallel with D_1 to cancel out its parasitic capacitance. As a result, by tuning the value of C, an optimum value can be measured. The frequency response for the values of $C = 1nF$ and $R = 150\Omega$ is drawn in Figure 5.12. Based on this figure, utilizing the negative C circuit, the frequency response has a flat curve up until 80MHz, while without using this technique its flatness extends only till 6MHz. This topology is applicable for commercial LEDs which have a large value of parasitic capacitance.

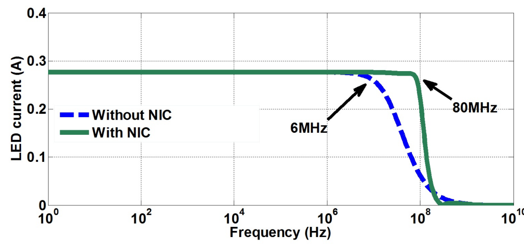


Figure 5.12: Frequency response of the proposed circuit shown in Figure 5.11

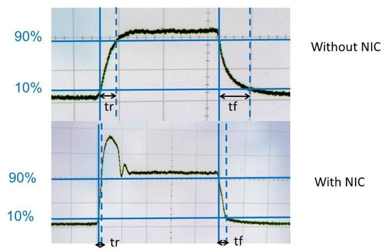


Figure 5.13: Measurement result for rise and fall time with and without using NIC

Figure 5.13 shows the measurement results. Without using NIC the rise time is $100ns$ and with using the NIC the rise time decreases to $8ns$. The optical bandwidth is given by $0.35\sqrt{3}/t_r$, where the t_r is the rise time of the LED current. Applying this formula, the optical bandwidth without using the NIC and with using NIC is calculated as 6.1MHz and 76MHz, respectively.

NIC is promising in cancellation of the parasitic capacitance of LED. By putting the negative C circuit in parallel with LED, at least some part of its parasitic will be cancel out and it helps to extend the flatness of the frequency response which leads to having higher bandwidths and higher data transmission rates.

5.3 Equalization and Complex Modulations

Several challenges are hindering the development of commercial VLC systems. A-mong them is the slow modulation response of commercial white LEDs based on blue LEDs with a yellow phosphor coating. The slow response time of the phosphor restricts the modulation bandwidth of the device to several MHz. The application of a blue filter at the receiver removes the slow component from the modulated signal and enables modulation frequencies of up to 12MHz. To extend the bandwidth of LEDs beyond their intrinsic values, some state of the art analog, digital or mixed signal processing is required. In this section, after reviewing and discussing well known techniques of increasing the bandwidth of LEDs in optical domain, the proposed methodology is introduced.

5.3.1 Multiple-Resonant Equalization

The bandwidth of a white LED is limited to around 2-3 MHz and this can be extended to around 12MHz after blue-filtering in the receive side. Multiple-resonant equalization is one way of achieving a higher bandwidth. In this scheme, let assume n number of LEDs can be used and each one will be located in a resonant circuit tuned to a unique frequency. In this scenario first LED, LED1, will be tuned to f_1, second LED, LED2, will be tuned to f_2 and in the same manner the nth LED, LEDn, will be set to the f_n which is the desired 3dB bandwidth of the system. This methodology is implemented using 16 ($n = 16$) number of resonated white LEDs as reported in [66]. LEDs are Luxeon Star and each one is fitted with a wide-angle diffusing lens. Measurement of the LEDs indicates the commercially packaged devices have significant series inductance. The resonant modulation circuit for an individual LED is also shown in Figure 5.14. Each of the 16 LEDs is modulated via a high-speed buffer ($BUF634T$), and a DC current is added to this signal using a bias Tee. Resonance is achieved for the ith device using a capacitor between the buffer and bias Tee. The value of resonant frequency is given by $f_i = 1/2\pi(\sqrt{L_{series}C_i}$. L_{series} is the total series inductance in the driving circuit including LED inductance. In the receiver the concentrator is used to focus the incoming light into the photodiode (PD), which later will be amplified and passed through a low pass filter (LPF) for signal processing. These 16 LEDs generates an overall bandwidth of 25MHz while the raw bandwidth of LED is 2.5MHz. This 25MHz equalized bandwidth is controlled by adjusting the resonant frequency of the LEDs and each LEDs contribution to the overall response. The total response is the superimposition of responses of all 16 LEDs.

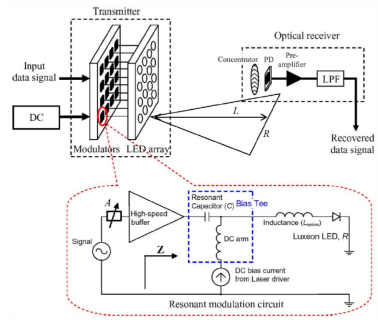


Figure 5.14: VLC testbed system using an array of 16 resonated white LEDs

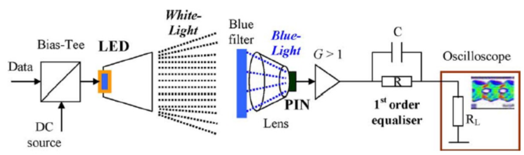


Figure 5.15: VLC system with post-equalizer

5.3.2 Passive Equalization at the Receiver

It is mentioned earlier that the blue-filtering helps to extend the bandwidth of the system. The other approach is using the equalization in the receive side after the incoming signal is detected and amplified. Different design methodologies are developed for the optical receivers. In [54] three distinct equalization methods of an RC high pass equalizer, a fractionally spaced zero-forcing equalizer (ZF) and an artificial neural network (ANN) are proposed. A systematic approach for designing a low noise and low power optical receiver targeting high sensitivity imaging architectures for optical wireless communications is proposed in [67]. The method that can be used to extend the bandwidth of VLC system based on phosphorescent white LED and improve the signal amplitude is utilizing a post-equalization circuit.

In the receive side the blue filter is used to filter out the slow phosphorus response of the LED and lens is used to guide the light to sit on the PIN photodiode. The output current of the photodiode will be amplified and passed through a first order equalizer. It is shown in [68] that using the equalizer in the receiver helps to extend the overall bandwidth of the link.

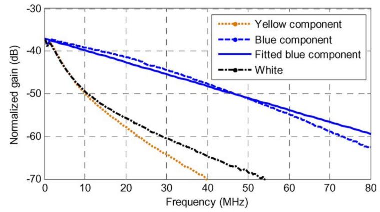


Figure 5.16: Modulation bandwidths of individual components

5.3.2.1 Transmit Side: First Order LED Response

The measured frequency responses of different components of a typical LED's emission, white, blue and yellow are depicted in Figure 5.16.

In the transmit side, the blue response can be modeled by the first order estimation of $H_t(\omega) = e^{-\omega/\omega_t}$. As shown in Figure 5.16, the slope of the blue component, lets call it S_t, is constant [68].

5.3.2.2 Receive Side: Equalization

This equalizer is composed of a capacitor in parallel with a resistor [68]. The frequency response of the equalizer, in the receive side, is calculated as $H_r(\omega) = \frac{1}{k} \times \frac{1+j\omega T}{1+j\omega T/k}$, where $1/k = R_L/(R + R_L)$ and $T = RC$. R_L is the load impedance. The $1/k$ term is the dc coefficient of the equalizer. The 3dB point above this equalized dc value is computed as $\omega_{3dB} = \frac{1}{T}\sqrt{\frac{k^2}{k^2-2}}$. The magnitude of $H_r(\omega)$ is linear around the 3dB point and can be approximated by $S_r = \frac{6\pi T}{\sqrt{\frac{k^2}{k^2-2}}}$. The other method as proposed by [54] is using high-pass filter equalizer. It can be assumed that the impulse response of an LED is given by $H_{LPF}(t) = \frac{1}{\tau}e^{\frac{-t}{\tau}}$, which can be written in the frequency domain as $H_{LPF}(\omega) = \frac{\omega_{LPF}}{j\omega_{LPF}+\omega}$, where $\omega_{LPF} = 1/(RC)$ is the measured cut off frequency of the LED. So as to alleviate this roll of in the frequency response of the LED, it is desired to have a high pass filter (HPF) with the impulse response of $H_{HPF}(t) = 1 - H_{LPF}(t) = 1 - \frac{1}{\tau}e^{\frac{-t}{\tau}}$. This yields to the HPF frequency domain response of $H_{HPF}(\omega) = \frac{j\omega}{\omega_{HPF}+j\omega}$, where $\omega_{HPF} = 1/(R_{eq}C_{eq})$ and R_{eq} and C_{eq} are the equalizer resistor and capacitor, respectively. Based on these equations, one can define a scenario for determining the values of R and C of the equalization network.

Such approach is defined in [68]. Here a practical approach can be defined as:

1. Determine the minimum value for the R such that the dynamic range of the receiver is satisfied. Based on $1/k = R_L/(R + R_L)$, and a fixed value for R_L (usually 50Ω), the value of k can be derived.

2. Measure the raw frequency response of the desired LED and calculate its ramp, *i.e.* S_t.

3. To cancel out the decreasing ramp of the LED response, the ramp of this curve should be set equal to the ramp of equalized response, *i.e.* $S_t = S_r$. Consequently, based on the equation of S_r, the value of T and hence the value of capacitance of the first order equalization, C, can be derived.

Due to non-idealities and error in the measurement cycle, one might need to tune the calculated values of R and C to grasp the optimum response with the maximum bandwidth. In [68] a simple first-order analog and low-cost approach to equalize the modulation bandwidth of white-LED-based VLC system is presented. The bandwidth achieved is 50MHz (25 times wider than unequalized LED bandwidth). Using this technique, data transmission in VLC system is experimentally demonstrated showing that a 100Mbps OOK NRZ transmission can be achieved with low BER.

5.3.2.3 Measurement Results for Post-Equalization

Here just to show the proof of concept, we have implemented the same testbed as the one showed in Figure 5.15. In the transmit side the bias Tee is used for injecting data as well as biasing the LED. In the receive side we have used blue-filtering at the input of the photo-detector. The first order equalization composed of a resistor, 480Ω and a capacitor, $20pF$ is used for bandwidth enhancements and finally its output is connected to the scope with input impedance of 50Ω. The measurement results are shown in Figure 5.17. Without using any equalization the LED can provide a VLC link with BER of less than 10^{-3} for data rate of 10Mbps. However,

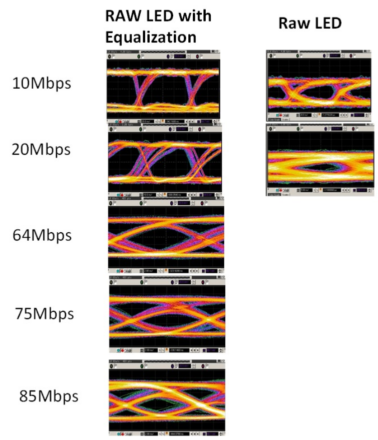


Figure 5.17: Measurement results of first order equalization in the receive side

with just using first order post-equalization and with the same BER performance, the VLC link with data rate of up to 85Mbps is achieved.

5.3.3 Active-Passive Equalization at the Receiver

The same design procedure can be applied to the case where equalization is done using active components. In [69] design and implementation of an active equalizer is described. High order post equalizations can be used to increase the degree of freedom such as controlling the gain of the receive chain and/or compensating the roll-off in the pre-amplifier or TIA response. One example of this approach is presented in [70] where an active cell is sandwiched between two passive first order equalizers, as shown in Figure 5.18. The design methodology in general would be the same as the one described in the previous section. In short, the poles and zeros of the system composed of the LED response, described in section 5.3.2.2, the preamplifier frequency response together with passive and active equalizers should be calculated and corresponding zeros placed in the vicinity of their counterpart poles of the system.

In [70] a three stage post equalization (two passive stages and one active stage to boost the signal) is used. Based on the results, without having any equalization the total bandwidth is 12MHz (limited by the LED and blue filtering), but after implementing the post equalization the total bandwidth goes to 151MHz.

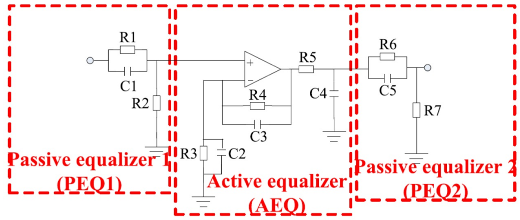


Figure 5.18: VLC post-equalization circuit using passive and active components

Equalization, either passive or active, is a good method of increasing the overall bandwidth of the system. These techniques can be applied to either of transmitter or receiver. Knowing the frequency response of the transmitter, a good systematic design is presented in [68] which can be extended to the case of active equalization as well. A matched transmitter-receiver equalization method is needed for ever increasing and extending the overall bandwidth of the VLC link.

5.3.4 Using Complex Modulation: DMT and OFDM

In VLC systems, the communication signal is simply modulated onto the instantaneous power of the optical carrier with no frequency or phase information and the optical photodiode generates a current proportional to the received instantaneous power which is the basis of intensity modulation with direct detection (IM/DD) [71]. Orthogonal frequency-division multiplexing (OFDM) is a promising multi-carrier modulation technique for VLC systems due to, for example, its high spectral efficiency and resistance to inter-symbol interference (ISI) [72]. In OFDM-based VLC systems, and assuming a limited LED bandwidth and high-quality signal from illumination requirement, high data rates are supported through parallel transmission of high-order multilevel quadrature amplitude modulation (M-QAM) symbols on orthogonal sub-carriers. Discrete multi-tones (DMT) is a baseband implementation of the more generalized OFDM and is most useful for channels with interference or strong low-frequency noise due to the artificial ambient light sources such as fluorescent and incandescent. Both quadrature amplitude modulation (QAM) on DMT and multilevel pulse amplitude modulation (PAM) are spectrally efficient modulation schemes suitable for LED-based communications, but they are less power

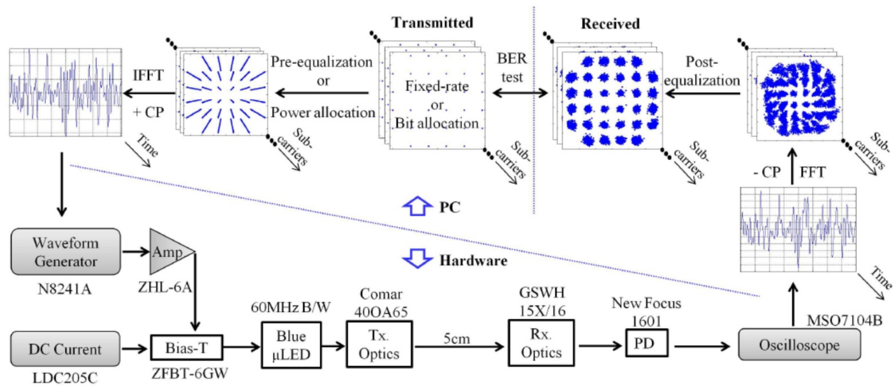


Figure 5.19: Experimental setup of single LED OFDM based wireless VLC link

efficient. The bandwidth of high-data-rate systems is limited due to the capacitance constraints of large-area photodiodes and, therefore, a compromise between power and bandwidth requirements must be pursued. In an OFDM transmitter, serial data streams are grouped and mapped into N constellation symbols using BPSK, QPSK or M-QAM modulation schemes [57].

By using spectrally efficient modulation techniques such as discrete multitone modulation (DMT) and MIMO-OFDM, 200Mbps, 513Mbps and 3.3Gbps VLC systems have been demonstrated in [73–75]. Micro LEDs exhibits a 3dB modulation bandwidth significantly higher than commercially available white lighting LEDs. These devices are promising and have the potential of meeting the target of Gbps for VLC links specifically in a system whether the OFDM/DMT modulation is being utilized. In [75] a VLC system based on a single $50\mu m$ gallium LED, with a 3dB modulation bandwidth of at least 60MHz is presented. OFDM is employed as a modulation scheme which enables the limited modulation bandwidth of the device to be fully used. Pre- and post-equalization techniques, as well as adaptive data loading, are successfully applied to achieve a demonstration of wireless communication at speeds exceeding 3Gbps. The modulation and signal processing is done in MATLAB.

Figure 5.19 shows the experimental set up [75]. The analog signal is amplified with a high-power amplifier, Mini-Circuits $ZHL-6A$ (This has a gain of 25dB across the frequency range of 2.5kHz to 500MHz with IP3 of +34dBm), which drives the

μLED. The μLED emits blue light with a wavelength distribution centered around 450 nm and has a maximum optical power of around $4.5mW$. A direct current (DC) bias from a laser driver is added to the drive signal using a bias-Tee, Mini-Circuits $ZFBT-6GW$. Light from the μLED is imaged onto a high-speed photo-detector, New Focus $1601FS-AC$, using a high numerical aperture (NA) microscope objective, model $40OA65$ from Comar Optics. The output signal of the photodetector is captured by a digital oscilloscope, Agilent $MSO7104B$. Afterwards, it is processed in MATLAB with a sequence of steps that include: synchronization, fast Fourier transform (FFT), equalization, and M-QAM demodulation. The distance between the transmitter and the receiver is set at $5cm$. This is limited by the optical power of the μLED and the small area of the photodiode (PD).

In general, complex modulations are superior to the baseband digital modulations in term of the bandwidth capacity. However, they need a bulky system for practical implementation, one of which is described in this section. The use of micro-LEDs also further helps in extending the overall bandwidth of the VLC link as these devices are not limited to the low frequency bandwidth of white LEDs. However, they might not provide the same level of brightness as white LEDs. This is an open research area and it is desired to find a systematic solution which leads to an appropriate brightness for office-sized locations while it can provide adequate bandwidth for data transmission. And as mentioned earlier the solution lies on providing a good compromise over the bandwidth of the system and the output power of the LEDs.

5.4 Bandwidth Enhancement using Pulse Shaping

Using the digital base-band modulation schemes such as NRZ OOK, some state of the art designs are needed to alleviate the overall low bandwidth of the system. Pulse shaping is one of potential candidates that can be utilized to overcome the low bandwidth of the VLC link. In the following, the carrier sweep-out technique is described which works based on removing the stored charge across the LED during the off-time of the data signal. The advanced version of the technique later on is presented which works by injecting current to the LED at the rising edge of the data signal. This mechanism shortens the rise time and extends the overall bandwidth.

5.4.1 Carrier Sweep-out

When the LED is turned on, the charge is stored on its parasitic capacitance which makes it hard to rapidly discharge as LED starts to be turned off. To improve this effect, one might shut the LED off by removing the stored carriers that has been stored when the LED was on. This is nothing but sweeping out the remaining carriers in the LED. In [76] two version of this technique is employed. One is performed using a driver fabricated on a board with discrete GaAs FETs. And the other one is implemented using a $0.18\mu m$ CMOS process to fabricate LED drivers with carrier sweep-out capabilities. The driver drives the LEDs using only a CMOS inverter. Therefore, the driver is simple and low power, both of which are important characteristics for an LED driver used primarily for illumination.

(a) Using the GaAs discrete transistors

A carrier sweep-out circuit using discrete GaAs FETs and passive elements on a board is designed and fabricated [76]. The circuit diagram is shown in Figure 5.20. A simple common-source T_1 drives the LED. The part of the circuit surrounded by the solid line represents the carrier sweep out region. Input voltage V_{in} and V_3 at the gate of T_2 are 180 degrees out of phase. T_2 is turned off the moment the LED turns on and is turned on the moment the LED shuts off. Because both terminals of the LED are shorted at the moment the LED shuts off, the remaining carriers in the LED are swept out. The maximum error-free bit rate for the NRZ PRBS signal increased from 69 to 95Mbps for the drivers without and with sweep-out carriers, respectively.

(b) Using the CMOS transistors on chip

A driver configuration with a CMOS inverter was employed to reduce the power dissipation of the LED driver in $0.18\mu m$ CMOS IC process and to

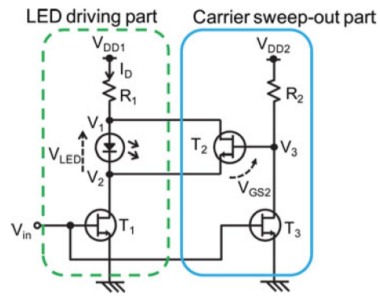


Figure 5.20: Schematic of LED driver for sweeping out the carriers using discrete GaAs FETs

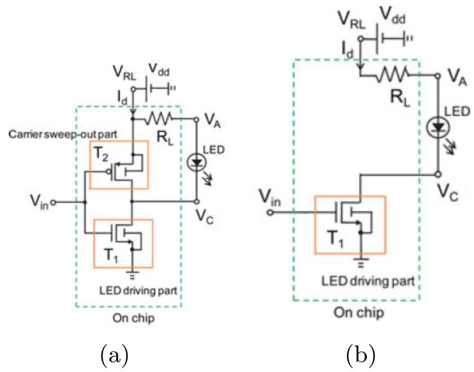


Figure 5.21: LED driver: (a) Sweeping out the carriers using PMOS, (b) Reference LED driver

sweep out the remaining carriers. Figure 5.21(a) presents the circuit diagram for the driver with carrier sweep-out. As a reference, Figure 5.21(b) presents the same diagram for an LED driver without carrier sweep-out. In 5.21(a), the PMOS transistor (T_2) in the sweep-out part of the circuit has a configuration complementary to T_1. The maximum error-free bit rate for the NRZ PRBS signal increased from 27.5 to 51.8Mbps for the system without and with the carrier sweep-out ability, respectively.

5.4.2 Pulse Shaping Circuit

The ultimate bandwidth of an optical communications channel using an LED source depends not only upon the material, but also on the rise times of the source and detector. Frequently, the limiting factor is the rise time of the source. A closed-form expression relating the source rise time to the parameters of the LED and the

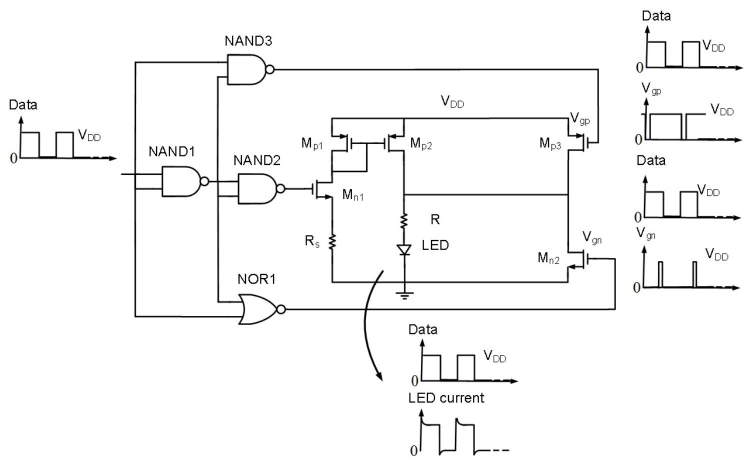


Figure 5.22: Schematic of LED driver for pulse shaping technique

current would therefore be of value as it shed some light in finding the limitations toward achieving a high data rate VLC link. Previously it was mentioned that current peaking, serves to reduce the rise time. The solution for the $10-90\%$ rise time t_R for a staircase excitation current is given by (5.9).

$$t_r = \frac{C_s}{\beta I_a}\ln 9 + (\frac{C_s}{\beta I_a} + \tau_s)\ln\frac{1-(I_b/10I_a)}{1-(9I_b/10I_a)} \tag{5.9}$$

And also it was mentioned that if $I_a = 2I_b$ and I_a, $t_r \simeq 0.55\tau_s$, which is considerably less than the value of $2.2\tau_s$, the minimum t_r without current peaking. Based on this point in the following we have presented the proposed pulse shaping circuit that injects a high peak current to the LED in order to reduce its rise time. Based on the rise time discussion of a typical LED, implementing the peaking technique helps to reduce the rise and fall times and achieve a high data rate link. The schematic of the proposed driver composed of analog and digital sections is depicted in Figure 5.22.

Digital sections composed of NAND and NOR gates generate the appropriate timing signals at the gate of peaking transistors. These signals are extracted based on the shape of input data signal. There are two modes of operations, one at the rising edge of incoming data and the other one at the falling edge. The desired objective is reducing the rise as well as fall time of the current signal passing though

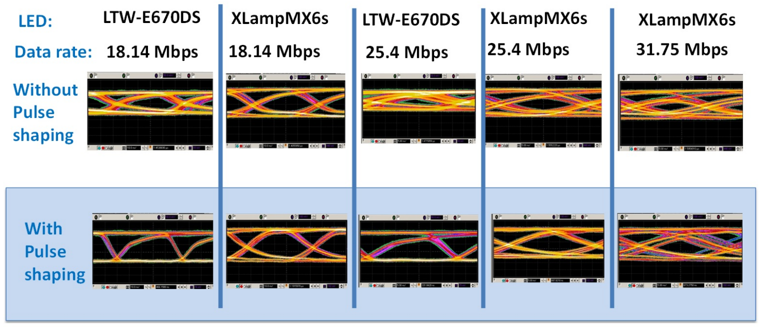


Figure 5.23: Measured eye diagram with and without using the peaking technique

the LED. In order to achieve this goal, a large current has to be injected at the rising edge of LED current. This is done by turning on MOSFET M_{p3} over short period of time and preferably at the exact timing as the rising edge; this is done by generating signal V_{gp}. The same thing hold for the falling edge and is implemented using the MOSFET M_{n2}, which is done by generating signal V_{gn}. V_{gp} (and V_{gn}) signals can be generated by the NAND (and NOR) operation of incoming Data signal, with its delayed version. Here, as is depicted on Figure 5.22, the delayed version of the incoming Data signal is connected to the gate of input transistor M_{n1} instead of just directly connecting the input Data signal to the gate of Mn1. This allows synchronizing the rising (and falling) edges of Data with the V_{gp} (and V_{gn}) signals. This input generates the current based on the threshold of the transistor M_{n1} and the value of resistor R_s and will be mirrored to the LED with the help of M_{p1} and M_{p2} transistors. For limiting the current through the LED a resistor R, 5Ω, is placed in series with the LED. Current of the peaking section (transistors M_{p3} and M_{n2}) is tuned by the supply voltage of the digital NAND and NOR gates.

For the measurement purposes, a 2^7-1 PRBS is generated and applied to the proposed LED driver. For the test purposes two different LEDs ($LTW-E670DS$ and $XLampMX6s$) are used. Figure 5.23 shows the eye diagrams taken with and without peaking technique. As it is depicted in this figure, the pulse shaping with the peaking technique allows transmission of high data rate signals where it was not possible without it.

Pulse shaping is the method that can be used along with the base-band digital modulation schemes in order to extend the bandwidth of the VLC link. The pulse shaping technique helps increasing the net bandwidth by shortening the rise and fall times of the LED current signal. The proposed circuit decrease the rise time by injecting a narrow pulse current at the rising edge of the input Data signal, and decreases the fall time by extracting current from the LED at the falling edge of the input Data signal.

5.5 Bandwidth Enhancement with Peaking

Inductive-peaking-based bandwidth extension techniques for CMOS amplifiers are discussed here. Passive filtering (*e.g.*, shunt and series peaking) has been used since the 1930s to extend amplifier bandwidth; it uses inductors to trade off bandwidth versus peaking in the magnitude response. Broadband design approaches that achieve larger bandwidth extension ratio (BWER) [77] are reviewed here.

5.5.1 Shunt Peaking

Shunt peaking is a bandwidth extension technique in which an inductor connected in series with the load resistor R. the output capacitor is denoted as C that can be written as $C = C_1 + C_2$, where C_1 is the drain capacitance of transistor and C_2 is the parasitic capacitance of the load. This shows how an inductor can enhance the bandwidth of an amplifier. Consider the simple common source amplifier illustrated in Figure 5.24(a). The gain of this stage is calculated as $\frac{V_{out}}{V_{in}}(\omega) = \frac{g_m R}{1+sRC}$.

The introduction of an inductance in series with the load resistance alters the frequency response of the amplifier as shown in Figure 5.24(b). This technique, called shunt peaking, enhances the bandwidth of the amplifier by transforming the frequency response from that of a single pole to one with two poles and a zero.

$$\frac{V_{out}}{V_{in}}(\omega) = \frac{g_m R(1 + s/(m\omega_0))}{1 + s/\omega_0 + s^2/(m\omega_0^2)} \tag{5.10}$$

The inductor introduces a zero that increases the overall gain with frequency, compensates the decreasing effect of C, and thus extends the 3dB bandwidth. An

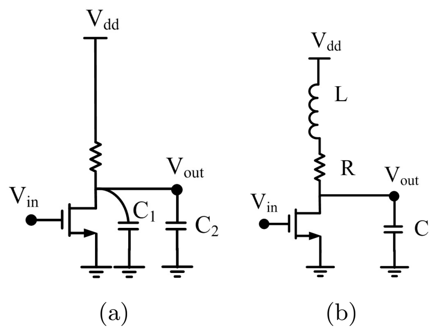


Figure 5.24: Shunt peaking: (a) Simple common source amplifier,(b) Common source with shunt peaking

m	**Normalized** ω_{3dB}	**Response**
0	1.00	No shunt peaking
$1+\sqrt{2}$	1.72	Maximally flat
$\sqrt{2}$	1.85	Maximum bandwidth

Table 5.1: Performance metrics for shunt peaking

equivalent explanation for increased bandwidth is reduced rise time. That is, the inductor delays current flow to the resistive branch so that more current initially charges C which reduces rise time. The poles are complex for practical cases of bandwidth extension. The zero is determined solely by L/R time constant or $m\omega_0$ term and is primarily responsible for the bandwidth enhancement. The frequency response of this shunt peaked amplifier is characterized by the ratio of the L/R and RC time constants. These two time constants are related by term m defined as $m = ((R^2C)/L)$. The case with no shunt peaking ($m = \infty$) is used as the reference so that its low-frequency gain and its ω_{3dB} (3dB bandwidth) are equal to one ($RC = 1$ and $g_mR = 1$). Performance metrics for shunt peaking for the values of m listed in Table 5.1. As expected, the 3dB bandwidth increases as m decreases. The maximum bandwidth is obtained when $m = \sqrt{2}$ and yields an 85% improvement in bandwidth. However, this comes at the cost of significant gain peaking. A maximally flat response may be obtained for $m = (1 + \sqrt{2})$ with a still impressive bandwidth improvement of 72%.

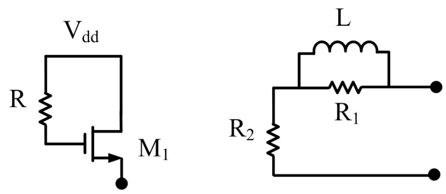


Figure 5.25: Active inductor and its equivalent model

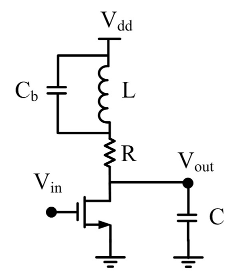


Figure 5.26: A common-source amplifier with bridged-shunt peaking

5.5.2 Active Inductive Shunt Peaking

Due to the big size of inductors, it might be wise to use the active inductor made of a resistor and a MOSFET. Figure 5.25 shows the circuit and its equivalent model. The equivalent input impedance seen from the source of the M_1 is calculated as $Z_{in} = \frac{1+sRC_{gs}}{g_m+sC_{gs}}$, where $R_1 = R - 1/g_m$, $R_2 = 1/g_m$, and $L = \frac{C_{gs}}{g_m}(R - 1/g_m)$.

For input impedance of this circuit to behave as an inductor, it is required that $R \gg 1/g_m$, then the impedance increases with frequency. However, this active inductor usually has a headroom problem that requires large supply voltages.

5.5.3 Bridged-Shunt Peaking

Although in shunt peaking, the increased impedance of the inductor accounts for the bandwidth improvement, it also leads to peaking in the response. Adding a bridge capacitor in parallel with the inductor allows for compensation of the frequency peaking with the possible maximum shunt peaking bandwidth increase. This parallel capacitor should be large enough to negate peaking but small enough to not significantly alter the gain response. This is depicted in Figure 5.26.

The voltage gain of bridged-shunt peaking is calculated as (5.11), where

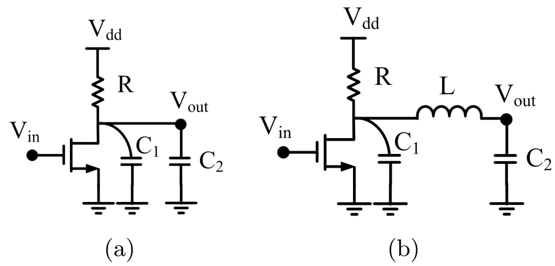


Figure 5.27: Series peaking comparison with simple common source amplifier

$k_B = C_b/C$, $\omega_0 = 1/RC$, and $m = (R^2C)/L$.

$$\frac{V_{out}}{V_{in}}(\omega) = \frac{g_m R(1 + (\frac{1}{m})\frac{s}{\omega_0} + (\frac{k_B}{m})\frac{s^2}{\omega_0^2})}{1 + \frac{s}{\omega_0} + (\frac{k_B+1}{m})\frac{s^2}{\omega_0^2} + (\frac{k_B}{m})\frac{s^3}{\omega_0^3}} \tag{5.11}$$

The advantage of bridged-shunt peaking over shunt peaking is that the maximum bandwidth is achieved for a larger value of m, which translates to a smaller inductance with smaller area.

5.5.4 Series Peaking

In designs where the drain parasitic (C_1) is significant, better BWER is achieved using capacitive splitting. Introducing a series peaking inductor is useful to "*split*" the load capacitance between the amplifier drain capacitance and the next stage gate capacitance. Without L, the transistor has to charge the total capacitance at the same time. And with L, initially only C_1 is charged, reducing the rise time at the drain and increasing bandwidth. This is depicted in Figure 5.27.

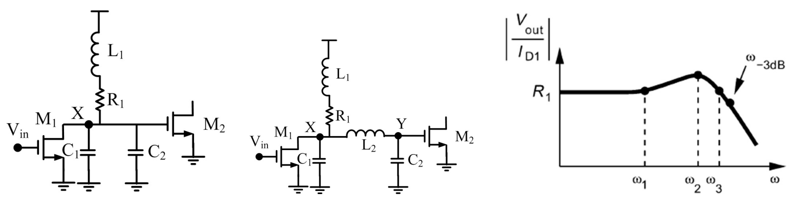
The voltage gain of series peaking is calculated as (5.12).

$$\frac{V_{out}}{V_{in}}(\omega) = \frac{g_m R}{1 + \frac{s}{\omega_0} + (\frac{1-k_C}{m})\frac{s^2}{\omega_0^2} + (\frac{k_C(1-k_C)}{m})\frac{s^3}{\omega_0^3}} \tag{5.12}$$

where $k_C = C_1/C$. Table 5.2 summarized the behavior of this series peaking for different values of m. As the parasitic capacitance ratio k_C increases, BWER increases as well.

$k_C = C_1/C$	Ripple (dB)	$m = (R^2C)/L$	BWER
0	0	2	1.41
0.1	0	1.8	1.58
0.2	0	1.8	1.87
0.3	0	2.4	2.52
0.4	1	1.9	2.75
0.4	2	2.5	3.17
0.5	3.3	1.5	2.65

Table 5.2: Performance metrics for series peaking



(a) Inductive shunt peaking stage

(b) TRA

(c) Frequency response of the TRA

Figure 5.28: Triple-resonance architecture

5.5.5 Triple-Resonance Architecture

Using two inductors, the new approach in extending the bandwidth is triple-resonance amplifier (TRA) [61]. The shunt peaking cascade of two stages is shown in Figure 5.28(a), where it is assumed that M_1 and M_2 contribute approximately equal capacitances $C/2$ to node X.

As the frequency approaches ω_1, defined as $\omega_1 = 1/\sqrt{L_1C}$, the impedance of L_1 rises and extend the bandwidth. To increase the bandwidth, inductor L_2 is placed in series with C_2 [Figure 5.28(b)] such that L_2 and C_2 resonate at ω_1. For L_2 and C_2 to resonate at ω_1, the value of L_2 should be equal to $2L_1$. In order to minimize peaking, R_1 should be set to $2\sqrt{(L_1/C)}$ [61].

The amplifier exhibits the frequency response shown in Figure 5.28(c), revealing three distinct resonance frequencies. For this reason, this topology is called "triple-resonance amplifier" (TRA). Second and third resonance frequencies are given by $\omega_2 = \frac{1}{\sqrt{L_2\frac{C_1C_2}{C_1+C_2}}} = \sqrt{2}\omega_1$, and $\omega_3 = \sqrt[4]{6}\omega_1$. The 3dB bandwidth is approximately equal to $\omega_{3dB} \cong \sqrt{3}\omega_1 = \frac{2\sqrt{3}}{R_1C}$. In other words, the TRA improves the

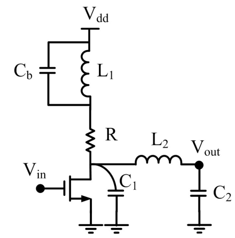


Figure 5.29: A common-source amplifier with bridged-shunt-series peaking and drain parasitic capacitance

bandwidth of the resistively loaded differential pairs by a factor of 3.5 ($2\sqrt{3}$).

5.5.6 Bridged-Shunt-Series Peaking

Combining capacitive splitting of the series-peaked circuit and inductive peaking of the bridged-shunt approach results in the bridged-shunt-series-peaked network of Figure 5.29. It uses two inductors but provides larger BWER values than its shunt-series-peaked counterpart. Combining both shunt and series peaking can yield even higher bandwidth extension.

Substituting $m_1 = (R^2C)/L_1$, $m_2 = (R^2C)/L_2$, k_B, k_C, and ω_0, as defined before, the voltage gain function of the bridged-shunt-series-peaked network is as shown in (5.13) and (5.14). Table 5.3 shows results for a range of k_C and passband ripple values.

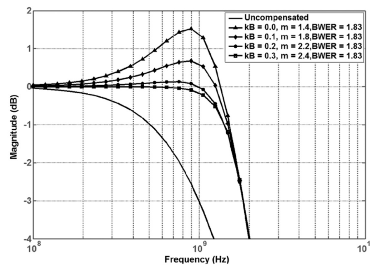
$$\frac{V_{out}}{V_{in}}(\omega) = \frac{g_m R(1 + (\frac{1}{m_1})\frac{s}{\omega_0} + (\frac{k_B}{m_1})\frac{s^2}{\omega_0^2})}{D_b(s)} \tag{5.13}$$

$$\begin{aligned} D_b(s) = 1 + \frac{s}{\omega_0} + (\frac{k_B + 1}{m_1} + \frac{1 - k_C}{m_2})\frac{s^2}{\omega_0^2} + (\frac{k_B}{m_1} + \frac{k_C(1 - k_C)}{m_2})\frac{s^3}{\omega_0^3} \\ + (\frac{(k_B + k_C)(1 - k_C)}{m_1 m_2})\frac{s^4}{\omega_0^4} + (\frac{(k_B k_C)(1 - k_C)}{m_1 m_2})\frac{s^5}{\omega_0^5} \end{aligned} \tag{5.14}$$

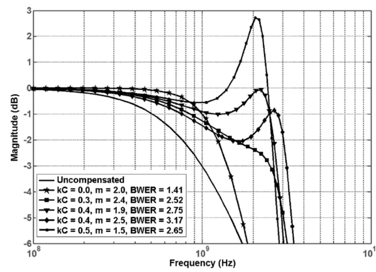
Proper choice of component values can yield close to four time increase in bandwidth with no peaking. However, this requires tight control of these components, which can be difficult with process-voltage-temperature (PVT) variations.

$k_C = C_1/C$	Ripple (dB)	$m_1 = (R^2C)/L_1$	$m_2 = (R^2C)/L_2$	$k_B = C_B/C$	BWER
0.4	0	8	2.4	0.3	3.92
0.4	2	6	2.4	0.2	4
0.5	2	6	2	0.2	3.53

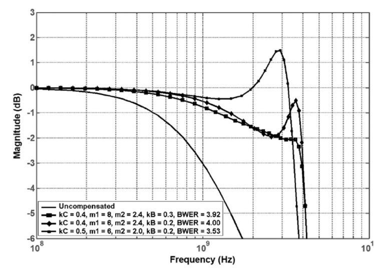
Table 5.3: Bridged-shunt-series peaking summary



(a) Ideal bandwidth improvement with bridged-shunt peaking



(b) Ideal bandwidth improvement with series peaking



(c) Ideal bandwidth improvements with bridged-shunt-series peaking

Figure 5.30: Comparison of bridged-shunt peaking, series peaking, and bridged-shunt-series peaking

Note that the shunt-series design explained in previous section that gives an ideal BWER of 3.5 (with 1.8dB peaking), is a special case of bridged-shunt-series peaking with $k_C = 0.5$ and $k_B \sim 0$; it is sub-optimum in applications where the load capacitance is large ($k_C < 0.5$). In contrast, C_B in a bridged-shunt-series peaked design adds a degree of freedom to control a zero that mitigates the effects of parasitics and leads to a larger BWER.

Figure 5.30 shows the comparison view of the frequency response plots of the bridged-shunt peaking, series peaking, and bridged-shunt-series peaking. According to these figures, by proper selection of the design parameters, different values of BWER are achievable.

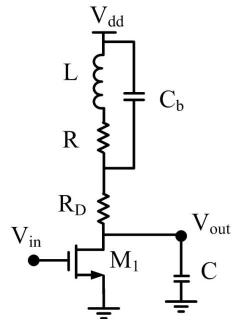


Figure 5.31: Modified bridged-shunt peaking

5.5.7 Proposed Bridged-Shunt-Zero Peaking

In this section, the modified version of the bridged-shunt peaking is proposed. First, this proposed bridged-shunt peaking is described and then another proposed peaking circuit suitable for driving nonlinear LEDs is described. As it was mentioned in previous section, the shunt-series TRA design gives an ideal BWER of 3.5, and bridged-shunt-series peaking which has one more degree of freedom yields to an even higher BWER value of 4.

5.5.7.1 Proposed Bridged-Shunt Peaking

Figure 5.31 shows the circuit schematic of modified bridged-shunt peaking. In this circuit a resistance R is added in series with inductor L to provide one extra degree of freedom in the design of the shunt peaking circuit.

The voltage gain of this structure is given by (5.15), where $k_B = C_b/C$, $k_R = R/R_D$, $\omega_0 = 1/((R_D C))$, $m\omega_0^2 = 1/LC$, and $m = (R_D^2 C)/L$.

$$\frac{V_{out}}{V_{in}}(\omega) = \frac{g_m R_D((1+k_R) + (1+mk_Rk_B)\frac{s}{m\omega_0} + (\frac{k_B}{m})\frac{s^2}{\omega_0^2})}{1+\frac{s}{\omega_0}(1+k_R(1+k_B)) + (mk_Rk_B + k_B + 1)\frac{s^2}{m\omega_0^2} + (\frac{k_B}{m})\frac{s^3}{\omega_0^3}} \tag{5.15}$$

Comparing with the bridged-shunt peaking given in (5.11), this structure offers one more degree of freedom by k_R, and a good compromise between the selection of R_D and C_b can be achieved. Based on the numerator, this structure can generates two distinct zeros similar to the one in conventional shunt-peaking

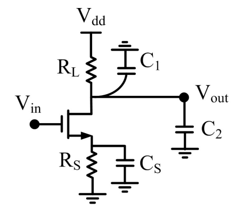


Figure 5.32: Source degeneration and its frequency response

structure. However, here in (5.15) more control over the placement of zeros is offered due to the parameter k_R which comes with series resistance R with the inductor L.

5.5.7.2 Peaking using Source Degeneration

It is desired to find an alternative for the bulky inductors. All is needed is generating a zero and placing it at or near the pole of the system. The source degeneration is a good candidate as it can produce a zero by placing a capacitor in parallel with its degeneration resistance. Assuming an R_s in parallel with C_s at the source of a transistor, it leads to a zero at frequency of $f_Z = 1/(2\pi R_s C_s)$. This is depicted in Figure 5.32 where $C = C_1 + C_2$.

With the assumption of $g_m \gg sC_{gs}$, the voltage gain is calculated as (5.16).

$$\frac{V_{out}}{V_{in}}(\omega) = \frac{g_m R_L(1 + sR_S C_S)}{(1 + sR_L C)(1 + sR_S C_S + g_m R_S)} \tag{5.16}$$

Indeed, adding an impedance of Z, the parallel combination of R_s and C_s, to the source of a common source amplifier change its trans-conductance from g_m to G_M and consequently its gain from $g_m(R_L \parallel C)$ to $G_M(R_L \parallel C)$, where G_M is given by (5.17).

$$G_M = \frac{g_m}{1 + g_m Z} = \frac{g_m(1 + sR_S C_S)}{(1 + sR_S C_S + g_m R_S)} \tag{5.17}$$

As it is obvious from this equation, adding a zero at f_Z introduces an extra pole to the system. However, the magnitude of this pole is $g_m R_s$ times bigger than the zero and by proper parameter design it can be placed outside of the frequency band of interest. This may come with reduction in gain and or increase the power

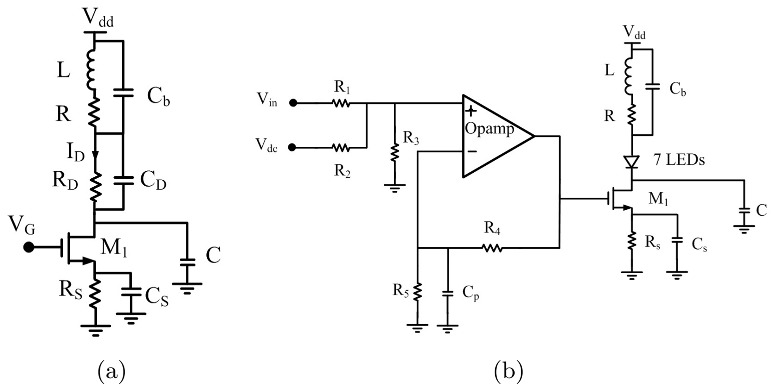


Figure 5.33: Proposed LED driver circuit using bridged-shunt-zero peaking

consumption of the circuit.

The combination of proposed bridged-shunt peaking together with source degeneration peaking yields a new design of peaking circuit in order to extend the bandwidth of the systems beyond their intrinsic limits. This proposed technique is shown in Figure 5.33(a). The passive elements connected to the drain of this circuit resembles the bridged shunt peaking and the one connected to the source is for generating zero using the passive components connected to the source of the transistor.

The trans-conductance gain from the current through resistor R_D to the input of transistor M_1 is calculated as (5.18) and (5.19), where $k_B = C_b/C$, $k_R = R/R_D$, $k_D = C_D/C$, $\omega_0 = 1/((R_D C))$, $m\omega_0^2 = 1/LC$, and $m = (R_D^2 C)/L$.

$$\frac{I_D}{V_G}(\omega) = \frac{g_m(1 + sR_S C_S)}{(1 + sR_S C_S + g_m R_S)} \times \frac{(1 + k_R k_B \frac{s}{\omega_0} + (\frac{k_B}{m})\frac{s^2}{\omega_0^2})}{D_p(s)} \tag{5.18}$$

$$D_p(s) = 1 + \frac{s}{\omega_0}(1 + k_D + k_R(1 + k_B)) + \\ ((1 + k_D)k_R k_B + (\frac{k_B + 1}{m}) + k_R k_D)\frac{s^2}{\omega_0^2} + (\frac{(1 + k_D)k_B + k_D}{m})\frac{s^3}{\omega_0^3} \tag{5.19}$$

In this circuit a good selection of k_B, k_R and k_D provides an optimum design with comprising the placement of poles and zeros. The inductor-less version of the

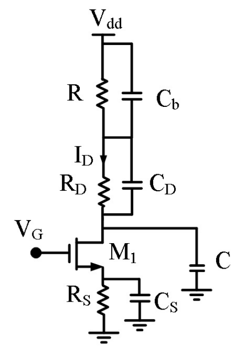


Figure 5.34: Inductor-less bridged shunt-zero peaking circuit

proposed peaking is depicted in Figure 5.34.

The transfer function of the LED current to the input voltage can be derived by setting $L = 0$ in the transfer function. The final result is given by (5.20).

$$\frac{I_D}{V_G}(\omega) = \frac{g_m(1 + sR_SC_S)}{(1 + sR_SC_S + g_mR_S)} \times \frac{(1 + k_Rk_B\frac{s}{\omega_0})}{1 + \frac{s}{\omega_0}(1 + k_D + k_R(1 + k_B)) + ((1 + k_D)k_Rk_B + k_Rk_D)\frac{s^2}{\omega_0^2}} \tag{5.20}$$

According to this equation, the exact location of zeros can be determined which are $f_{z1} = 1/(2\pi R_SC_S)$, and $f_{z2} = \omega_0/(2\pi k_Rk_B)$. This structure is applicable for scenarios in which the use of bulky inductors is prohibited. In order to apply this peaking circuit for driving the LEDs, the circuit of Figure 5.33(b) is proposed. According to this figure, input signal V_{in} will be shaped by the network of R_1, R_2 and R_3 resistors and then will be amplified by the gain of $(1 + R_4/R_5)$. The DC voltage V_{dc} will be shaped by the network of R_1, R_2 and R_3 as well and after amplification, its value will be superimposed by that of input signal. To keep operation in the linear region, the minimum level of output signal at the output of opamp should be higher than the threshold voltage of M_1. Also, for the 50Ω input matching, the values of this resistive network at the input of driver should be set as to have the equivalent input impedance of 50Ω. As depicted in this figure, seven series of "Cree $XLampML - B$" LEDs are used which are operated under the DC supply (V_{dd}) of

$25V$ and DC current of $100mA$. The MOSFET used in this implementation, M_1, is $BSP110$, and the opamp is $AD8009$. Most of the commercially available LEDs, which are considered as the load of driver, have a nonlinear I-V curve for all given input voltages; this makes it hard for the driver to achieve a linear response. The linear portion of the curve is defined from the turn on voltage to the start of its saturation region where the ramp of the I-V curve is constant. This driver makes it possible to provide the appropriate voltages across the linear range of the LED such that the output light intensity which is proportional to the LED current varies linearly with the input voltage. Comparing Figure 5.33(a) and 5.33(b), the model of an LED, is shown as the parallel combination of R_D and C_D. The degenerated common source configuration of this proposed circuit not only converts the voltage at the gate of M_1 into the current signal, but also helps to extend the linearity of the circuit. To increase the bandwidth for providing the high data rate VLC link, the previously mentioned peaking technique is utilized in this driver. The value of inductor can be calculated as $L_d = (R_d^2 C_d)/m$, and values of C_s and R_s can be calculated using the zero at the frequency of $1/((2\pi R_s C_s))$ which can be used to cancel the pole associated with the parasitic capacitance of LEDs. Moreover, the shunt capacitance C_p adds peaking at higher frequencies which helps in extending the bandwidth. However, high values of C_p causes the nonlinearity to the overall response and might cause some unwanted oscillations as well. Figure 5.35 shows the measured results of this proposed LED driver. Based on this frequency response, this driver is capable of achieving 42MHz of bandwidth which is 10 times higher than that of circuit without peaking.

Different structures of shunt, series, shunt-series and bridged-shunt series are presented in the literature. These topologies are used to help in extending the overall bandwidth of a system. Here a new structure which is called bridged-shunt zero peaking is introduced that takes advantage of the bridged-shunt peaking and the zero-peaking due to the source degeneration structure. This peaking technique is used to make an LED driver and based on the measurement results, the bandwidth of the LED driver increased by 10 times.

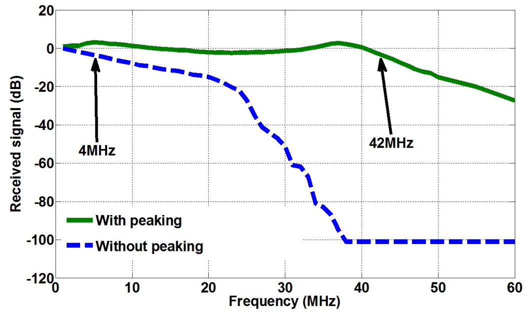


Figure 5.35: Frequency response of the proposed bridged-shunt-zero peaking

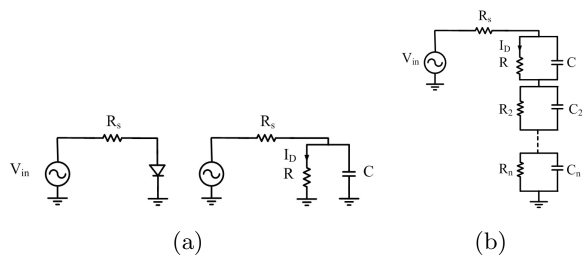


Figure 5.36: LED drives with pole zero cancellation

5.6 Bandwidth Extension by Pole Zero Cancellation

In this section, the technique of pole zero cancellation for enhancing the bandwidth of LED drivers is presented. As mentioned earlier, the bottleneck in achieving high bandwidth for LED drivers is the LED itself. First it is instructive to find the equation of the current through the resistive part of the LED. Figure 5.36(a) shows the series connection of an LED with the source resistance R_s. The ratio of this current to the input voltage is given in (5.21) which is corresponding to a pole at the frequency of $f_p = ((R_s + R))/(RR_sC)$. This pole puts a restriction on the maximum achievable bandwidth. It is desired to generate a zero in the transfer function of LED current to the input voltage such that the effect of this pole can be minimized. Figure 5.36(b) shows the connection of n series parallel RC elements with the model of LED. This has a potential of introducing zeros to the transfer function.

$$\frac{I_D}{V_{in}} = \frac{1}{(R + R_S) + sRR_SC} \tag{5.21}$$

For the case where $n = 1$, the transfer function of Figure 5.36(b) is calculated as (5.22).

$$\frac{I_D}{V_{in}} = \frac{1+\tau_1 s}{R_s(1+\tau_1 s)(1+\tau s) + R_1(1+\tau s) + R(1+\tau_1 s)} \tag{5.22}$$

According to this transfer function, one zero which is corresponding to the time constant of $\tau_1 = R_1C_1$ is generated. However, this addition of R_1C_1 generates one extra pole to the system. To achieve a high bandwidth, an optimized solution to the selection and design of two poles of the system and its single zero is needed. Design methodology is based on locating one of the poles outside the frequency band of interest and placing the other one at the vicinity of the zero. Equations (5.23) and (5.24) show the transfer function of Figure 5.36(b) for the case of $n = 2$.

$$\frac{I_D}{V_{in}} = \frac{(1+\tau_1 s)(1+\tau_2 s)}{D_2(s)} \tag{5.23}$$

$$\begin{aligned} D_2(s) = R_s(1+\tau_1 s)(1+\tau_2 s)(1+\tau s) + R_1(1+\tau_2 s)(1+\tau s) + \\ R_2(1+\tau_1 s)(1+\tau s) + R(1+\tau_1 s)(1+\tau_2 s) \end{aligned} \tag{5.24}$$

Based on this equation, for $n = 2$ the number of zeros increases to two and accordingly the number of poles increased to three. The same design methodology can be implemented here which is based on the adjusting the placement of zeros with that of poles such that the overall bandwidth is extended beyond its limit. A special case for Figure 5.36(a) is when all the time constants are equal which is $\tau_1 = \tau_2 = \cdots = \tau_n$. Assuming $R_1 = R_2 = \cdots = R_n$, and $C_1 = C_2 = \cdots = C_n$, and setting $R_s = 0$, the frequency response in this case is reduced to (5.25).

$$\frac{I_D}{V_{in}} = \frac{(1+\tau_1 s)}{R(1+\tau_1 s) + nR_1(1+\tau s)} \tag{5.25}$$

In this case, there is just one pole and one zero in the transfer function which

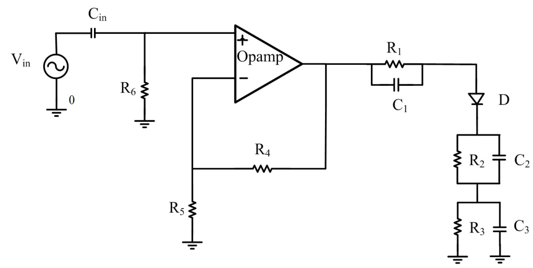


Figure 5.37: Proposed LED driver with pole-zero cancellation technique

are given by $(R + nR_1)/[(RR_1)(C_1 + nC)]$.

Overall, based on the selection of the passive components around the LED, it is desired to reduce the resistance of the source, R_s and to place the zeros in the vicinity of the associated poles. According to equations (5.22) and (5.23) the very small value of R_s reduces the order of the denominator which is equivalent to reducing the number of poles by one. Based on these considerations, the proposed LED driver with pole-zero cancellation technique is depicted in Figure 5.37. The value of R_s is minimized as the equivalent resistance at the output of the opamp is low.

The transfer function of this structure is given by (5.26) and (5.27).

$$\frac{I_D}{V_{in}} = \frac{R_4 + R_5}{R_5} \times \frac{(1 + s\tau_1)(1 + s\tau_2)}{D(s)} \tag{5.26}$$

$$\begin{aligned} D(s) = (R + R_1 + 2R_2 + R_s) + s[R_1(\tau + \tau_2) + R(\tau_1 + \tau_2) + \\ 2R_2(\tau + \tau_1) + R_s(\tau + \tau_1 + \tau_2)] + \\ s^2[R_1\tau\tau_2 + R\tau_1\tau_2 + 2R_2\tau\tau_1 + R_s(\tau\tau_2 + \tau\tau_1 + \tau_1\tau_2)] + s^3[R_s(\tau\tau_1\tau_2)] \end{aligned} \tag{5.27}$$

It is assumed that the output resistance of the opamp is low and the opamp is capable of providing the appropriate current for the LED. The input is matched to the 50Ω by setting $R_6 = 50$ and setting $R_4 \parallel R_5 = R_6$ for proper bias and offset balancing. According to this transfer function, the system introduces two zeros

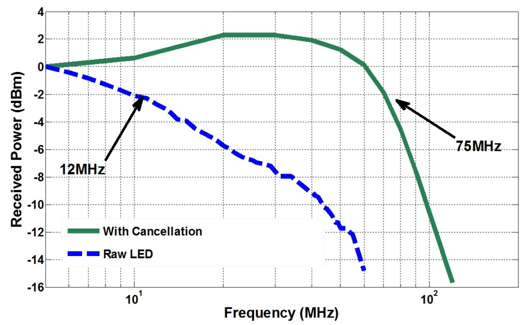


Figure 5.38: The frequency response with and without using pole-zero cancellation

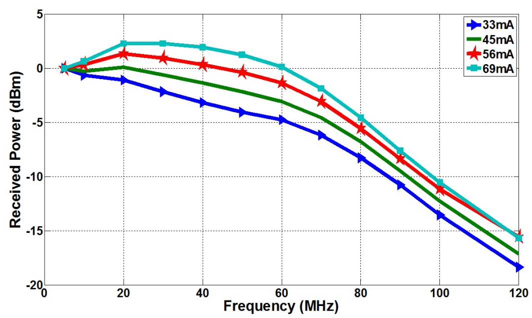


Figure 5.39: Frequency response comparison for different LED currents

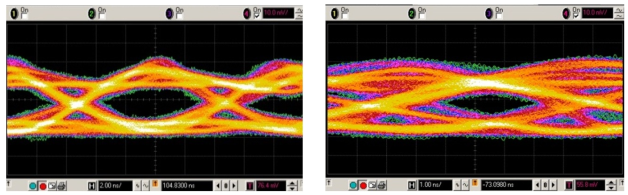
which can be used to extend the bandwidth. The measurement result for frequency response is shown in Figure 5.38. As it is shown in this figure, the bandwidth is enhanced from 12MHz to 75MHz using the pole-zero cancellation technique.

Figure 5.39 shows the frequency response of the proposed pole-zero cancelation for different values of LED current. The LED current can be set by the DC bias of the opamp. According to this figure, it is crucial to bias the LED in its linear range to get the best result.

For the measurement purposes, a 2^7-1 PRBS is generated and applied to the proposed LED driver. The measured eye diagrams with the BER of less than 10^{-3} are shown in Figures 5.40(a) and 5.40(b) for 100Mbps, and 160Mbps, respectively.

5.7 Bandwidth Extension using Time Interleaved LEDs

This section presents a novel optical access point transceiver that features addressable arrays of LEDs and photodetectors. The transmitter array enables combined



(a) 100Mbps (b) 160Mbps

Figure 5.40: Measured eye diagram of the proposed pole-zero cancellation technique

illumination control and serial data transmission for an array of 16 LEDs producing an aggregate data rate of 100Mbps. The receiver consists of a 16-element array of broadband receiver channels. Designed in a 0.5μm CMOS process to enable miniaturization and VLC system integration, the transceiver is capable of processing multiple user requests.

The proposed optical transceiver subsystem has been designed to feature the goals of VLC technology. This optical access point transceiver features an addressable transmit/receive matrix of LED and photodetector arrays. The transmitter array enables combined illumination control and serial data communication for an array of 16 LEDs producing an aggregate data rate of 100Mbps using a novel convolution-based discrete time interleaved driver circuit architecture. A negative feedback circuit provides regulated current for the LED driver to enable constant current control despite device parameter variation. To service the whole area within a room, multiple transceivers can be integrated with luminaires to enable data communication.

The transmitter has been designed to only transmit data/light signals when the room has been occupied by at least one user in the room. If no user is in the given spatial dimension, the data/light signal will be suspended and thus energy conserved. The downlink data, in the format of white light, will be sent from the transceiver to the user. However, the uplink signal will be sent via infrared signals from the users to the corresponding transceivers placed on the ceiling of the room. The optical receiver consists of a 16-element array of broadband receiver channels including a low-power TIA driving a differential output limiting amplifier with DC

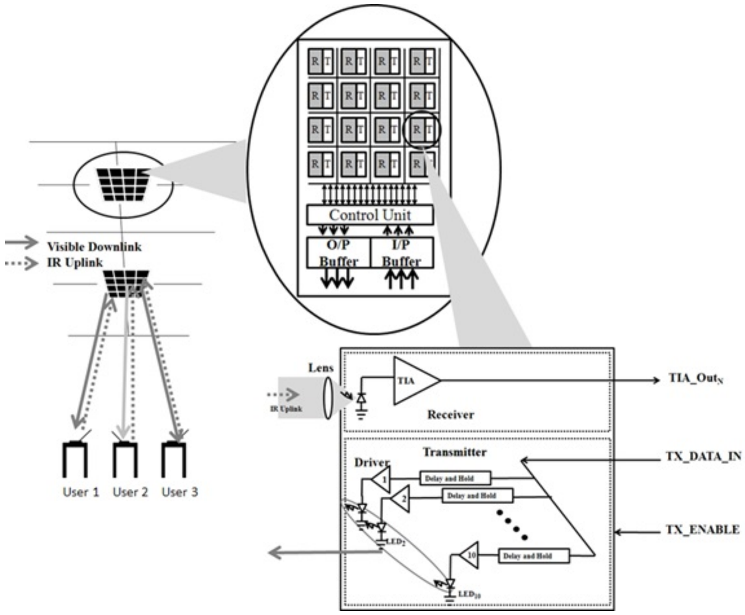


Figure 5.41: Conceptual diagram of the Smart Room with the proposed optical access point transceiver block diagram

offset cancellation. The access point transceiver is capable of processing multiple user requests by implementation of a winner-take-all control circuit topology. This system has been built to support multiple users within a given spatial dimension. The evolution of multiple user support will be expected to continually increase in parallel with the ability to achieve higher data rates. The transceiver was designed in a $0.5\mu m$ CMOS process to enable miniaturization and VLC system integration.

Recent published work on VLC system demonstrations have employed several techniques to extend data rates, including complex modulation schemes, equalization techniques, and optical filtering to remove the slow phosphor response [66, 68, 78]. However, most systems utilize off-the-shelf, disparate components integrated at board level with bulky bench top test/measurement equipment for demonstration. We present a cost-effective, low-power transceiver subsystem exhibiting a small form factor to enable integration into a network of luminaires for energy-efficient visible light communication.

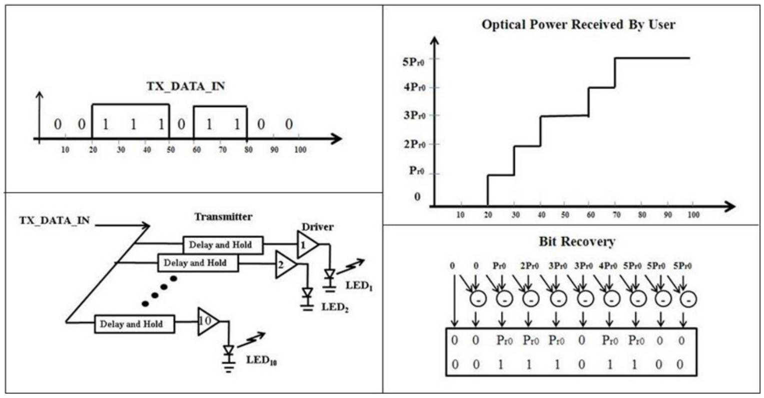


Figure 5.42: Time interleaved data coding based 100Mbps transmission scheme

5.7.1 Transmitter Design using Time Interleaved LEDs

5.7.1.1 Visible light communication based on data coding

The 4×4 transceiver array consists of 16 transmitters with 1 transmitter at each node. The goal is to be able to communicate by sending data at 100Mbps while providing sufficient light output. Most LEDs commercially available have a large internal capacitance resulting in much slower modulation frequencies. Different complex modulation schemes such as MIMO OFDM [79] and discrete multi-tone modulation (DMT) are proposed to compensate the low data rate of these conventional LEDs [80].

A scheme of having 10 LEDs, time interleaved at each transmitter node have been employed to mitigate this issue and provide sufficient light output as well. The time interleaved approach is pictorially explained in Figure 5.42.

The time interleaved scheme as shown in Figure 5.42 allows each LED to be on for $100ns$ rather than $10ns$ that would be required for 100Mbps transmission. This picture shows this scheme for 10 bits. In this figure the "0011101100" series of data is chosen to be sent. First bit, "0" will be sent after a delay of $10ns$ using the LED1, then the second bit, "0" will be sent after a $20ns$ delay using the LED2 and so on. The Received Optical Power in Figure 5.42 shows how the receiver sees the incoming signal of "01011". Finally the Bit Recovery shows the reconstruction of received signal. Basically each bit is extracted by subtraction of two consecutive received optical powers; it will be detected as "1" if the subtraction result is a nonzero value and otherwise will be regarded as "0". To understand the working of this scheme, consider a string of N bits corresponding to N LEDs used for the f/N reduction in switching frequency. Every Nth LED will transmit the corresponding Nth bit in the string after a delay of N/f seconds. Accordingly, the problem of having to transmit every consecutive bit at a fast rate is compensated by transmitting every Nth bit by the Nth source. Effectively the array of N LEDs transmits all the bits. In our design, we have chosen an array of 10 LEDs such that each LED transmits one of the 10 bits and holds it for $100ns$. The delays are implemented using inverters and D-flip-flops. The light signal received by the photodiode at the receiver end will have discrete values rather than digital logic levels. This makes the receiver design challenging but this method of communication is suitable for this application since the change in received average intensity per bit will not vary at a high rate.

5.7.1.2 Circuit design and simulation results

The LED driver consists of a negative feedback that maintains constant current and provides regulated current for the LED. OOK modulation is used to transmit the bit stream. The on signal is represented by a $50mA$ current through the LED. As mentioned before, this scheme has 16 pixels each having a receiver and a transmitter and each transmitter has 10 LEDs working in an interleaved manner. Three transmitters from the array consisting of 16 (4×4) transmitters will be selected by the control mechanism based on the strongest signal received from the user. Once these three transmitters are selected, the 10 LEDs from these 3 transmitters are used for communication whereas the other 13 transmitters can be used for ambient light by making its input signal high, essentially transmitting a string of "1"s.

Figure 5.43 shows the circuit diagram of one LED driver with the regulated feedback composed of transistor M_3, resistor R_s, and the opamp2, and the current mirror composed of M_2, M_4 and M_5 transistors. The $10ns$ Delay and Hold Block is used to generate the $10ns$ delayed signals for each LED, which is composed of NAND gate, Inverter and D Flip-Flops. These two D-flip flops and the $10ns$ delay signal are

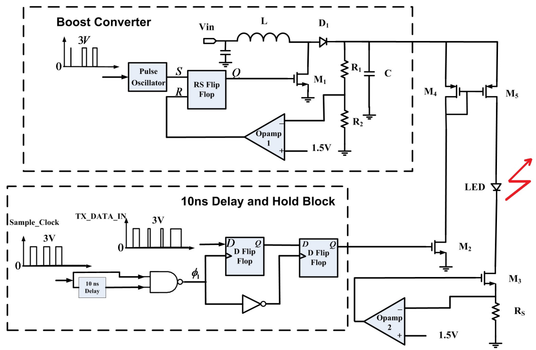


Figure 5.43: LED driver with current regulation

used to sample the correct bit for the particular LED source. In each pixel there are ten of these parts (Delay and Hold, current mirror and regulated feedback). A Boost converter composed of L, D_1, C and M_1 is implemented to provide $9V$ dc from the $3V$ supply voltage, named by V_{in} in Figure 5.43. Opamp1 with the voltage division of R_1 and R_2, the Pulse Oscillator and RS Flip Flop provide a local feedback for the boost converter. This Boost Converter is shared for the all 16 pixels of this scheme and in this converter the L, M_1 and C components are off chip. The 4×4 array consists of such drivers for each of the 160 LEDs. LED is modeled as the series combination of $3V$ DC source with the series resistor of 5Ω and a parallel capacitor of $20pF$. This LED has the optical efficiency of $73lm/W$; each pixel in this array will generate around 110 lumen and the whole array consisting of 16 pixels will have the 1700 lumen. Figure 5.44 shows a transient simulation of a single node of the 4×4 transmitters consisting of 10 LEDs with a PRBS generator as the input of the transmitter. As seen in the simulation, a bit string of "0011101100" is transmitted by 10 LEDs where LED1 transmits a "0" and LED2 transmits a "0" $10ns$ later, LED3 transmits a "1" $20ns$ later and so on up until the LED10 which transmits a "0" 90ns later such that all of these 10 bits are transmitted in the course of $100ns$.

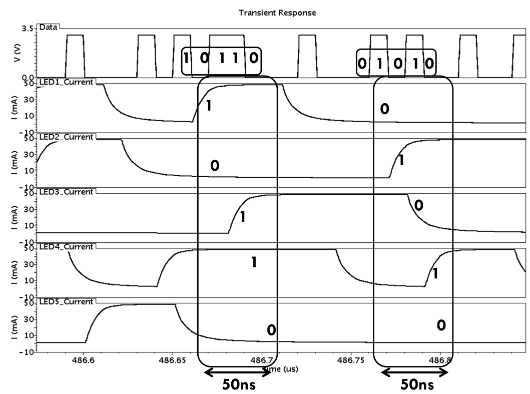


Figure 5.44: Transient simulation of the LED transmitter with a PRBS source

5.8 16-Level Pulse Amplitude Modulation of an LED Array

In this section, the pulse amplitude modulation (PAM) technique using an LED array which increases the data transmission rate from 10Mbps to 40Mbps is presented. This LED array also provides sufficient brightness for the applications in the office-sized locations. In the following the description of a video demonstration using our 16 LEDs array is explained.

Different complex modulation schemes such as OFDM for MIMO [79] and discrete multitone modulation (DMT) are proposed to compensate the low data rate of conventional LEDs, but they need bulky and complex system [80]. The objective of this work is achieving an appropriate link range using the base-band modulation schemes. In this section, the PAM applied to 4×4 LED array is presented in order to get the enough brightness and also data bit rate suitable for the indoor applications. The LED array can provide appropriate luminous flux levels compared with a single LED. This characteristic enables pulse amplitude modulation, increasing the transmission rate from 10Mbps to 40Mbps due to sending 4bits in each level. To show the pulse amplitude modulation with the proposed 4×4 LED array, an experimental demonstration of a video transmission system based on VLC using the LEDs array is reported.

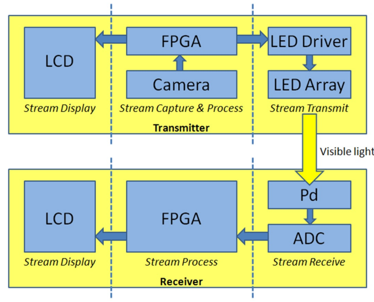


Figure 5.45: VLC system block diagram for PAM implementation

5.8.1 VLC System Description for PAM Implementation

5.8.1.1 Overview

The video transmission system based on VLC using a 4×4 LED array is depicted in Figure 5.45. It consists of two parts of transmitter and receiver. Both the transmitter and receiver comprises three blocks as shown in this figure. At the transmission side, the FPGA (Stream Capture and Process Block) receives the real-time video stream captured by the camera and sends it to the LCD (Stream Display Block), which is called the original video stream. Meanwhile, it modulates and processes the data stream, and sends it to the LED driver (Stream Transmit Block). Modulated information will then be transmitted through the light path and will be received by the commercial Photodiode (PD) in series with a high speed ADC (Stream Receive Block). The ADC will pass the converted digital data stream to FPGA (Stream process Block). Eventually, the data stream will be demodulated and sent back to the LCD (Stream Display Block) , which is called restored video stream.

A comparison is done between the restored video stream at the receiver side and the original video stream at the transmission side to prove that the VLC system works. The transmission rate was bandwidth-limited on the transmission side because of the LED itself. This challenge is overcome by implementing an LED array with pulse amplitude modulation instead of a single LED using simple ON-OFF Keying modulation.

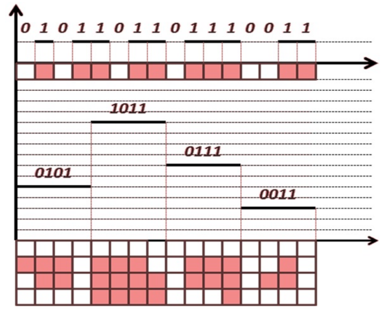


Figure 5.46: OOK versus pulse amplitude modulation

5.8.1.2 Modulation Scheme

For a simple OOK, one bit is transmitted each time. A digital one is represented when the LED is on while a digital zero means turning the LED off. With pulse amplitude modulation using our 16 LED array, four bits are managed to be transmitted in one clock period. This is shown in Figure 5.46.

While transmitting 4 bits "0101" in 4 clock period using the ON-OFF Keying method, pulse amplitude modulation enables the data to be transmitted in one clock period as level 5. In the same manner code "1011", "0111", and "0011" corresponds to the level 11, level 7 and level 3, respectively. In Figure 5.46, the grids below the waveform simulates the 4×4 LED array. A red square means the LED is on while the white square means the LED is off. For instance for this 4 bits "0101", just five LEDs are on and the rest are off.

5.8.1.3 Stream Transmit Block

The analog transmitter is composed of LED driving circuits and a 16 LEDs array. A heat sink is integrated in the PCB design to help out the heat removing process. The analog transmitter board is shown in Figure 5.47. The LED driver which acts as a transmitter in this system drives the LEDs based on the incoming signal from the FPGA. This driver is composed of 16 identical LEDs. Each LED is driven by a single identical driving circuit which keeps its low complexity. The 16 LEDs are gathered as close as possible to generate a linear light output.The light emitted from each LED is controlled by the MOSFET; the driving circuit for each LED is a

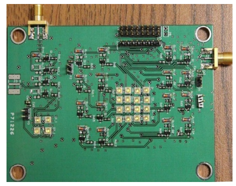


Figure 5.47: LED driver PCB for 16-level PAM

common source structure with a zener diode to protect the LED from overdriving. Each LED is in series with one MOSFET, a limiting resistor and power supply. Appropriate MOSFETs should be chosen to match the electrical characteristic of LED. Also it is necessary to choose a large bandwidth MOSFETs such that there was not any limitation on the performance of the driver in this regard. All the 16 LEDs are divided into two groups and each group can be controlled separately based on its power supply, while all the 16 LEDs are individually controllable. This will allow us to turn on just 8 LEDs or all 16 LEDs. The incoming signal from FPGA goes directly into the gate of MOSFET and generates a current proportional to the level of incoming voltage. In this design, the LED with part number of $LUWCN5M$ from Osram semiconductor and the MOSFET with the part number of $2N7002$ is used.

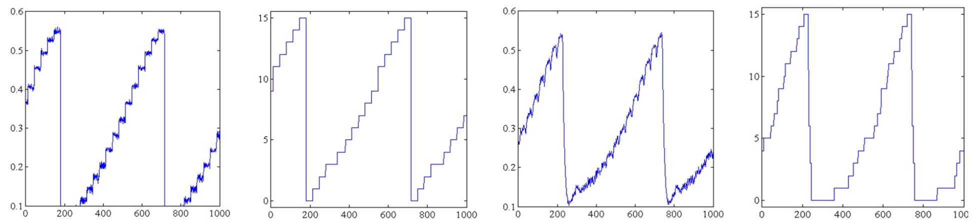
5.8.1.4 Stream Receive Block

The analog receiver has a concentrator lens ($ACL2520 - A$), a commercial photodiode receiver ($APD110A2$) and a high-speed ADC. A concentrator lens is used for gathering all the light of LEDs and collimating at the receiving point of the photodiode. A blue filter also used to increase the bandwidth for high speed data transmission. A commercial photodiode is used at the reception side because of its high gain, which saves to build an extra amplifier after the photodiode. The analog signal received by the photodiode is converted to a digital signal by the use of the high-speed ADC ($AD9248$). This digital signal is then sent to FPGA for further processing and reconstructing of data.

5.8.2 Experimental Results for 16-Level PAM

On the transmit side, the transmitter captures the video stream and sends it to the FPGA for modulation; the modulated signal in the format of PAM is sent to the LED driver. On the receive side, the incoming signal after passing through the lens and blue filtering enters the photodetector. The lens is aimed to concentrate the light to the reception point of the photodetector. Then, the receiver gets the amplified signal and send it to the second FPGA for the demodulation process. Finally the restored video stream goes to the LCD. By testing the system using OOK modulation, a clear restored video stream without noise and with the transmission rate of 10Mbps is captured. It is worth mentioning that this data rate without using the blue filter was 6Mbps. The link range is about 1 meter with the commercial photodector ($APD110A2$). With pulse amplitude modulation using the 4×4 LED array, the 40Mbps data streaming is demonstrated, but just with some background noise. The overcoming of this noise is achieved with adding a software processing procedure after the ADC at the reception side. Both the original restored waveforms generated by photodetector and modified restored data generated after software processing procedure are compared and shown in Figure 7 to illustrate the result. In Figures 5.48(a) and 5.48(c), the waveforms are the analog outputs after the photoderector block. And Figures 5.48(b) and 5.48(d), show the modified digital outputs after being processed by the software. Comparing Figures 5.48(a) and 5.48(c), more noise is seen as the transmission rate increases from 100kbps to 6Mbps. After processing using the software, those noise are cleared, which can be seen in Figures 5.48(b) and 5.48(d).

In summary, we reported a video transmission system based on visible light communication. The system utilizes pulse amplitude modulation instead of traditional OOK modulation with a 4×4 LED array. The new modulation helps to increase the transmission rate from 10Mbps to 40Mbps. Unexpected noises are detected when utilizing the pulse amplitude modulation which is overcomed by using a software processing procedure at the reception side.



(a) $100kbps$ raw restored data after PD (b) $100kbps$ modified restored data (c) $6Mbps$ raw restored data after PD (d) $6Mbps$ modified restored data

Figure 5.48: Raw restored data after PD versus modified restored data after software processing procedure

5.9 Conclusion

Different bandwidth enhancement techniques are reviewed in this chapter such as negative impedance converter (NIC), equalization techniques, peaking and pole-zero methodologies. It is mentioned that the source of limitation is the LED and design techniques at the transmitter or receiver should be employed to alleviate the limitation. The NIC is promising structure which generates negative capacitances and by putting its output in parallel with the LED, the parasitic capacitance of LED will be degraded in full or in part, either of them helps in extending the bandwidth. Pre and post equalization techniques such as multiple resonant, and active and passive equalizations are methods which compensate the roll-off in the transfer function of raw-LED, leading to bandwidth extension. Complex modulations such as OFDM/DMT are proved to have dominant role in enhancing bandwidth. However, their implementation is bulky, expensive and complex. Accordingly, different alternative methods are invented to compensate the low bandwidth density of base band modulation schemes; carrier sweep out techniques is one of them which yield high bandwidth by decreasing the rise and fall times. Pulse shaping, described in this chapter, is yet another method in the regime for enhancing the overall bandwidth of the VLC link by shortening the rise and fall times. Peaking techniques such as shunt, series, (bridged) shunt-series and triple resonant peaking techniques are also hired during last decade or so to achieve a high bandwidth. A peaking technique called bridged-shunt-zero peaking is presented in this chapter which is suitable for implanting in the LED driver circuits. The pole-zero technique in extending the bandwidth is explained and one LED driver with enhanced bandwidth is proposed. The pole-zero cancellation in general generate zero in the transfer function and extend the bandwidth by canceling the associate pole. Time-interleaved which works based on sending "1"s and "0"s with a fixed delay time is also introduced as a method which can compensate the low bandwidth of LED.

Chapter 6

Demonstrations

In this chapter two distinct test-beds which are the joint work with BU and RPI are presented. The first one is implementation of the link using software defined radio. And the second one is implementing a wireless access test-bed with dimming compatible OFDM. In these demonstrations, our work was centered on designing and developing the transmitters. For the receiver part, we have either used the boards designed by RPI or we have used the commercial photodetectors. And the system design and characterization are carried out by the BU.

6.1 Implementation using Software Defined Radio (S-DR)

Software defined radio (SDR) has proven to be an effective and practical tool in RF communications, essentially allowing flexible and rapid exploration of dynamic RF signal processing techniques while accelerating the advancement of configurable RF antennas and front-end hardware. The software-defined concept can also be adapted to other physical communication media; we investigate a software defined visible light communications (SDVLC) solution that implements an optical front-end to adapt SDR platforms to the constraints of an optical wireless (OW) channel using the visible spectrum. Utilization of an SDVLC platform allows the VLC link to be dynamically modified in order to meet requirements of a dual-use system providing both data communications and illumination. The platform also enables concurrent development of signal processing techniques and front-end hardware within an integrated testbed. This modularity, along with the ability to quickly bring up an OW system and implement new test scenarios, makes SDVLC a powerful concept for facilitation of research and experimentation with VLC. We describe the use of our SDVLC system to investigate tradeoffs in the delivery of room lighting and simultaneous adaptive modulation. Given the early stage of development in the area of VLC and the complexities involved in implementing signal chain components in a testbed, we have found a need for tools to accelerate the development and testing of VLC prototypes, solutions and protocols. Software-defined systems offer an efficient low-cost platform with the flexibility to assist in development by (a) providing a modular separation of front-end hardware and signal processing techniques, (b) offering the agility to modify and test various signal processing techniques without any hardware updates, and (c) allowing for dynamic variations of the signal processing techniques in order to adapt to changes in the lighting requirements.

6.1.1 SDVLC Hardware Architecture

Figure 6.1 shows a high level signal chain for a software defined communication link. From a hardware perspective, the major differences between an SDR link and a link in an SDVLC system are that (a) the up-converter and down-converter (*i.e.*, carrier frequency modulation) can potentially be ignored in the SDVLC system, and (b) the front end hardware is either a set of RF antennas for SDR or an optical transmitter and receiver for SDVLC.

6.1.1.1 Transmitter Architecture

The emergence of interest in dual-purpose VLC systems has generated a need for optical devices that meet the requirements of both high speed communications and illumination. As such, this application introduces new challenges in the development of LED driver circuits. The ideal driver will combine techniques from high speed R-F transmitters and illumination-grade luminaires. RF transmitters are an essential

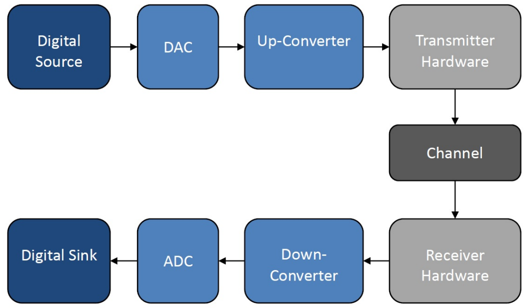


Figure 6.1: High level signal chain for a software defined communication link

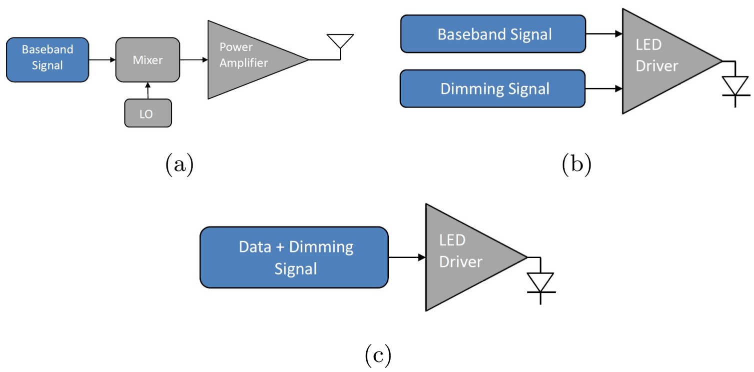


Figure 6.2: (a) Signal chains for an SDR transmitter, (b) an SDVLC transmitter with dimming and data as separate inputs, (c) an SDVLC transmitter with a single input with combined data and dimming signal

part of a modern communication system. Designed and assembled from core RF components, RF transmitters have various architectures. The conventional architecture for a transmitter consists of a baseband/modulator, a mixer/up-converter, a power amplifier and an antenna as shown in Figure 6.2. If the transmitter is designed to send amplitude-modulated or multi-carrier signal, the power amplifier must have adequate linearity. This power amplifier may be implemented as multi stage to provide the linearity and also enable a good matching to the antenna; however, this increases the complexity of the design. One of the key merits of optical wireless systems, which operate at baseband, is the relatively low transceiver complexity and low energy-per-bit required for data transmission compared to RF systems.

Models of transmitters for VLC are also shown in Figure 6.2. The challenge in the design of these transmitters is to provide a good trade-off between the communication and illumination benchmarks. Both data and desired dimming level determine the optical signal. Note that the brightness and data input can be (a) processed independently as input to an LED driver capable of controlling both signal and dynamic range, or (b) processed together in the signal processing unit to generate a single drive signal. The latter provides more flexibility for the signal processing unit, which is ideal in a software-defined system. The design proposed in [41] is a case which is capable of combining the data signal and illumination level digitally to maintain data transmission over a wide range of illumination levels. VLC drivers can also be implemented for either analog or discrete level output. Again, the former provides the ideal flexibility of a software-defined system; however, the latter can be designed with improved bandwidth and still provide some degree of flexibility for analysis of schemes such as VPPM. Regarding the transfer function of the LED drivers we have implemented for analog modulation schemes, the conversion is nonlinear across the attainable output range of the LED; however, there is typically a near-linear range that can be used without equalization. This is due to the relationship between voltage and current through the MOSFET as well as the relationship between forward current and optical power provided by an LED.

6.1.1.2 Receiver Architecture

Software defined communication, by definition, needs to be adaptive to multiple communication standards and modulation schemes. Unlike conventional optical receivers, therefore, receivers for the SDVLC system need to maintain certain linearity characteristics analogous to specifications for a SDR. A software-defined receiver typically consists of an analog front end and a digital signal processing (DSP) unit as shown in Figure 6.3. This section proposes the design of such an optical front end adaptive to multiple standards in a software-defined scenario and focuses on its implication on signal processing performance in the digital domain.

Figure 6.4 depicts a typical optical front end consisting of a photodiode followed by a transimpedance amplifier (TIA) and a limiting amplifier (LA). Despite

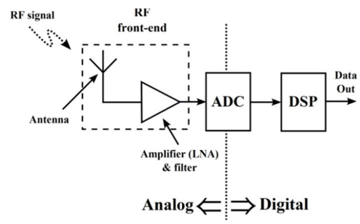


Figure 6.3: SDR RF receiver front-end

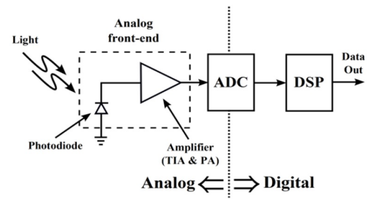
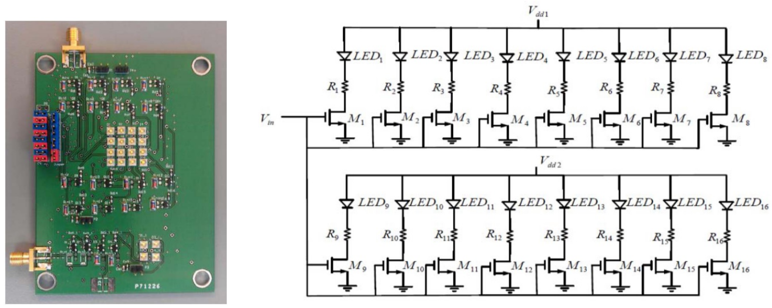


Figure 6.4: SDVLC optical receiver front-end

the similarities, however, there are some subtle differences between an optical and RF front end. Since light intensity cannot be negative, the current generated by the photodiode can only be unidirectional. Therefore, a DC illumination is generally necessary for analog modulation to ensure that the signal is not clipped. Moreover, in an IM/DD system, the carrier frequencies are located in the baseband [81], eliminating the necessity of oscillators and down-conversion mixers as used in a typical SDR system [82]. Most importantly, the limiting amplifier (LA) in conventional optical receivers is designed to be heavily non-linear. Although efficient for binary modulation schemes such as OOK, these amplifiers will generate severe distortion in single/multi-carrier modulation with envelope variation. The non-linearity in an optical receiver chain, however, can result from any part of the circuit including the photodiode.

6.1.1.3 Transmitters

The LED driver in Figure 6.5 acts as an analog optical transmitter. It is composed of 16 identical LEDs, each tied to the same drive signal and in series with a MOSFET (M), a limiting resistor (R) and power supply. The light emitted from each LED is controlled by the MOSFET which generates a current proportional to the level

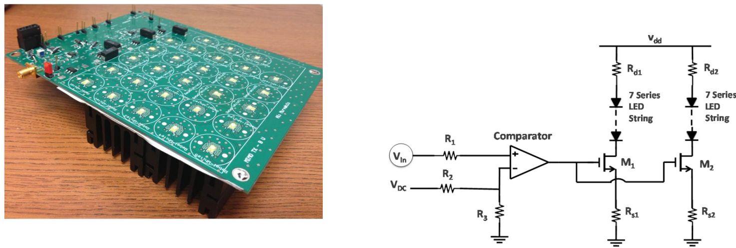


(a) (b)

Figure 6.5: First analog LED driver for SDR demonstration: (a) LED driver PCB, (b) LED driver circuit

of incoming voltage from the USRP. This voltage has a DC component as well as an AC component. The DC keeps the transistor in its saturation region and the AC component modulates the LED. The 16 LEDs are divided into two groups that can be powered by separate supply voltages (V_{dd1} and V_{dd2}), while the gates of all 16 MOSFETs are connected together. In this design, LEDs are from Osram Semiconductor, $LUWCN5M$, and MOSFETs are $2N7002$.

The second driver that we have investigated is shown in Figure 6.6. In this design, a high speed comparator ($LT1116$) is used to increase the level of incoming signal to the appropriate threshold necessary to turn on the MOSFETS (M_1 and M_2). The sensing resistor, R_s, is designed to provide the local feedback and the role of resistor R_d is to limit the current passing through the LEDs. There are 7 LEDs put in series with the MOSFET to provide the required brightness. To prevent noise from turning on the LEDs, the V_{DC} voltage is used to set the decision point after which the output of comparator goes high in order to turn on the MOSFET. The MOSFET used is $ZVN4210G$, and the LEDs are $LuxeonRebelES$. The PCB of this design uses two sets of the circuit shown in Figure 6.6 in order to provide the required illumination of 400Lux at a distance of $2m$. Note that this driver does not have the flexibility of the former but it is better suited for Binary level PWM schemes such as VPPM.



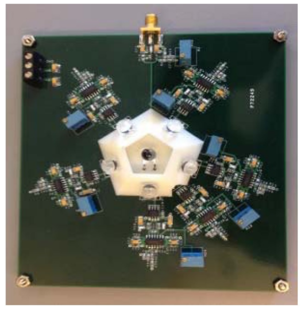
(a) (b)

Figure 6.6: Second analog LED driver for SDR demonstration: (a) Two-level LED driver PCB, (b) Two-level LED driver circuit

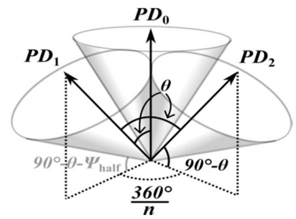
6.1.1.4 Receivers

Regarding optical receivers, we have used a commercial device as well as a device developed to explore channel selection due to the directionality of the medium. We first used the commercial photodetector (Thorlabs $PDA36A$) with an aspheric condensing lens (Thorlabs $ALC2520-A$). The detector employs a PIN silicon photodiode with active area of $13mm^2$ and a responsivity of $0.2-0.4A/W$ in the visible range, depending on wavelength of incoming light. It is set in a transimpedance amplifier configuration with adjustable gain. We use the highest gain setting for which the receiver has sufficient bandwidth to match the transmitter. That is the 10dB gain setting, at which the bandwidth is 12.5MHz. A diversity receiver was also designed in order to study the effect of signal combining in VLC. Figure 6.7 shows the diversity receiver with 6-links, each composed of a photodiode (PD), TIA and variable gain amplifier (VGA). Signals from all channels are combined by a summer circuit. To optimize SNR, maximal-ratio-combining technique is utilized by tuning VGA gain. In order to ensure uninterrupted coverage, the number of channels was carefully chosen. Placing one photodiode in the middle and arranging "n" photodiodes around it with their axes tilted from each other by "θ" degrees (also shown in Figure 6.7), the following relationship can be derived:

$$n = \frac{2\pi}{\cos^{-1}(\frac{\cos\theta}{1+\cos\theta})} \tag{6.1}$$



(a)



(b)

Figure 6.7: Receiver: (a) Diversity receiver PCB, (b) FOV design model for an arbitrary n

With a reasonable choice of $\theta = 50^o$ owing to fact that the half angle (Ψ_{half}) of the Hamamatsu $S6036$ photodiode is 25^o, n is calculated to be 5.37. After rounding to $n = 5$, the ideal θ is found to be $\sim 43^o$. Therefore, a total of 6 photodiodes (including one photodiode in the middle) need to be placed at $\sim 43^o$ from one another to cover a solid angle of $4\pi \sin^2((\theta + \Psi_{half})/2) = 3.9sr$. This means about 60% coverage over the planar surface of the receiver.

Since the input pole of the transimpedance amplifier ($AD8015$) is at about 85MHz with 110Ω input impedance and $17pF$ capacitance, the bandwidth of the receiver front-end is mainly limited by the photodiode (25MHz). With an extrapolated input referred noise of $20pA/\sqrt{Hz}$ at $17pF$ input capacitance and $0.56A/W$ photodiode responsivity, the sensitivity of the front end is about -38dBm for 25MHz bandwidth. Since all the photodiodes will not be at line-of-sight simultaneously, summing the response of all the links with equal gain will result in degraded SNR. Therefore, a dB-linear gain controlled VGA ($LMH6503$) is used after the TIA. With a tunable gain of -80dB to 20dB, any link can be completely shut down or amplified 10-fold for optimal SNR. The summer circuit is implemented with a 1.5GHz gain-bandwidth product Opamp ($LMH6624$). Since the feedback factor of the inverting configuration adder circuit scales down by a factor of the number of channels, the bandwidth also reduces. However, it was made sure that the bandwidth was enough for at least 10MHz operation.

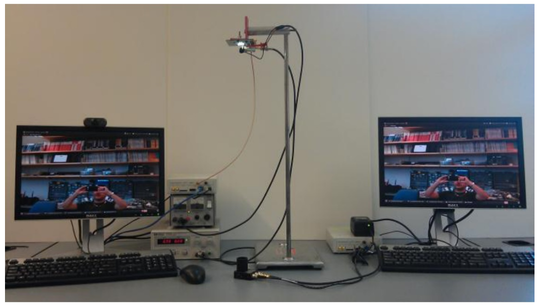


Figure 6.8: Software defined VLC implementation

Figure 6.8 shows the development of an SDVLC system, which uses SDR tools to implement, integrate, and operate VLC links.

6.1.2 Additional Applications

The SDVLC system as described here has potential for future testing of many other system level VLC applications [3]. One application under consideration is an implementation of a VLC system that optimizes its signal processing scheme to best fit the channel and to dynamically maximize data rate. Due to the large dynamic range of the VLC channel, an ideal system should account for close proximity LOS paths as well as highly attenuated signals at the outer reaches of a VLC cell or multipath signals. As a simple example, a system implementing PAM modulation technique could dynamically change the symbol set size from 4-PAM to 8-PAM under high SNR conditions (close proximity LOS) or to OOK in low SNR scenarios (high attenuation and multipath). The agility of the SDVLC system allows this type of dynamic processing to be achieved. The SDVLC system can also be applied for dynamic channel selection with the optical diversity receiver. Based on the effect that angle of arrival has on the received signal and the assumption of dynamic rotation of a user device, appropriate selection of a subset of sensors with the transmitting luminaire in its FOV can be implemented in software mitigating noise from unused sensors. Development of software defined implementations for various physical media is necessary for exploration of heterogeneous systems and Software Defined Networks.

6.2 Wireless Access Testbed through Visible Light and Dimming Compatible OFDM

VLC technology has a potential to complement the RF wireless technology for indoor coverage. It promises concurrent illumination control and wireless data transmission capabilities. The potential of advanced multi-carrier modulation techniques, *i.e.* OFDM, introduces new challenges in the development of driver circuits. The reverse polarity optical OFDM (RPO-OFDM) is a recent approach to realize compatibility between the analog OFDM signal and the industry well-known pulse-width modulation (PWM) for dimming control. In this section, we present the implementation of a wireless access testbed through visible light and dimming compatible RPO-OFDM. A driver topology capable of driving a string of LEDs using a RPO-OFDM signal is proposed. The driver alleviates the nonlinearity of LEDs by proper biasing and maintaining a quasi-linear range of operation, *i.e.* minimizes the OFDM signal clipping. Using a software defined radio (SDR) platform for online modulation and demodulation, and limit for a range of un-coded quadrature amplitude modulation (QAM) constellations, the experimentally obtained measurements demonstrate linear wide-range dimming while independently maintaining a bit-error performance below the forward error correction (FEC). Error free BER performance without symbol level equalization is obtained for binary phase shift keying (BPSK) and 4-QAM.

6.2.1 Introduction

OFDM is a promising multi-carrier modulation technique for VLC systems due to, for example, its high spectral efficiency and resistance to inter-symbol interference (ISI). In OFDM-based VLC systems, and assuming a limited LED bandwidth and high-quality signal from illumination requirement, high data rates are supported through parallel transmission of high-order multilevel quadrature amplitude modulation (M-QAM) symbols on orthogonal sub-carriers. However, the complex-valued OFDM signal used in RF is not suitable for IM/DD as the LED driving signal must be real and positive. Therefore, real-valued OFDM optical formats suitable for IM/DD are proposed. In the optical domain, the conventional bipolar DC biased optical OFDM (DCO-OFDM) offers full spectral efficiency and low power efficiency due the DC component [83]. Half spectral efficiency and higher power efficiency are achieved using the unipolar asymmetrically clipped optical OFDM (ACO-OFDM) [84] and pulse-amplitude-modulated discrete multi-tone (PAM-DMT) [85]. However, polar OFDM (P-OFDM) and hybrid ACO-OFDM (HACO-OFDM) offer full spectral efficiency as well as high power efficiency, *i.e.* same as DCO-OFDM without the need of DC-biasing [86], [87]. In addition to a high spectral and power efficient optical OFDM formats, a major design challenge that limits the commercialization of VLC is incorporating dimming techniques widely adopted in the lighting industry while maintaining a broadband and reliable VLC links. Specifically, the challenge is the development of hybrid modulation techniques incorporating the pulse-width modulation (PWM) for dimming control and the OFDM signal for data communication. The recently proposed reverse polarity optical OFDM (RPO-OFDM) utilizes the entire PWM cycle for data transmission (data communication is taking place during the on-time as well as during the off-time of the PWM signal) [88]. Moreover, the full LED dynamic range of operation is utilized to minimize the nonlinear distortion (clipping) of the OFDM signal. In this section, we realized a wireless access testbed through visible light and dimming compatible RPO-OFDM. In this real-time testbed, the hardware components include a PCB luminaire and a software defined radio (SDR) platform based on the universal software radio peripheral (USRP) module. A single USRP is used as a VLC transceiver. The RPO-OFDM signal is generated in MATLAB and Simulink is used to interface with the USRP. The output of the USRP is applied to the PCB luminaire and the output after the optical detector is applied to the input of the USRP. The PCB luminaire provides the 50Ω input matching, amplifies the incoming RPO-OFDM signal and adds a DC level to insure quasi-linear range of operation. Targeting 10^{-3} BER, and for a range of QAM modulation orders up to 16-QAM, a linear dimming range from 90% down to 12.5% is experimentally demonstrated.

6.2.2 Dimming and Modulation in VLC

6.2.2.1 Optical Communication Constraints

Optical communications such as VLC implement IM/DD [71]. Letting $x(t)$ represent instantaneous optical power, or intensity of an illumination quality LED source, the constraint $x(t) \geq 0$ holds for all t. The illumination source also has a constraint $x(t) \leq P_{max}$, where P_{max} represents the maximum optical power output of the LED or luminaire. In addition, the optical conversion function is typically nonlinear near the minimum and maximum optical power levels. These constraints imply that conventional bipolar modulation schemes must be biased and conditioned in order to mitigate clipping and distortion. In the case of dual-use VLC systems, the constraint $E[x(t)] \sim P_{ave}$ must also be satisfied in order to meet requirements of the lighting system. VLC modulation is also constrained by the resolution of the transmitter. Many commercial LED drivers are designed with 2-level outputs and dimming is controlled via PWM where the duty cycle of the pulse is varied. While discrete level modulation schemes such as OOK or pulse position modulation (PPM) are viable with two output levels, more complex modulation schemes require higher resolution. This driver resolution, or the resolution of the digital-to-analog converter (DAC) in cases where the optical converter is driven by an analog signal, constrains the potential levels of the modulated signal. The frequency response of the VLC transmitter is often the limiting factor when considering the rate of a VLC link. The typical response time of the optical conversion (*e.g.*, LED emission or phosphorescence) leads to a 3dB frequency response in the range of 5-12MHz, hence VLC is conventionally constrained to real-valued baseband signals. Data rates of pulse-based schemes are limited by this frequency response since distortion occurs for symbols that span a wide frequency range; however OFDM techniques benefit from separation in the frequency domain and have been shown to transmit signal components beyond the 3dB bandwidth using techniques such as bit loading where higher frequency components utilize lower order modulation schemes [89].

6.2.2.2 Modulation Schemes

Various modulation schemes have been proposed for use in VLC. Pulse-based schemes such as pulse amplitude modulation (PAM) and PPM offer relatively simplistic processing techniques for encoding \ decoding. Modifications to these schemes have also been proposed in order to incorporate dimming capabilities. Varying the DC bias of a PAM or PPM signal will alter the average optical output power; however the dynamic range must be conditioned to minimize clipping. Dynamic range affects the received signal and, accordingly, the signal-to-noise ratio (SNR) performance of the link. Variable PPM (VPPM) sets the duty cycle of a PPM pulse in order to meet average optical power requirements and has been proposed in the IEEE 802.15.7 standard [90]; however, varying the pulse width also changes the Euclidean distance between symbols and, accordingly, link performance.

The multi-carrier OFDM technique offer a distinct advantage over pulsed schemes in regards to the use of individual frequency bins. This mitigates signal distortion from the nonlinear frequency response by utilizing many subcarriers such that the modulated signal on each subcarrier has a relatively linear response. This allows the OFDM signal to utilize frequency components beyond the 3dB bandwidth without severe distortion of the signal components from any individual subcarrier. In optical communications, techniques such as DCO-OFDM and ACO-OFDM [83, 84] have been developed to satisfy many of the optical communications constraints; however additional modifications are required to dynamically adapt to average optical power constraints. RPO-OFDM is a proposed technique that combines ACO-OFDM with PWM in order to satisfy both the channel and illumination constraints of a dual-use VLC link.

6.2.2.3 Reverse Polarity Optical OFDM

RPO-OFDM is proposed to combine the fast optical OFDM communication signal with the relatively slow PWM dimming signal, where both signals contribute to the effective LED brightness. The building blocks and the method of deriving this RPO-

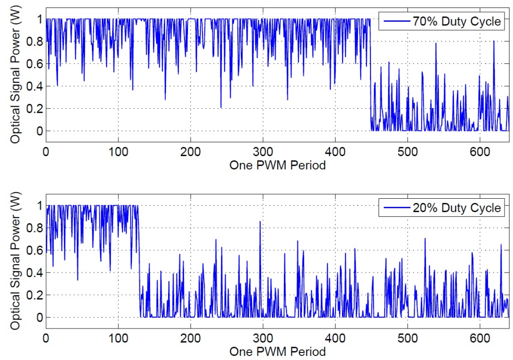


Figure 6.9: Optical RPO-OFDM signal waveform based on ACO-OFDM at 70% (upper) and 20% (lower) duty-cycles

OFDM are explained in details in [88]. The basic idea is superimposing the OFDM signal on top of the PWM dimming signal. For example, and assuming an ACO-OFDM signal and a known dimming set point, convenital ACO-OFDM symbols are superimposed during the off-time of the PWM signal and flipped (reverse polarity) ACO-OFDM symbols are added during the on-time of the PWM signal.

RPO-OFDM can be applied to any optical OFDM signal including the bipolar DCO-OFDM. The same modulation-demodulation sequence is valid for a DCO-OFDM signal. However, and compared to ACO-OFDM symbols, two consecutive PWM periods are required to transmit the DCO-OFDM symbols, *i.e.* in order to include the positive as well as the negative time-domain samples of the DCO-OFDM symbols. While maintaining positive synchronization signals suitable for IM/DD, conventional fine and course synchronization techniques used in RF can be adapted and applied for frame/symbol synchronization. Figure 6.9 shows the RPO-OFDM for two different dimming ratios of 70% and 20% duty-cycles of the PWM period.

6.2.3 PCB Based Luminaire

The emergence of modern illumination applications for LEDs and the complex modulation techniques used for data transmission in the VLC systems, introduces new challenges in the development of driver circuits. The digital modulation schemes such as OOK are compatible with standard PWM dimming technique, and the data-dimming combination can be implemented in the circuit level design for ei-

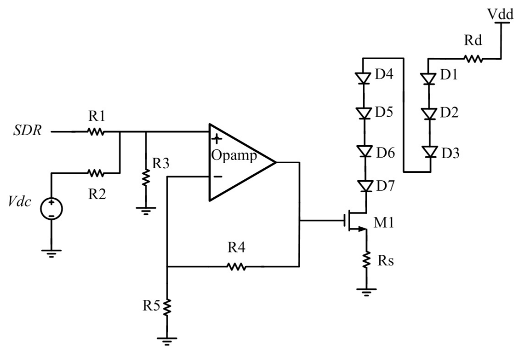


Figure 6.10: The schematic diagram of proposed LED driver for dimming compatible OFDM

ther analog input dimming [40], [41] or digital input dimming [39]. Similar design can be applied to the analog modulation schemes as well. As mentioned earlier, the combination of data signal with the PWM dimming signal, *i.e.* RPO-OFDM, is done in the MATLAB and the output is transferred into the USRP platform using Simulink. USRP is the peripheral device that generates an electrical signal from the digital signal produced in MATLAB. For the implementation and proof-of-concept of RPO-OFDM, a linear LED driver for concurrent data transmission and dimming control is presented in this section. The schematic of this proposed LED driver and the PCB luminaire are depicted in Figure 6.10 and Figure 6.11, respectively. Most of the commercially available LEDs, which are considered as the load of driver, have a nonlinear I-V curve for all given input voltages; this makes it hard for the driver to achieve a linear response. The linear portion of the curve is defined from the turn-on voltage to the start of its saturation region where the ramp of the I-V curve is constant.

The electrical signal generated by the USRP will be the input of this LED driver. According to the Figure 6.10, this signal will be shaped by the network of R_1, R_2 and R_3 resistors and then will be amplified by the gain of $(1 + R4/R5)$. Voltage gain from input to the output of Opamp is given by 6.2.

$$\frac{(R_2 \parallel R_3)}{R_1 + R_2 \parallel R_3}(1 + \frac{R_4}{R_5}) \tag{6.2}$$

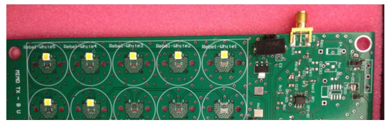


Figure 6.11: The PCB luminaire for dimming compatible OFDM

The DC voltage V_{dc} will be shaped by the network of R_1, R_2 and R_3 as well and after amplification its value will be superimposed by that of signal coming from USRP. The voltage gain for this DC voltage is given in 6.3.

$$\frac{(R_1 \parallel R_3)}{R_2 + R_1 \parallel R_3}(1 + \frac{R_4}{R_5}) \tag{6.3}$$

To keep operation in the linear region, the minimum level of signal at the output of Opamp should be higher than the threshold voltage of MOSFET M_1. Also for the 50Ω input matching, the values of this resistive network at the input of driver should be set as to have the equivalent input impedance of 50Ω. The input impedance is given by (6.4).

$$(R_1 + R_2 \parallel R_3) \tag{6.4}$$

By optimization of these three equations, the design parameters are derived. The resistor R_d is placed in series with LEDs as to limit the current through them. The resistor network as well as the gain stage can be considered a linear circuit as long as the frequency of interest lies under the 3dB bandwidth of the system. It is worth mentioning that the degenerated common source configuration composed of M_1 and R_s not only converts the voltage at the gate of M_1 into the current signal, but also helps to extend the linearity of the circuit. Placing R_s in series with the MOSFET changes the equivalent trans-conductance of the circuit from g_m to G_m where g_m is the trans-conductance of M_1 and G_m is defined as (6.5).

$$G_m = \frac{1}{R_s + 1/g_m} \tag{6.5}$$

Based on this equation, the equivalent trans-conductance is no longer chang-

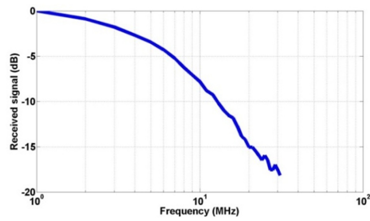


Figure 6.12: The frequency response of LED driver

ing directly by g_m, which is process, temperature and DC current dependent. The equivalent or effective trans-conductance in this case is controlled by the value of R_s especially for the large values of g_m, and it helps to increase the linearity. To increase the linear range of operation, the LEDs are biased properly by setting the DC voltage of V_{dc} shown in Figure 6.10. The frequency response of this driver is shown in 6.12. In obtaining this frequency response, a photodetector ($PDA10A$) is used. Based on this frequency response, the 3dB bandwidth of this circuit is 5MHz which is well beyond the bandwidth needed for transmission of the electrical signal that is sampled at 400kSps and used as the input to the PCB luminaire in this implementation. As depicted in Figure 6.10, seven series of Cree $XLampML-B$ LEDs are used which are operated under the DC supply (V_{dd}) of $25V$. The MOSFET used in this implementation, M_1, is $BSP110$, and the Opamp is $AD8009$. The intensity of light over the wide dimming range varies linearly which is explained more in detail in the next section.

6.2.4 Measurement Results

The SDR concept is a broadly adopted technique where the signal processing, *i.e.* the complete modulation and demodulation chains, is moved from the analog domain to the digital domain in order to provide implementation flexibility. The block diagram of the proof-of-concept testbed for dynamic adaptation of lighting conditions (to fulfil illumination requirements) is shown in Figure 6.13. MATLAB is used to build the RPO-OFDM system model, while Simulink is used to interface with the USRP from Ettus Research. We generate a random series of data and the corresponding digital RPO-OFDM samples in MATLAB. We use the USRP Hardware

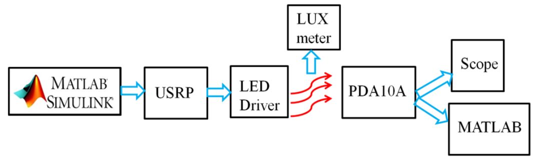


Figure 6.13: Block diagram of the testbed

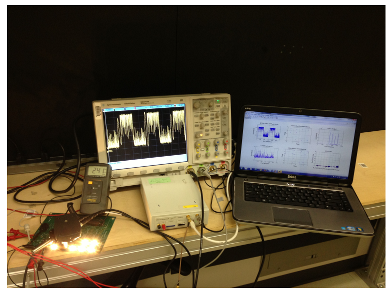


Figure 6.14: The measurement setup for dimming compatible OFDM

Driver (UHD) interface within Simulink (this requires the USRP support package for the communications system toolbox) to repeatedly transmit the digital signals to the USRP. In this implementation, and within the USRP, we utilize the low frequency transmitter (LFTX) daughter card to generate the baseband electrical signal at 400kSps that acts as the input to our PCB luminaire introduced in Section 6.2.3. The USRP is equipped with the LFRX daughter board also operating at 400kSps. In this setup, 8 ACO-OFDM symbols per PWM period, 64 subcarriers per symbol and 17dBm average electrical power per ACO-OFDM symbol are considered. A sinusoidal wave at the beginning of every PWM period is transmitted and used to realize a coarse Tx-Rx synchronization, *i.e.* the receiver searches for this sinusoidal wave (correlation process) to determine the start of a PWM period (see Figure 6.15).

At the receiver, we utilize the off-the-shelf transimpedance amplifying photodetector $PDA10A$ from Thorlabs with a concentrating lens (no blue filtering). The received electrical signal is input to the low frequency LFRX daughter card receiver of the USRP. The received digital signals are precessed in real-time using MATLAB/Simulink in order to calculate the BER performance. For measurements, the optical detector and a Lux meter are located directly on top of the PCB luminaire. A LodeStar Lux meter is used to evaluate the linear change brightness at

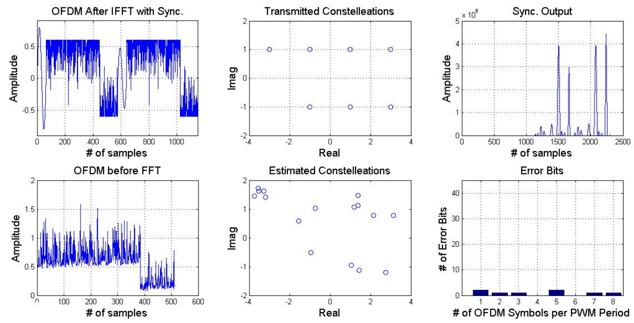


Figure 6.15: The MATLAB GUI showing the generated RPO-OFDM signal (using 8-QAM) (upper left), the ideal QAM constellations (upper middle), the peaks of the correlation process to realize frame synchronization (upper right), the received RPO-OFDM after extracting the RPO-OFDM from the PWM signal (lower left), the estimated constellations (lower middle) and the number of bits in error per OFDM symbol where 8 symbols are used within a PWM period (lower right)

different dimming levels. Figure 6.14 shows the measurement setup, where 8-QAM modulation with a 50% duty cycle is used and displayed on the oscilloscope window. A single USRP is used as a VLC transceiver.

We realized a real-time implementation, where the MATLAB-based graphical user interface (GUI) shows, for example, the number of bits in error per OFDM symbol and the estimated complex constellations (see Figure 6.15). Figure 6.16 shows the linear change of dimming for modulation schemes of BPSK, 4-QAM, 8-QAM and 16-QAM. Also for several modulation schemes BPSK, 4-QAM, 8-QAM and 16-QAM the measured BER curves as a function of the PWM duty cycle are shown on Figure 6.17. It is experimentally confirmed that at a fixed average of power of a RPO-OFDM symbol (17dBm), the obtained BER is maintained independent on the dimming level within the supported dimming range. Error free BER is obtained for BPSK and 4-QAM. The supported dimming range covers as low as 12.5%. It is also noticed that at around 50%, the QAM modulation order has no effect on the dimming level. The reported BER in the order of 10^{-3} is obtained without channel estimation and symbol equalization, *i.e.* no pilot symbols are transmitted to estimate the channel for frequency-domain equalization (raw estimated bits without symbol equalizations are used to calculate the BER). In addition, error free BER performance using BPSK and 4-QAM is obtained.

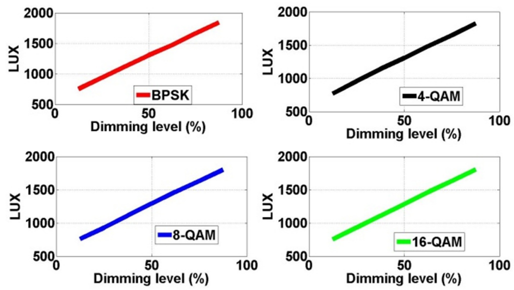


Figure 6.16: Linear change of dimming for different modulation schemes

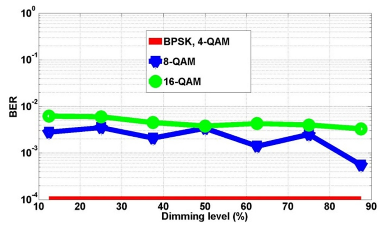


Figure 6.17: BER vs dimming level for different modulation schemes. Error free BER is obtained for BPSK and 4-QAM

6.3 Conclusion

In this chapter two distinct demonstrations were described. In the first one, software defined visible light communication; we have provided the SDR concept and its application for the visible light medium as well as a detailed description of the implementation of an SDVLC system. A fully functional SDVLC system provides the opportunity for rapid implementation and experimentation of optical communications. While much of the current research in SDR is leading the way to next generation radio systems, the idea of SDVLC expands the "Software Defined" concept beyond the RF domain and into the broader classification of Software Defined Communication. The second part was implementing a wireless access testbed through visible light and dimming compatible OFDM. The developed PCB luminaire is successfully used in a real-time testbed to demonstrate VLC transmission using RPO-OFDM to achieve dimming compatibility with the industry-standard PWM signal. Error free BER performance using un-coded BPSK and 4-QAM and without symbol equalization is obtained. Using the same setup parameters, a BER performance in the order of 10^{-3} is achieved for 8-QAM, and 16-QAM modulations over a wide-range of dimming levels. A linear control of the brightness is confirmed while maintaining the target data rate.

Chapter 7

Conclusion and Future Work

One of the key merits of optical wireless systems, which operate at baseband, is the relatively low transceiver complexity and low energy-per-bit required for data transmission compared to RF systems [91]. Furthermore, transceiver integration using CMOS which are inherently low-power, show promise in providing combined illumination/communication networks with ”net-zero” energy increase using LEDs. Such systems provide an opportunistic medium for indoor video streaming, communications, and wireless sensor networks for smart grid networks and industrial automation/control [92,93]. VLC offers the advantage of unlicensed part of the spectrum as well as security property and will play a key pioneering role in providing ubiquitous wireless connectivity using white LEDs. With LEDs being increasingly used in different illumination applications, the necessity for an efficient driver with an optimized control circuitry becomes more important. Since LEDs are current-driven devices in which light is produced via the recombination of injected holes and electrons in a semiconductor junction, the luminous intensity of LEDs is typically controlled by controlling the forward current flowing through the device. The biggest challenge toward achieving this vision is the limitation over rise and fall times of white LEDs. To address this issue, developing optimum transmitter architectures together with using circuit design techniques are known to be the best approaches. In this manner, different techniques are used in LED drivers to improve the performance and efficiency of LEDs. The two well-known trends which are commonly used to increase the achievable bandwidth are blue filtering and equalization. The emergence of non-traditional illumination applications for LEDs introduces new challenges in the development of driver circuits. For visible light communication, driver circuit compatibility with standard PWM dimming control methods is preferred [38]. Consequently, it is a necessity to make the Off-the-shelf LED drivers compatible with the data transmission capabilities in order for them to be used in various VLC based applications. The conventional LED driver design incorporates circuitry to provide a constant supply voltage and current regulation of LED devices. The design tradeoff between feedback loop bandwidth, switching losses, and ripple rejection put limitations on data modulation rates of VLC transmitters using commercial LED driver architectures. The driver circuit architecture presented in this work overcomes the modulation bandwidth limitation by providing a feedback control loop to maintain the DC-DC converter output voltage independently of the LED drive signal to control data modulation and dimming. The driver should provide the dimming capability as well. The combination of data transmission with the dimming control is implemented in the digital and also analog domains and the details for both approaches are described in this work. In addition to dimming capabilities, LED driver to be used for the VLC systems has to support the data transmission as well. The level of illumination which is required for reading and writing ensures that the channel bandwidth is higher than the sources; thus the channel by itself does not limit the performance of the system. The limiting factor, however, is the low bandwidth of LEDs. This limitation is two sided; one is related to the optical and the other is related to the electrical domain. Rise and fall time are the two most significant factors contributing to LED bandwidth limitations in the electrical domain, which in turn establish the maximum data rate achievable by the device. This electrical bandwidth limitation is emanated from the large value of parasitic capacitance of LED. The larger the parasitic capacitance, the longer time needed for its charging and discharging and the higher the value of rise and fall time. Optical domain is the other side of LEDs bandwidth limitation. Total optical bandwidth is inversely proportional to the carrier lifetime or carrier recombination.

This modulation bandwidth of an LED device can be increased by increasing the carrier concentration in the active region, with a simultaneous decrease of the carrier lifetime. This, however, has a negative effect on the LED overall optical output power. Therefore, a compromise between modulation bandwidth and power output must be reached during the design process. Analog or digital circuit design, then, can be used to shorten the rise or fall time and extend the overall bandwidth. Perhaps the simplest way of alleviating the low bandwidth problem of the transmitter which is due to the long decay time of the phosphor is to block its component at the receiver by using a blue filter; this can increase the bandwidth substantially with the cost of a small reduction in received power due to the filter losses. Applying bandwidth-efficient modulation schemes that take advantage of the high available SNR is another approach; complex modulations such as OFDM/DMT are proved to have dominant role in enhancing bandwidth. There are different methods of increasing data rates, and a combination of these can be applied to get a better and more reliable performance. In this work the conventional methods of extending the bandwidth of LED drivers are reviewed and proposed topologies are introduced. Seven distinct methodologies of negative impedance converter (NIC), equalization techniques, pulse shaping, peaking, pole-zero cancellation, time-interleaved LEDs, and 16-level PAM are presented. The concept of NIC is reviewed and two different modes of fixed and floating structures with their corresponding proposed LED drivers are introduced. The NIC is promising structure which generates negative capacitances and by putting its output in parallel with the LED, the parasitic capacitance of LED will be degraded in full or in part, either of them helps in extending the bandwidth. Pre and post equalization techniques such as multiple resonant, and active and passive equalizations are methods which compensate the roll-off in the transfer function of raw-LED, leading to bandwidth extension. The other method is pulse shaping; the carrier sweep out technique for decreasing the rise and fall times is explained and a pulse shaping circuit is presented which enhances the overall bandwidth of the VLC link by shortening the rise and fall times. The next method for bandwidth enhancement is peaking; different peaking techniques such as shunt, series, (bridged) shunt-series and triple resonant peaking techniques are reviewed and a new technique called bridged-shunt-zero peaking is proposed. A peaking technique called bridged-shunt-zero peaking is presented in this work which is suitable for implanting in the LED driver circuits. Pole-zero cancellation is another method that has been used for bandwidth enhancements. The pole-zero cancellation in general generate zero in the transfer function and extend the bandwidth by canceling the associate pole. A proposed LED driver with enhanced bandwidth using the pole-zero cancellation methodology is presented. Time-interleaved LEDs is yet another trend in compensating the low bandwidth of LEDs. In this method each binary input is sent with a fixed delay and with processing the received signal a data rate of 100Mbps is achievable with low 10MHz LEDs. Finally, seventh method is 16-level PAM using 4×4 array of LEDs to increase the data rate by 4 times.

If we want to just state one feature for the future LED drivers, the answer would be efficiency. The trend toward making LED drivers is determined by its efficiency. Hence, the total power consumption of the driver should be minimized. The LED driver to be used for the VLC applications should provide dimming as well as high rate of data transmission. Its architecture also depends on the type of modulation scheme it is going to take. For the base-band modulation techniques such as OOK, implementing the dimming control is straight forward. However, this is not the case for the analog and complex modulation schemes. Even though the RPO-OFDM is one solution for this problem, more research should be done in this area. The other negative point of using the complex modulation schemes is being bulky and expensive. Accordingly, the design trend is toward integration and a the target is a product which is low cost and low power.

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