Gigascale Silicon Photonic Transmitters Integrating HBT-based Carrier-injection Electroabsorption Modulator Structures

A dissertation submitted by

Enjin Fu

In partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

TUFTS UNVERSITY

August, 2015

Advisor: Prof. Valencia Joyner Koomson

For my family

Abstract

Demand for more bandwidth is rapidly increasing, which is driven by data intensive applications such as high-definition (HD) video streaming, cloud storage, and terascale computing applications. Next-generation high-performance computing systems require power efficient chip-to-chip and intra-chip interconnect yielding densities on the order of 1Tbps/cm^2. The performance requirements of such system are the driving force behind the development of silicon integrated optical interconnect, providing a cost-effective solution for fully integrated optical interconnect systems on a single substrate. Compared to conventional electrical interconnect, optical interconnects have several advantages, including frequency independent insertion loss resulting in ultra wide bandwidth and link latency reduction.

For high-speed optical transmitter modules, the optical modulator is a key component of the optical I/O channel. This thesis presents a silicon integrated optical transmitter module design based on a novel silicon HBT-based carrier injection electroabsorption modulator (EAM), which has the merits of wide optical bandwidth, high speed, low power, low drive voltage, small footprint, and high modulation efficiency. The structure, mechanism, and fabrication of the modulator structure will be discussed which is followed by the electrical modeling of the post-processed modulator device. The design and realization of a 10Gbps monolithic optical transmitter module integrating the driver circuit architecture and the HBT-based EAM device in a 130nm BiCMOS process is discussed. For high power efficiency, a 6Gbps ultra-low power driver IC implemented in a 130nm BiCMOS process is presented. The driver IC incorporates an integrated 2^7-1 pseudo-random bit sequence (PRBS) generator for reliable high-speed testing, and a driver circuit featuring digitally-tuned pre-

emphasis signal strength. With outstanding drive capability, the driver module can be applied to a wide range of carrier injection modulators and light-emitting diodes (LED) with drive voltage requirements below 1.5V. Measurement results show an optical link based on a 70MHz red LED work well at 300Mbps by using the pre-emphasis driver module. A traveling wave electrode (TWE) modulator structure is presented, including a novel design methodology to address process limitations imposed by a commercial silicon fabrication technology. Results from 3D full wave EM simulation demonstrate the application of the design methodology to achieve specifications, including phase velocity matching, insertion loss, and impedance matching. Results show the HBT-based TWE-EAM system has the bandwidth higher than 60GHz.

Acknowledgement

First and foremost, I am deeply indebted to my advisor Prof. Valencia Joyner Koomson for her continuous encouragement, mentorship and support. I cannot overstate how influential Prof. Koomson has been for my personal and professional developments. Her inspiration was essential to the completion of this dissertation.

I would like to thank my thesis committee members: Prof. Mohammed N. Afsar, Prof. Mark Cronin-Golomb from Tufts biomedical department, and Prof. Ronald W. Knepper from ECE department at Boston University for their time and dedication. Thanks for their insightful suggestions on this work.

I would like to thank Prof. Z. Rena Huang and my colleagues Pengfei Wu and Shengling Deng at RPI for their continuous help and inspiration of the collaborative optical modulator project. I would like to thank Prof. Afsar and my colleagues Liu Chao, Tinghao Liang, Hassan Oukacha, Jun Jadormio, Kate Auerbach, Wei Wang at Tufts for their great cooperation of the CMOS integrated microwave circulator project. It's so exciting to work on both cutting-edge projects with them.

I would like to thank Prof. Sameer Sonkusale for teaching me analog and mixed signal circuits design and letting me have access to the test instruments in Nanolab. Thanks Prof. Knepper at Boston University for teaching me radio frequency circuits design. He was always willing to answer all my questions. Meanwhile, I would like to thank Prof. Joseph Noonan, his "Communication systems" course is the most funny and also informative one I ever taken. Also, I

would like to thank Prof. Tom Vandevalde for his insightful suggestions to this research project.

Special thanks to Cheng Li at Hewlett-Packard Laboratory for his useful discussion about this research project. His papers inspired me a lot of good ideas. I would like to thank Saroj Rout and Pramod Singh for their precious help and discussion about the circuits design. They are always nice and helpful.

Also, I would like to thank my Qorvo colleagues: Mike Coolen for his help about RF PCB design, and Ginny Bouthillette for her help about chip-on-board wirebonding.

I would like to thank my lab fellows Ali Mirvakili, Chirag Sthalekar, Ruida Yun. It's very lucky to work with them in the same lab, I would never forget about it. I would like to thank all the other lab colleagues: Pooria Mostafalu, Ninrat Datiri, Chenguang Xi, Shideh Kabiri, Saber Bahranifard, Zhengxin Zhao, Kyoungchul Park, Sam MacNaughton, Guoqing Fu, Meera Punjiya, Robbie D'Angelo, Krener Konomi, Yun Miao, Yu Chen, Chiamaka Chima, Nana Kwakwa, Stephen Akaeze, Barbara Gyasi, Jian Guo, Wangren Xu, and my friends at ECE department: Hao Zhang, Chen Gao, Jincheng Pang, Ruiling Gao, Yuping Dong, Anjali Sharma, Yuanwei Wu. Forgive me if I miss any names here. It's really nice to meet them in my life.

I would like to thank all the administrative staffs at Halligan: Miriam Santi, Jennifer St Pierre, Ilse Allen, Renee Simonetti, Merrianne Terranova for their great assistance. I want to state my appreciation and gratitude to George Preble, Eric Patton, Patrick Hynes, Mike Bauer, Jon Fredrick for their support in handling any technical matters. The international center advisors are amongst the best and they were always happy to provide help. I would like to thank Jane Etish-Andrews, Lois Hutchings, Naoko Kotoge, Carol Murphy and Whitney Sullivan. They are one of the important reasons why I love Tufts so much.

The most important, I would like to thank my family for their great support. Without their encouragement and understanding, I could not finish this dissertation.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Data communication

Nowadays the demand for more bandwidth is rapidly increasing driven by data intensive applications such as HD video streaming, cloud storage, etc. Varieties of internet accessible terminals such as smartphones, pads, PCs, and smart home appliances multifold the demand for data. According to the estimation by CISCO systems, in 2016 the data traffic is expected to be one zeta (10^{21}) bytes, which is nearly doubled compared to 2013 as shown in Figure 1.1[1].

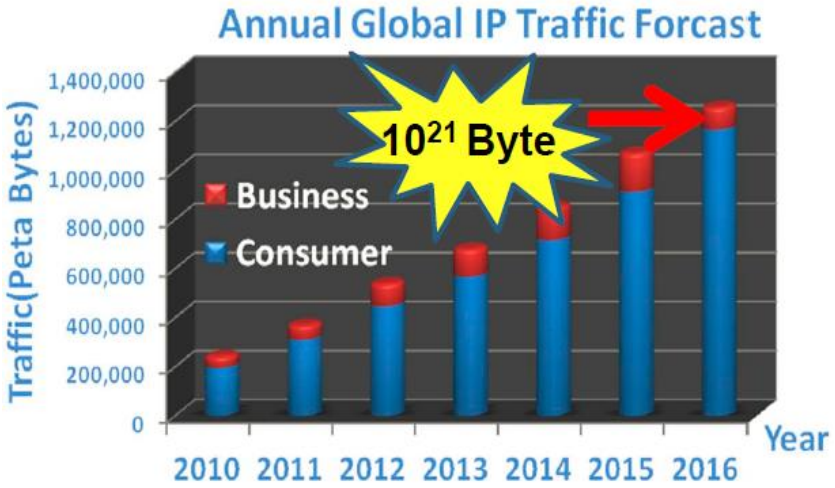


Figure 0.1: Global IP traffic forecast [1]

To keep up the pace with the data demand, scientists are keep inventing data communication methods with higher bandwidth. With unbeatable bandwidth optical interconnect is the dominant method for long distance, ultra-high speed

data communication.

1.2 Optical interconnect VS electrical interconnect

Optical fiber interconnect (or optical interconnect/link) and electrical interconnect (or electrical wire interconnect) are mainstream mediums for data communication. Base on the mediums, optical communication system and electrical communication system can be built with extra components and circuits as shown in Figure 1.2 and 1.3. In the figures the *L* denotes the link length. Moreover, optical interconnect requires laser (or LED) and photodiode to realize electrical-optical and optical-electrical conversion.

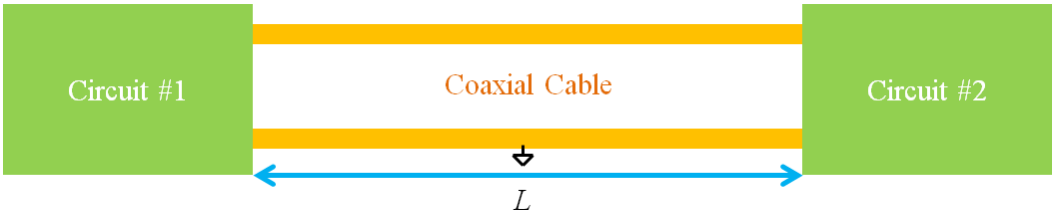


Figure 0.2: Electrical interconnect system

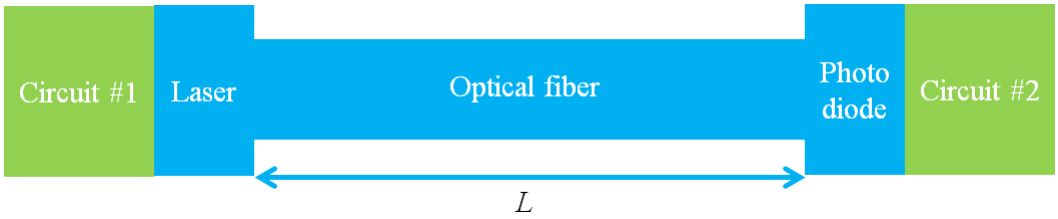


Figure 0.3: Optical interconnect system

Electrical interconnect mitigates the demand for extra optical component so it's favorable for short distance lower speed communication. However, due to the fact that the dielectric loss is proportional to frequency and length, electrical interconnect is not a good solution for long distance and high speed communication. Here the optical interconnect and electrical interconnect will be compared from three perspectives.

A. Insertion loss

The most common board-to-board electrical interconnect is coaxial cable. The insertion loss of coaxial cable has the state-of-art specification of -7.5dB/m@70GHz[2]. On the other hand, the material loss of multi-mode optical fiber is around 0.0035dB/m[3], which means the loss from material is negligible if link length is shorter than 100m. By accounting for the coupling loss, the total loss is summarized in Table 1.1 and plotted in Figure 1.4.

Table 0.1: Loss comparison of board-to-board interconnect

	Coaxial cable [2]	Optical Fiber [3] (multimode@850nm)
Material loss (dB/m)	-7.5@70GHz -5.3@40GHz -2.5@10GHz	0.0035
Coupling loss (dB)	-0.2	-3
Total loss	-0.2-7.5**L*@70GHz -0.2-5.3**L*@40GHz -0.2-2.5**L*@10GHz	-3-0.0035**L*

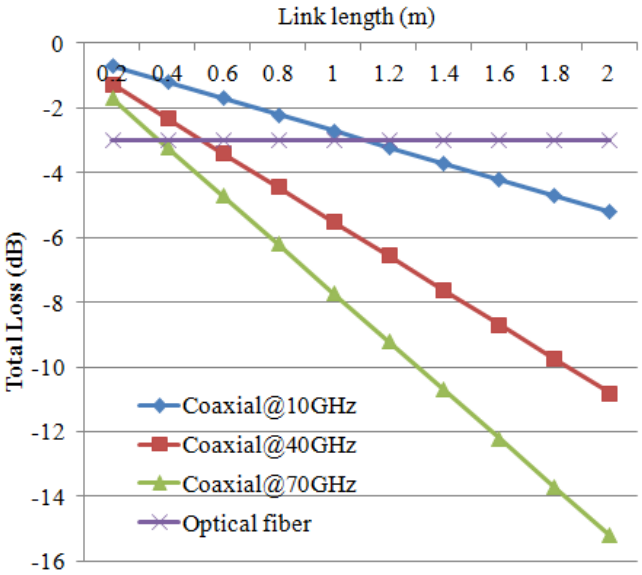


Figure 0.4: Loss comparison of board-to-board interconnect

It can be summarized that, at frequency of 10GHz, the link loss of optical fiber is less than coaxial cable when link length is longer than 1.1m; at frequency of 40GHz, the critical length is about 0.4m; while at frequency of 70GHz, the critical length is as short as 0.3m. Next generation optical fiber communication is at the speed of 50Gbps or even higher. At this data rate the electrical signal is only viable up to 10cm [4] which limits its application in the long distance communication. On the other hand, the state of art VCSEL-based optical fiber communication has been realized with data rate higher than 40Gbps [5][6][7][8].

Figure 1.5 shows supercomputer “Sequoia”[9], which has 1.5million cores and was ranked number one in the world in 2012. As it shows the communication between modules are realized by optical fiber, but not coaxial cable or other electrical wire.

Figure 0.5: Supercomputer “Sequoia” invented by IBM [9]

On the other hand, chip to chip to intra-chip interconnect can be realized by electrical-magnetic waveguide such as coplanar waveguide (CPW) for electrical signal or silicon waveguide for optical signal. The insertion loss of on-chip CPW has the state-of-art specification of -2dB/mm@70GHz [10]. On the

other hand, a state-of-art silicon optical waveguide which has the link loss of -0.17dB/mm was proposed in [11]. By accounting the coupling loss, the total loss is summarized in Table 1.2 and plotted in Figure 1.6.

Table 0.2: Loss comparison of on-chip interconnect

	CPW [10]	Silicon waveguide[11]
Material loss (dB/mm)	-2@70GHz -1.1@40GHz -0.4@10GHz	-0.17
Coupling loss (dB)	Negligible	-1
Total loss	-2**L*@70GHz -1.1**L*@40GHz -0.4**L*@10GHz	-1-0.17**L*

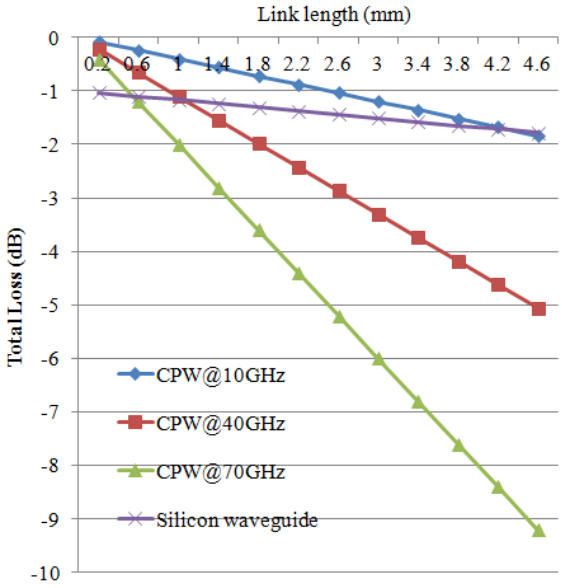


Figure 0.6: Loss comparison of on-chip interconnect

It can be summarized that, at frequency of 10GHz, the critical length when link loss of optical fiber is less than coaxial cable is 4.4mm; at frequency of 40GHz, the critical length is about 0.8mm; while at frequency of 70GHz, the

critical length is as short as 0.4mm. Thus, optical interconnect is favored over electrical interconnect in the application of board-to-board and intra-chip communication when the data rate is the main concern. Equalizer can be used at the receiver to retrieve the link loss for the electrical interconnect. However, it adds power consumption overhead to the system [12].

B. Propagation delay

Minimizing the signal propagation delay is a primary requirement for interconnect in very large scale integration (VLSI) architectures [13]. For ultra-high speed interconnect the propagation delay is a critical factor for the synchronization especially when the system has many clock driven building blocks. Ideally the propagation delay should be as minimum as possible otherwise extra circuits are required for compensation which adds complexity, power budget and cost. Table 1.3 shows the unit length delay of coaxial cable and optical fiber (n=1.43). Table 1.4 shows the unit length delay of on-chip CPW and silicon optical waveguide. The optical phase velocity is defined as the phase velocity in vacuum divided by the refractive index n in the optical medium, as described by equation (1.1)

$$v = \frac{c}{n} \tag{1.1}$$

Table 0.3: Delay comparison of board-to-board interconnect

	Coaxial cable [2]	Optical Fiber [3] (multimode, n=1.49)
Delay (ns/m)	4.43	4.97

Table 0.4: Delay comparison of on-chip interconnect

	CPW[13]	Silicon waveguide [13] (n=3.4)
Delay (ns/m)	20	10

As the tables show, the phase delay of an optical interconnect is similar or better than an electrical interconnect. Considering the extra delay on E-O and O-E conversion components, the total delay of an optical interconnect is expected to be only one third of which of electrical interconnect in 2016 [14].

C. Power efficiency

To evaluate the power efficiency of an interconnect, a FOM is proposed as described in equation (1.2).

$$FOM = \frac{Total\ power\ of\ the\ link}{Data\ rate} \tag{1.2}$$

By using a hybrid optical I/O structure, the power efficiency is expected to reach up to 1pJ/b at data rate of 50Gbps when using a 16nm CMOS process for fabrication. On the other hand, by using monolithic optical I/O, the power efficiency is expected to be as low as 0.35pJ/b at 50Gbps data rate when using a 16nm CMOS process [12]. As discussed in [15], optical interconnect has pre-dominant power-efficiency over electrical interconnect when interconnect length is longer than 15mm.

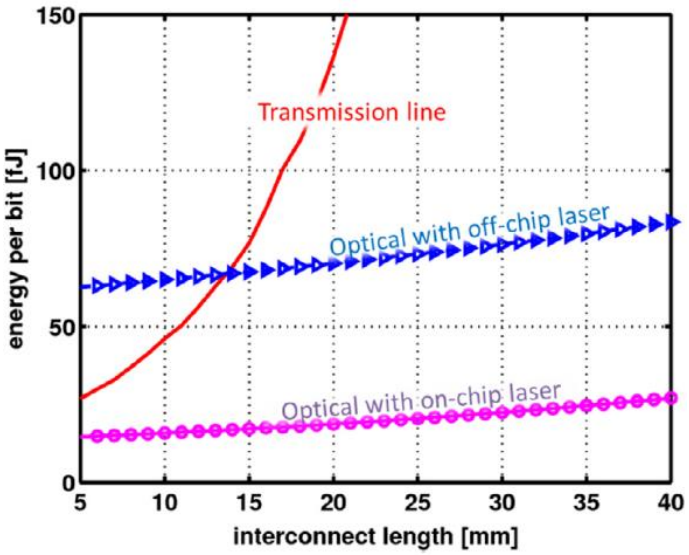


Figure 0.7: Comparison of the energy/bit of the low-latency interconnect options in a 22 nm logic node [15]

1.3 Silicon photonics

Next-generation high-performance computing systems require chip-to-chip or intra-chip interconnect working at higher speed with lower loss, lower latency and higher power efficiency. The demand drives the feasibility of integration of optical communication system in the chip level. The integration can be realized by hybrid integration or monolithic integration. Hybrid integration means the optical components and electrical components are separately designed and fabricated before integrated electrically, as depicted in Figure 1.8. It has the merit that each component can be custom tailored but has the deficiency of higher cost on multi-process fabrication and chip packaging.

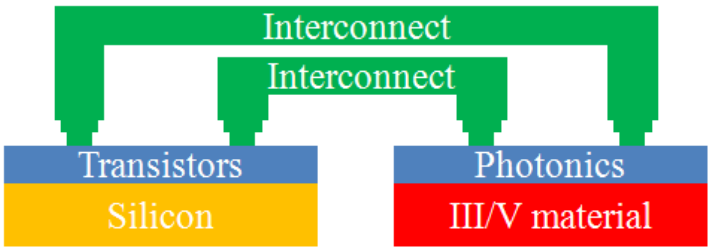


Figure 0.8: Hybrid integration of an OE system

On the other hand, monolithic integration means the optical components and electrical circuits are fabricated on the same substrate as depicted in Figure 1.9. It mitigates the integration overhead, but requires traditional VLSI process compatible with optical component. The second integration method has been popularly studied recently and called photonics integrated circuits (PIC) or silicon photonics.

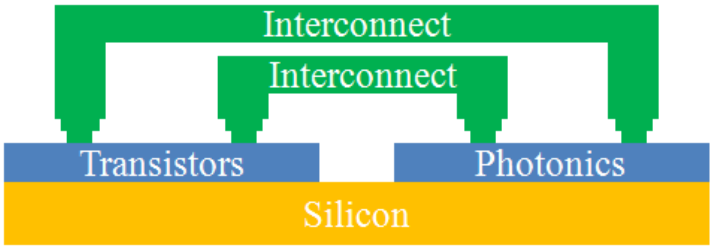


Figure 0.9: Monolithic integration of a OE system (silicon photonics)

The main goal of silicon photonics is to realize optical components by using commercial silicon CMOS process. With twenty years of developing and commercialization silicon process has become the first option for large scale electronics integration with the merit of low cost, high robustness, high level integration and fast yield cycle. It becomes a main solution for most electronics realms from consumer products, such as cellular phone, WiFi, automotive radar to military products such as phase array radar. In recent years, the silicon processes are popularly studied about the possibility to be used to fabricate photonics components such as light source, waveguide, modulator, and photodetector as shown in Figure 1.10. By taking advantage of VLSI and optical communication, an unprecedented ultra-high bandwidth and high efficient interconnect can be realized within silicon chips [16][17][18]. Moreover, silicon is an attractive optical material because its transparency to infrared communication wavelengths and its high refractive index which facilitates the miniaturization of photonic devices [19]. The state of art silicon photonics optical transceiver system has the power efficiency as low as 500fJ/b [20] which utilized a commercial 40nm CMOS process for circuits fabrication and 130nm CMOS SOI platform for photonics component fabrication. The world class data rate performance of an intra-chip optical link has reached up to 25Gbps/channel [21] with power efficiency of 10.2pJ/b. By using wavelength division multiplexing technology, the multi-channel data rate can reach up to 80Gbps (4*20Gbps)[22].

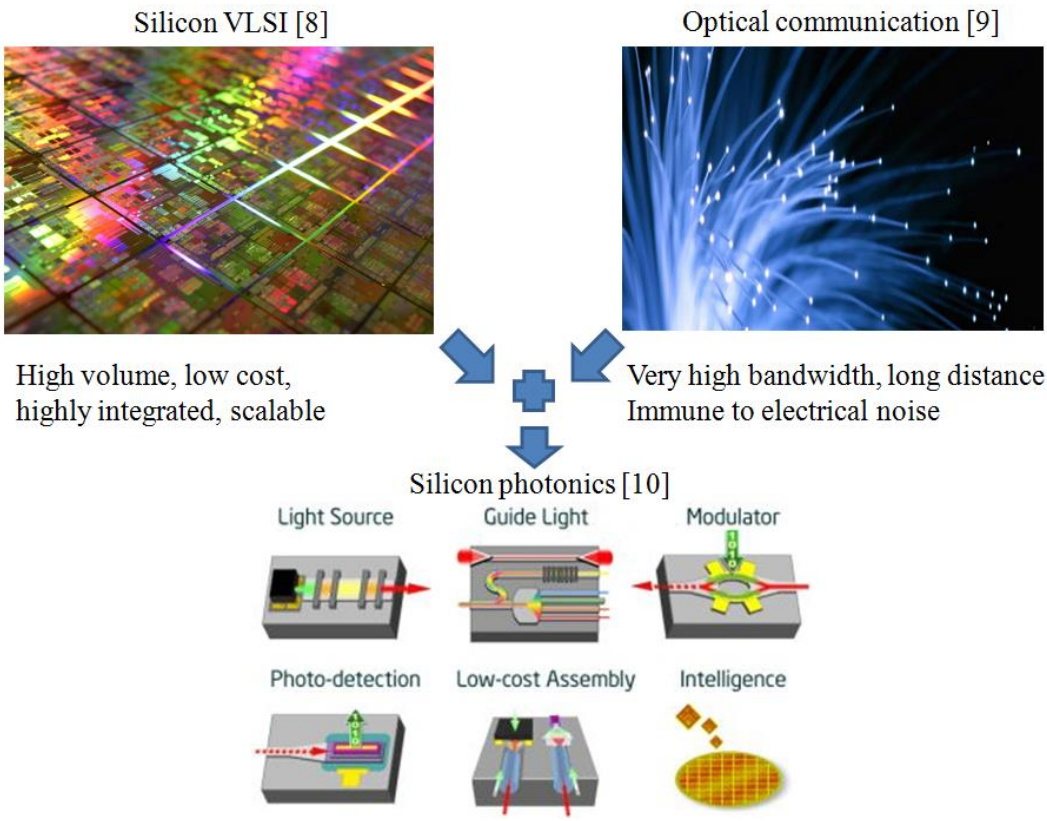


Figure 0.10: Silicon photonics [16][17][18]

Figure 1.11 shows the cross-section view of a typical N-type MOSFET transistor in a commercial CMOS SOI process. The transistor is built on top of insulator layer and isolated by surrounding shallow trench. Figure 1.12 shows the cross-section view of an optical modulator based on P-N diode. Compared to the NMOS transistor which has N+ type doping at two terminals, the P-N diode has one N+ doped terminal and one P+ doped terminal. Same as NMOS transistor, the P-N diode has its intrinsic region covered by SiO_2 (could be other type of dielectric material such as Si_3N_4), which helps to confine the light signal in the center of the waveguide as the oval region denotes. As the figure shows from the process complexity point of view the processing modification from CMOS transistors to photonic components is cost effective. Previously deep-ultraviolet photolithography and dry-etching is popularly used for micro-fabrication of the photonics components [23]. Due to comparably high roughness which is critical to the optical signal loss, this technology is gradually replaced by E-beam

lithography[24].

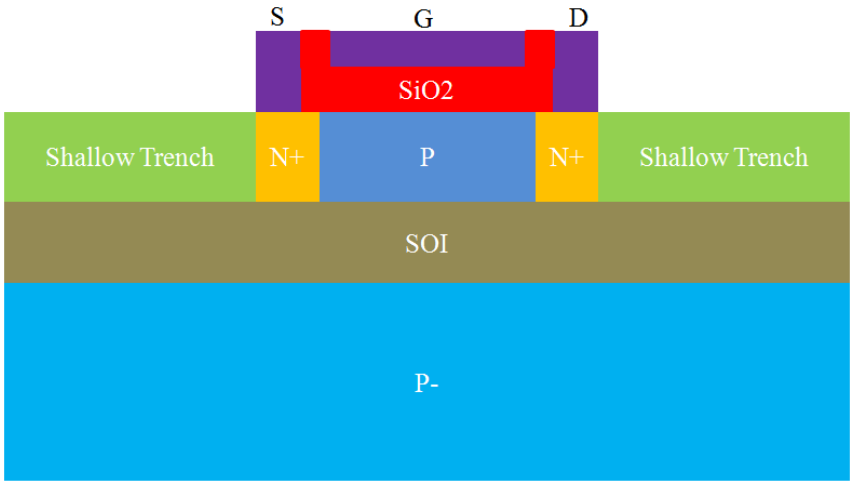


Figure 0.11: NMOS FET in SOI process

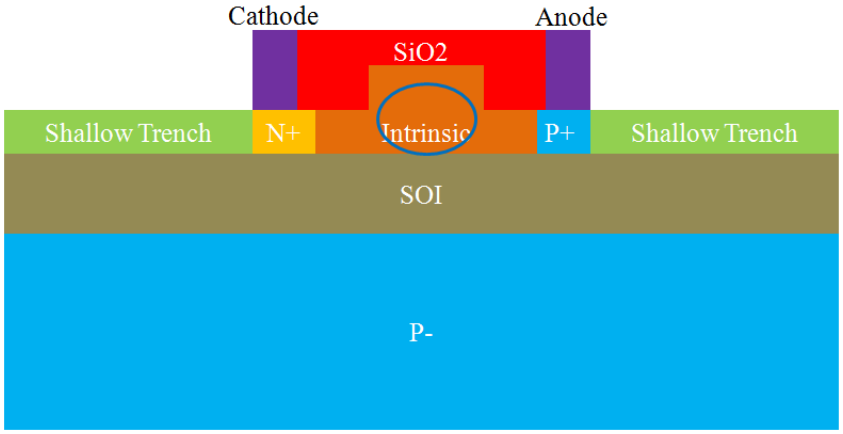


Figure 0.12: Optical waveguide/modulator on a SOI wafer

There are some challenges to integrate the two traditionally hybrid systems onto the same substrate from the perspective of performance. For optical components, they are required to be functional at the wavelength of 1.3μm or 1.5μm because silicon material is "transparent" to optical signals only at those wavelengths. Secondly, the electrical-optical (EO) components need to be functional within the electrical capability of the silicon process. For example, an optical modulator which needs to be driven at 3V is not compatible with the silicon process which has the maximum rating voltage (V_{dd}) of 1V.

On the other hand, the silicon processes also need to be adapted to optical components. Besides the physical layer modification described previously in Figure 1.11 and 1.12, the modification also includes the accurate modeling of optical components. Some foundries already possess the accurate modeling of some common photonics components such as imec-ePIXfab[25] while some commercial software have the co-simulation capability of electrical components and optical components such as VPIphotonics^{TM} [26].

It's happy to see quite a few optical components have been successfully fabricated on silicon wafer in recent years, from the optical source, such as laser diode [27][28][29]; optical modulator [30]; and to photodiode [31][32]. Most existing monolithic silicon photonics systems is based on micro-ring modulator such as [33] which has merit of CMOS compatibility and ultra-low power. However, its narrow optical bandwidth and high sensitivity to temperature and process variation makes it not a robust solution. Paper [34] proposes tuning circuitry to solve this problem but it adds extra power and cost to the system. This thesis is going to present a silicon HBT modulator based optical transmitter. Besides the merit of wide optical bandwidth, the modulator has the feature of high speed, low power, low driving voltage, small footprint, high modulation efficiency which makes it a good candidate for the modulator in optical interconnect. Because the modulator is based on HBT-device in a commercial process, it can be easily monolithic integrated with VLSI circuits. In the next section, the adopted commercial process will be introduced as the background information.

1.4 Silicon photonics on SiGe BiCMOS substrate

Bipolar-CMOS (BiCMOS) process is famous for the availability of high performance bipolar transistors. They are commonly used for high speed high power circuits such as power amplifier, driver circuitry, etc. Germanium (Ge) material is introduced into silicon bipolar transistors because it has a larger lattice constant and smaller energy bandgap than silicon (0.66eV vs 1.12eV), making it a

suitable candidate for bandgap engineering in silicon. By introducing Ge into Si the carrier mobilities are improved with respect to pure silicon because of the reduction in carrier scattering [35] and the grading of the bandgap. The improvement of mobility will lead to high transition frequency (f_T).

The first SiGe heterojunction bipoloar transistor (HBT) was demonstrated in 1987, and became famous in June of 1990 with the demonstration of a non-self-aligned SiGe HBT grown by ultra-high vacuum/chemical vapor deposition (UHV/CVD), with a peak f_T of 75GHz [35][36][37]. Nowadays the f_T of advanced HBT devices can reach up to 500GHz [38]. Commercialized processes such as IBM SiGe 7HP with 200nm emitter width has peak f_T of 120GHz; 8HP with 120nm emitter width has peak f_T of 210GHz; and 9HP with 90nm emitter width has peak f_T of 300GHz [39].

On the other hand, SiGe bipolar transistors can be easily integrated into silicon CMOS process to make a SiGe BiCMOS process. The cross-section view of SiGe HBT transistor is depicted in Figure 1.13. The germanium material is applied in gradient in the base area.

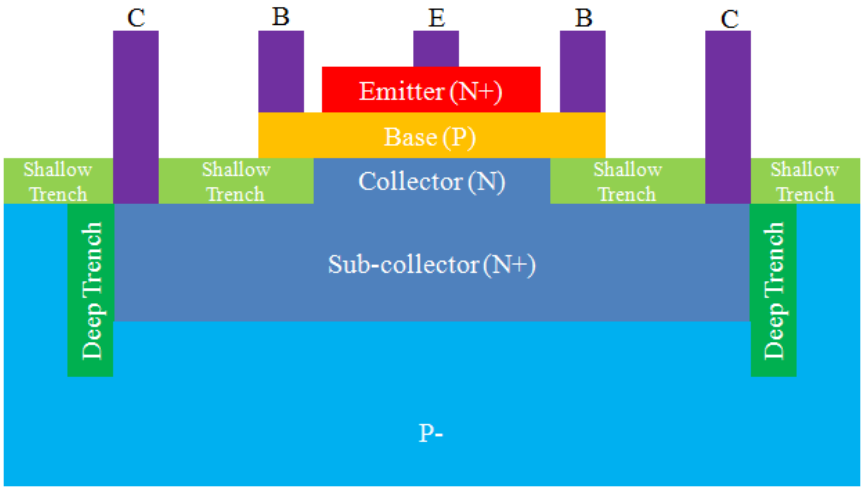


Figure 0.13: SiGe HBT device cross-section view

Figure 1.14 shows the SiGe MOSFET can be easily integrated with SiGe HBT on the same substrate. A typical state-of-art SiGe HBT BiCMOS process generally have a roughly 20% adder in mask count compared to pure digital

CMOS process, which means its cost-efficient.

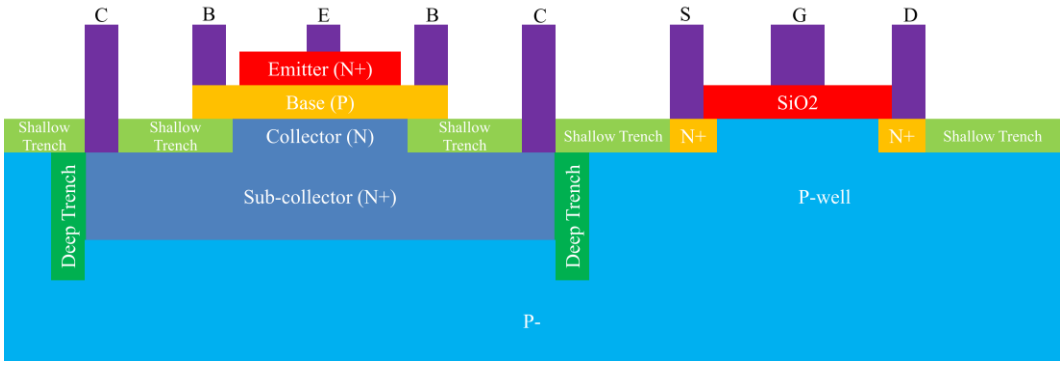


Figure 0.14: SiGe HBT and silicon NMOS on a same substrate

As Figure 1.13-14 shows, the existing high performance BiCMOS processes all sit on bulk silicon instead of SOI substrate for the reason of good heat dissipation because high speed HBT transistors are usually power hungry [40]. However, this stack layer configuration is not compatible with optical components. A solution for the compatibility of high performance BiCMOS process to the photonics components, which adopts a method called "local SOI" was proposed in paper [41]. Figure 1.15 depicted the method that for the HBT transistor which are used as photonics components, a SOI layer is inserted under it. The blue oval denotes the center of the light. For those HBT transistors used only for circuitry, the device structure is kept the same as Figure 1.13 shows.

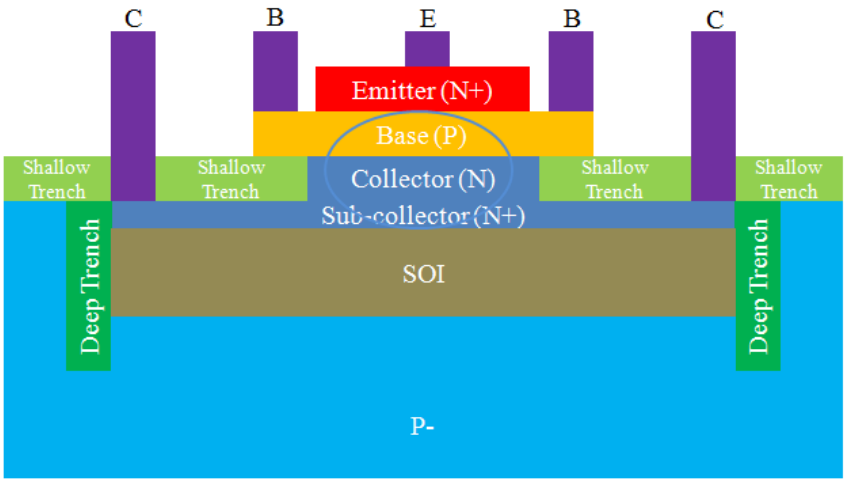


Figure 0.15: Adapted photonics friendly SiGe BiCMOS process

1.5 Thesis organization

This thesis is going to present a gigascale silicon photonics transmitter design integrating silicon HBT-based carrier injection electroabsorption modulator structures. The thesis is organized in the following manner. Chapter 2 will introduce the optical communication system with the focus on optical modulator. The principle, mechanism and varieties of modulator will be discussed. After that a SiGe HBT-based carrier injection electroabsorption modulator (EAM) is going to be presented from the physical design, post-processing steps to the electrical modeling and simulation results. In chapter 3 a 10Gbps driver design will be presented while the post-processing challenges and limitations will be discussed. In chapter 4 an ultra low power 6Gbps transmitter design will be discussed from the system level to every building blocks and to transistor level design. RF PCB design will be presented while measurement results from the packaged dies and chip-on-board solution will be compared. Measurement based on probe station which generates the best results will be discussed in detail. In chapter 5 a red LED-based optical communication link, which is based on the transmitter discussed in chapter 6 will be presented. It will be proved that the pre-emphasis can be used for LED bandwidth enhancement. In chapter 6 a traveling wave electrode design will be discussed and a new methodology will be proposed. Chapter 7 will discuss the future work of this project and the conclusion.

Chapter 2

SiGe HBT-based Carrier Injection Electroabsorption Modulator

In an optical communication system, modulator is a component used to realize electrical-to-optical signal conversion. It's a key component which significantly determines the performance of the whole system. This chapter is going to present different varieties of modulator with the focus on free-carrier dispersion effect. We are going to present a novel HBT-based carrier injection electroabsorption modulator design. Before discussing the modulator, the optical communication systems basics will be introduced, with some major specifications reviewed.

2.1 Optical communication systems

2.1.1 Application

The unbeatable data rate and ultra-low loss compared to its electrical counterpart makes optical interconnect as "backbone" of global optical communications. Figure 2.1 shows an overview of optical communication systems which include main system, metro system, local area network (LAN), storage area network (SAN) and fiber to the home (FTTH) system[42]. Let's take FTTH as an example, home use internet is used to be connected by Asymmetric Digital Subscriber Line (ADSL) for many years. Because the interconnect is based on twisted wire, the physical data speed limit is about 8Mbps. With the demand for high quality experience at home such as HDTV, ADSL based internet is not a good option anymore while faster communication method is required. Thus, this field is starting to be occupied by FTTH systems. Nowadays, the

internet providers can supply personal high speed internet options such as 25Mbps, 50Mbps, 105Mbps, etc. Speed with 500Mbps is also available on the market if you would like to pay 300 dollars per month to experience the speed.

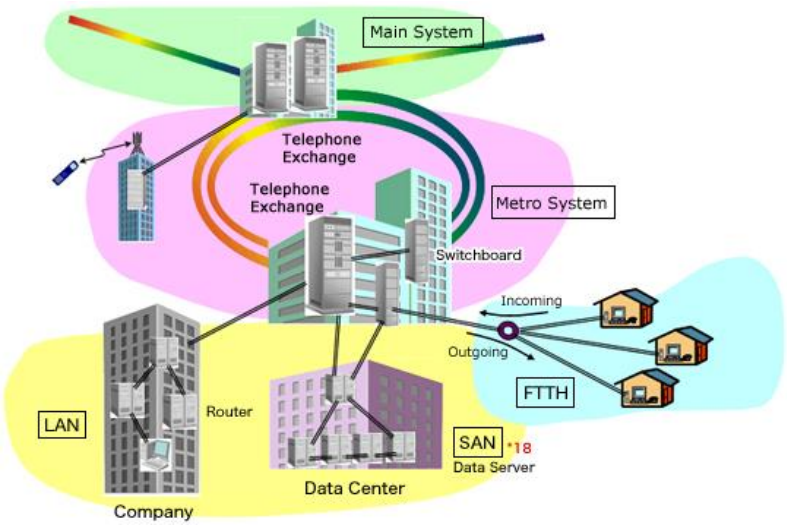


Figure 0.1: Applications of optical communication [42]

With the upgrading of the micro-fabrication and exploration of new materials, the speed of single-wavelength optical channel can reach up to 25Gbps [21]. By using wave-division-multiplexing(WDM)[43] a single optical channel can reach a speed of 50Gbps. A typical optical communication system can be described by Figure 2.2, which includes optical source, optical modulator, optical waveguide, optical detector and electrical building blocks such as modulator driver, transimpedance amplifier (TIA), limiting amplifier, equalizer, etc.

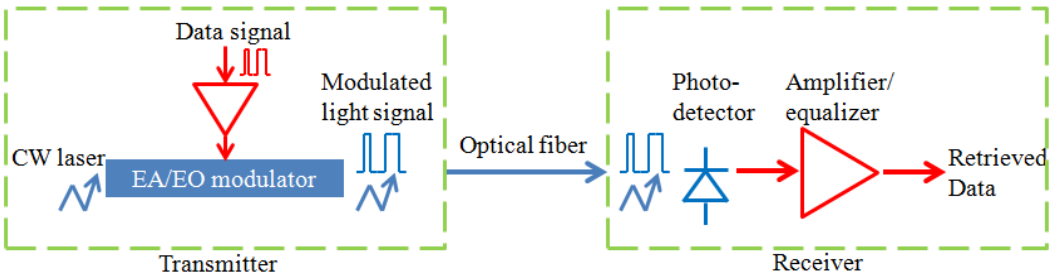


Figure 0.2: Optical communication system

2.1.2 Key specifications

In this section some key specifications of an optical communication system are going to be reviewed. They will be the background information for the discussion of optical modulator.

A. Data format

Usually, the high speed data signal is modulated on the light either by direct intensity modulation as in an electroabsorption modulator (EAM) or in-direct intensity modulation as in an electro-optic modulator (EOM) represented by Mach-Zehnder interferometer (MZI). For intensity modulation the most common data format is Non-Return-Zero (NRZ) which is described by Figure 2.3. In this format the two amplitude levels representing logics zeros and ones. High level represents logic one and low level represents logic zero while the duty cycle of each bit is 100%. Return-Zero (RZ) is another format described in Figure 2.3 which has less than 50% duty cycle for logic ones and 100% duty cycle for logic zeros.

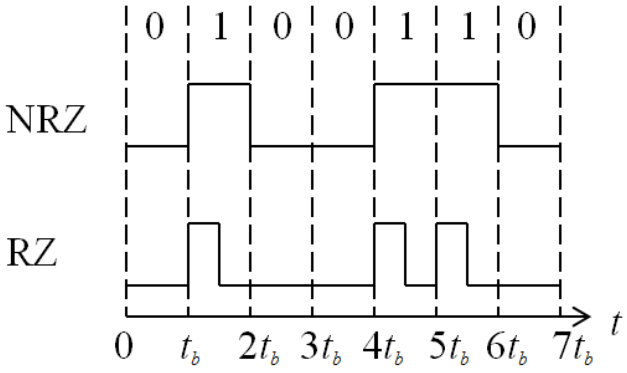


Figure 0.3: Format of NRZ and RZ signal

Figure 2.4 and 2.5 show the spectrum of NRZ and RZ signal respectively. In comparison, RZ signal contains clock information which provides convenience for clock recovery. However its doubled bandwidth compared to NRZ signal provides complexity to the circuit design.

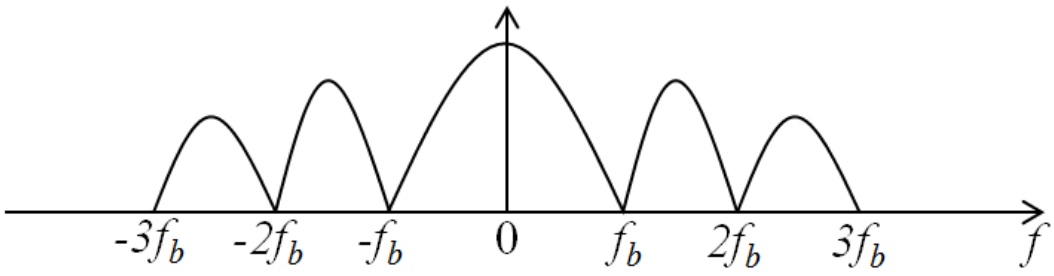


Figure 0.4: Spectrum of NRZ signal

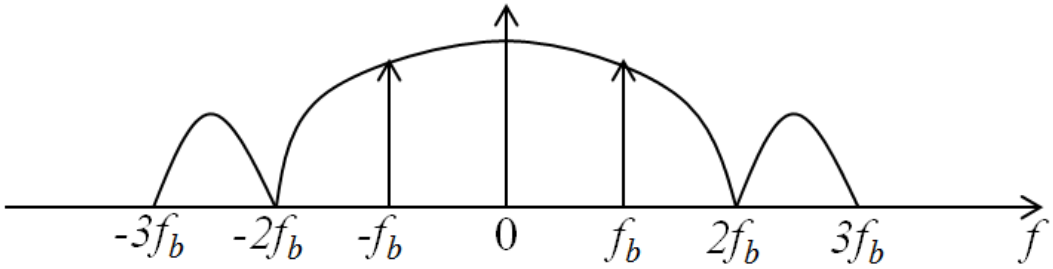


Figure 0.5: Spectrum of RZ signal

Pseudo-random bit sequence (PRBS) signal is a special data pattern used to characterize the performance of a data communication link. Because the data pattern is "random" zeros or ones which is close to the real data stream, the performance of an optical transceiver can be evaluated sufficiently by using it as a test signal. "Pseudo-random" means the sequence is not really random. Actually, it is still repetitive data pattern but only with random data sequence in each period.

The most common PRBS generators have the data length of 2^3-1, 2^7-1, 2^{15}-1 and 2^{31}-1, etc. The longer data length means the data pattern is more complex which provides more stringent requirement for the hardware performance. A 2^3-1 PRBS generator is shown in Figure 2.6. It consists of three DFFs triggered by the same clock signal, and one XOR gate. One of the DFFs needs to have the function to be set to logic one in order to initialize the PRBS generator while avoiding the all zero state.

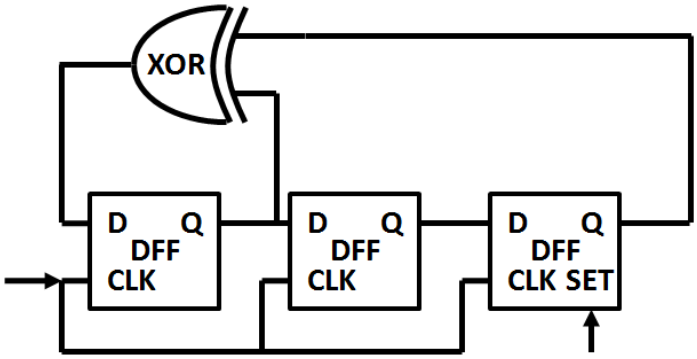


Figure 0.6: 2^3-1 PRBS generator

The generated bit pattern is depicted in Figure 2.7. It can be seen that the data pattern is repeated every 2^3-1 bits. By using different number of DFFs the length of data pattern is different. The number of the DFFs determines the longest consecutive ones in the data pattern. For example, as Figure 2.7 shows the longest consecutive ones in a 2^3-1 PRBS signal is three. The long consecutive ones/zeros is not favorable because the energy will be concentrated at DC or very low frequency which requires very wide bandwidth circuits. Otherwise, the voltage level of long consecutive ones/zeros will droop significantly.

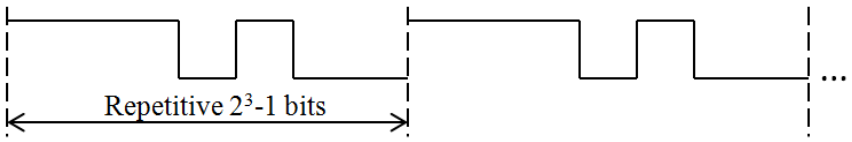


Figure 0.7: 2^3-1 PRBS signal

Because PRBS signal is still periodic, its spectrum is a bunch of tones with the spacing of 1/(bit length*bit duration). The envelope of the tones is the same as NRZ signal as shown in Figure 2.4. Figure 2.8 depicts the spectrum of the 2^3-1 PRBS signal with the tone spacing of 1/(7*bit duration). The spectrum beyond f_b is not shown here for simplicity but it has the same tone spacing and the envelope as Figure 2.4 with zeros at integers of f_b.

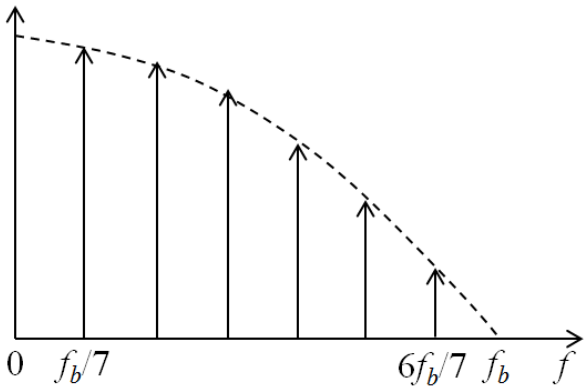


Figure 0.8: spectrum of PRBS signal

B. Eye diagram

For a data signal the most important specifications are: the amplitude of logic ones and zeros; the rise/fall time at logic transitions; and the timing of each bit. All those information can be achieved by overlapping each bit on top of each other and display them in a small time window, which is called "eye diagram". There are a lot of information can be retrieved from eye diagram, such as the bandwidth, noise, etc. Figure 2.9 describes an example of how an eye diagram is formed by separate bits. Here t_b denotes the time duration of each bit. Figure 2.9(a) shows three bits at time from 0 to $3t_b$ with a logic zero to one transition at t_b. Figure 2.9(b) shows three bits at time from x to $x+3t_b$ with a logic zero to one transition at $x+2t_b$. Figure 2.9(c) shows three bits at time y to $y+3t_b$ with a logic one to zero transition at $y+t_b$. Figure 2.9(d) shows three bits at time z to $z+3t_b$ with a logic one to zero transition at $z+2t_b$. Figure 2.9(e) shows the overlapping of the twelve bits into the window of Figure 2.9(a), which forms the eye diagram.

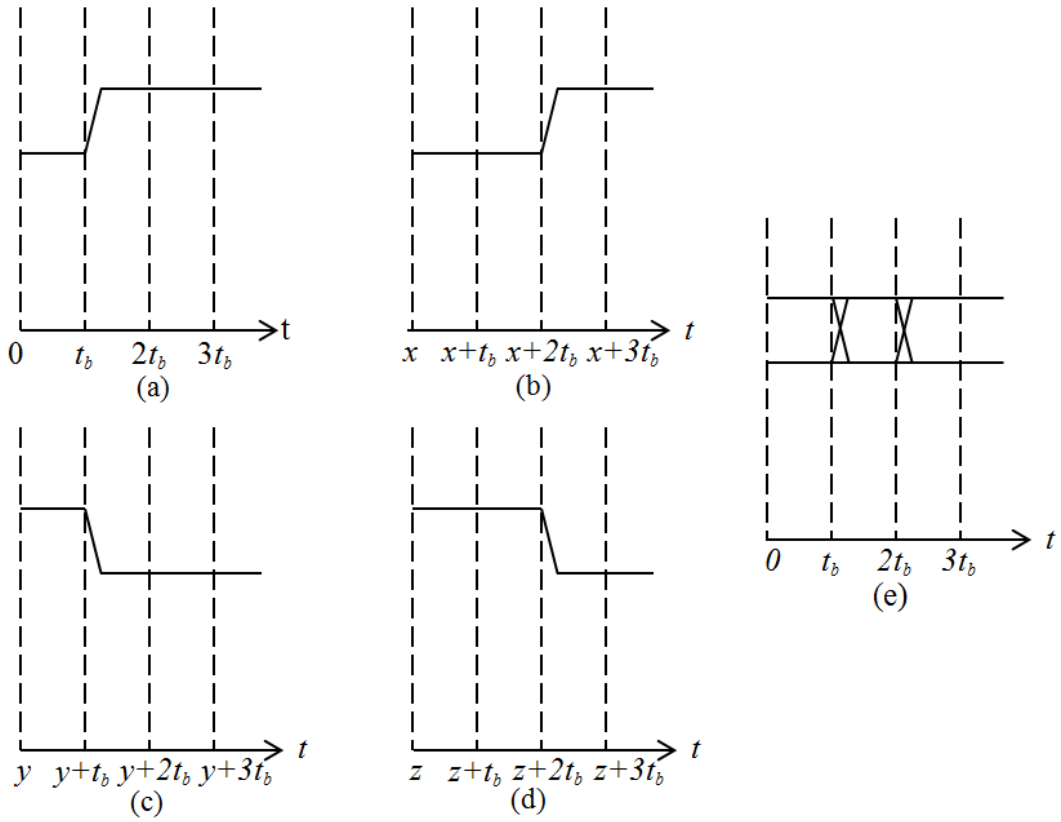


Figure 0.9: how an eye diagram formed

While Figure 2.9(e) shows the ideal eye diagram, Figure 2.10 shows an example of realistic eye diagram. Figure 2.10(a) depicts the problem that every logic transition is not overlapping each other perfectly but with some variations. The accumulation of the variations is called peak-to-peak jitter (J_{pp}), which is usually due to the noise of circuits, or the circuits are data pattern dependent.

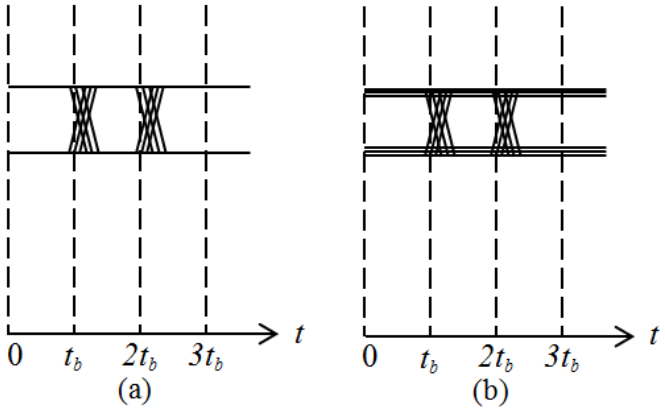


Figure 0.10: (a) Jitter and (b) noise

Figure 2.10(b) depicts the non-ideality of amplitude, which makes a smaller eye opening than the ideal eye diagram. This problem is mainly due to the circuit noise or the DC droop caused by circuit limited bandwidth, and it may cause the decision circuits to make errors.

There are several different jitter definitions. Peak-to-peak jitter J_{pp} and root-mean-square (rms) jitter J_{rms} are two commonly used jitter specifications. Jitter can be decomposed into different categories. Figure 2.11 shows jitter is composed of random jitter and deterministic jitter, while the deterministic jitter can be further decomposed to period jitter, data dependent jitter, etc. Nowadays advanced sampling oscilloscopes have the capability to do these jitter analysis.

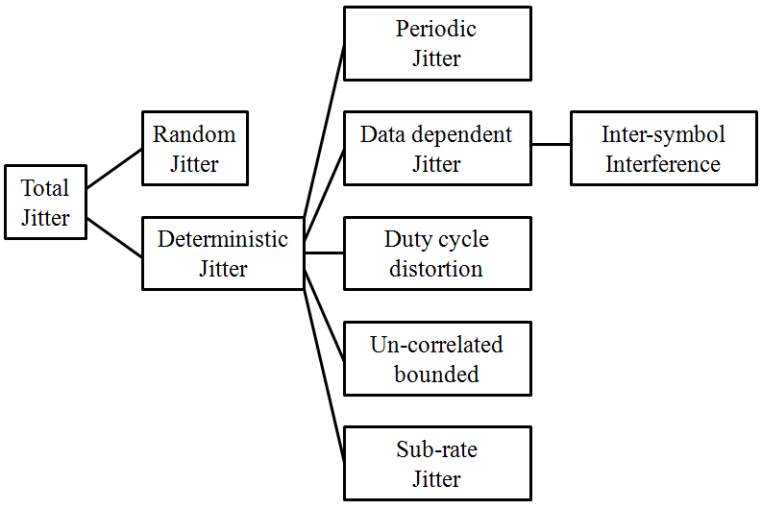


Figure 0.11: Jitter components

C. Bit error rate

Both noise and inaccurate timing could generate logic error. Figure 2.12(a) shows the ideal timing which is at the center of each bit while the bit is clean without noise. Figure 2.12(b) shows a realistic eye which carries a lot of noise while the timing could vary from t_1 to t_2. The decision circuit will generate a logic error if the sampling is at t_1 or t_0 but error free if it is at t_2.

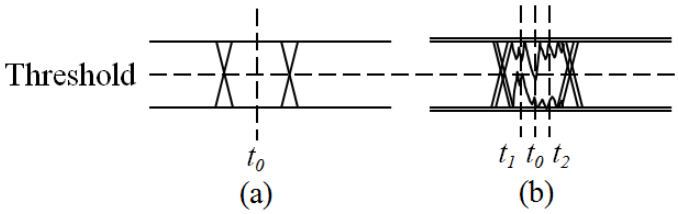


Figure 0.12: Logic error

Bit error rate (BER) is the specification used to describe how many logic errors happen in an amount of bits. Usually the claimed data rate of an optical system is described based on a specific BER, such as 10^{-12}, which means the system has only one bit error after sending one trillion bits at the claimed data rate. The BER is directly related to the signal to noise ratio (SNR), which can be statistically described by equation (2.1, 2.2) [44][45].

$$SNR = \frac{eye\ level\ one - eye\ level\ zero}{rms\ noise\ level\ one + rms\ noise\ level\ zero} \tag{2.1}$$

$$BER \approx \frac{1}{SNR * \sqrt{2\pi}} e^{\frac{-SNR^2}{2}} \tag{2.2}$$

D. Bit rate

Bit rate is a major specification of every data communication method because it is a specification that end consumer can really feel directly and care most. Bit rate is determined by almost every building block in the system. On one hand, the component which has lowest bandwidth in the system determines the maximum bit rate of the system. On the other hand, the noise contribution of every building block and the loss of the link medium decrease the SNR and the bit rate at a specific BER.

The state of art bit rate performance of single wavelength can reach up to 25Gbps per channel. The bit rate can be multi-folded by using Wavelength Division Multiplexing (WDM) which is described in Figure 2.13. By using comb laser, the data rate in a single optical waveguide can be increased by four times.

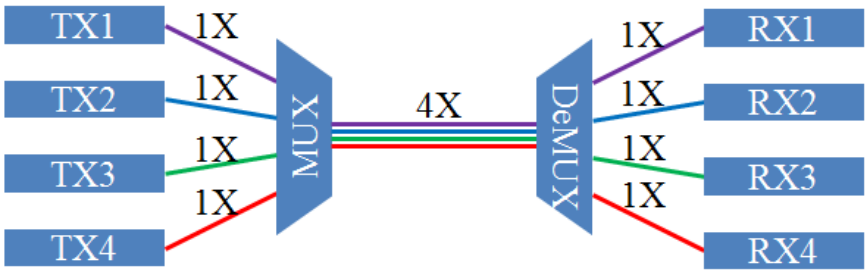


Figure 0.13: WDM transceiver system

E. Link power budget

Power efficiency is an important specification for battery powered systems. Although most optical communication system is not battery powered, there are some exceptions. For example, some optical interconnects which are used to replace the traditional electrical interconnects have stringent power budget because they need to defeat the electrical interconnects from every perspective. The power efficiency of an optical interconnect is evaluated by the required energy to send a single bit depicted by the unit of pico-joule-per-bit (pJ/b).

With stringent budget, every component in the optical link needs to be upgraded or improved. The state of art low power optical link has the power efficiency around 1pJ/b[12].

F. Cost

Although cost is not the most important specification in front of many other obstacles, it will be definitely an important one when silicon photonics technology becomes more mature and commercialized. There are some agencies which can provide standard silicon photonics components fabrication and fast production cycle, such as OPSIS; It can be predicted that, similar to silicon VLSI circuits technology, the cost of silicon photonics will keep reducing in the near future while it becomes more and more mature and commercialized.

2.2 Optical modulator

In an optical transmitter, modulator is a component used to realize

electrical-to-optical signal conversion. It's a key component which performance significantly determines the performance of the whole optical link. Usually, optical modulator is driven by electrical signal. The modulation of an optical signal can be realized by internal modulation, i.e. switching on and off the LED/laser directly by using a data modulated current source as depicted in Figure 2.14; or by external modulation, i.e. using fast switched optical modulator to modulate a continuous wave light source, as depicted in Figure 2.15. Usually internal modulation is not as efficient as external modulation. Most multi-Gbps optical modulator adopts the external modulation method. This section will focus on the external modulator and its ramifications.

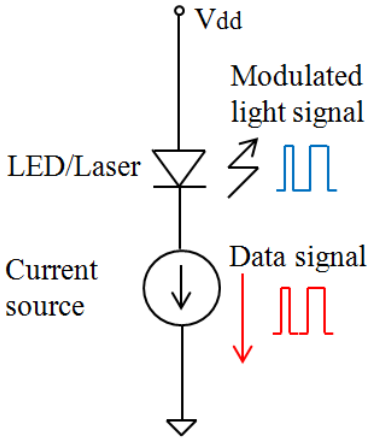


Figure 0.14: Internal modulation

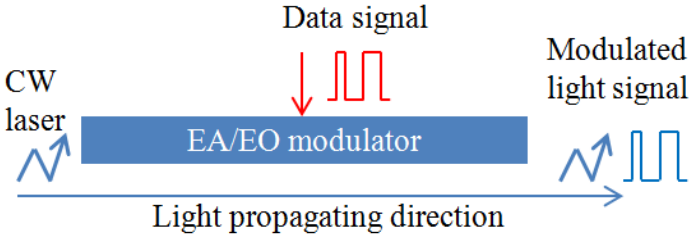


Figure 0.15: External modulation

2.2.1 Free carrier plasma effect

External optical modulator can be sorted into several categories by its modulation mechanism. The first category Electro-optic (EO) modulator relies on

the refractive index change brought by the external electrical field change as described in equation (2.3). The linear term of the Taylor expansion is defined as Pockels effect and the second order term is defined as Kerr effect. Traditional $L_iN_bO_3$ based optical modulator adopts the Pockels effect, thus they have very linear $n(E)$ relationship.

$$n' = n + a_1E + a_2E^2 + \cdots \tag{2.3}$$

Unfortunately, silicon has very weak Pockels or Kerr effect. Most silicon EO modulators utilize the free carrier plasma effect to manipulate the refractive index. The free carrier plasma effect is the second modulator mechanism category which refers to the change of refractive index manipulated by the change of electron and hole densities. As illustrated by Drude [46], the change of real part of refractive index, Δn, and change of imaginary part of refractive index, $\Delta\alpha$, are determined by the electron and hole density change, ΔN_e and ΔN_h. Soref derived an empirical equation for free carrier plasma effect in silicon, as described in equation (2.4)[47]

$$\begin{cases} \Delta n = \Delta n_e + \Delta n_h = -[8.8 \times 10^{-22}\Delta N_e + 8.5 \times 10^{-18}\Delta N_h^{0.8}] \\ \Delta\alpha = \Delta\alpha_e + \Delta\alpha_h = 8.5 \times 10^{-28}\Delta N_e + 6 \times 10^{-18}\Delta N_h \end{cases} \tag{2.4}$$

In the meanwhile, silicon is an attractive optical material from two perspectives. Firstly, it is transparent to infrared communication wavelengths. And secondly its high refractive index facilitates the miniaturization of photonic devices [48].

2.2.2 Silicon modulator varieties

By taking advantage of free carrier dispersion effect in silicon, there are three main categories of modulators. The first category is represented by Mach-Zehnder Interferometer (MZI) which uses phase change to realize amplitude modulation. The mechanism is described by Figure 2.16. The continuous wave

light enters into a MZI and splits into two branches. Branch #2 is free of modulation signal with the light phase at the output of MZI shifted by x degree. Branch #1 is modulated by a high frequency data signal which changes the light phase by $x+\pi$ degree with an extra of π degree compared to branch #1. At the output of the MZI, the light signals of the two branches are either constructively added which generates logic one, or destructively added which generates logic zero. For MZI, $V_\pi L_\pi$ is a FOM describing the modulation efficiency. Here L_π denotes the length of modulator which achieves the extra phase shift of π while V_π denotes the required AC voltage swing.

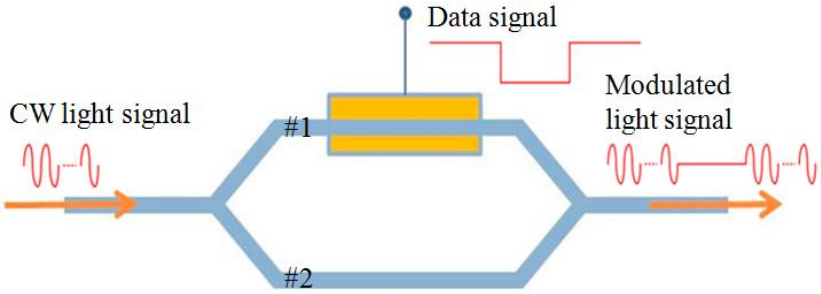


Figure 0.16: Mach-Zehnder Interferometer

The second category is called electroabsorption modulator (EAM). Different from MZI, it takes advantage of the light intensity change but not the phase change to realize the modulation. As depicted in Figure 2.17 the EAM has only one optical channel. The electrical data signal modulates the absorption coefficient of the waveguide, which will translate to the light strength change at the output of modulator waveguide. The difference of the light strength represents logic ones and zeros. In essence, EAM is working as an electrical controlled optical switch.

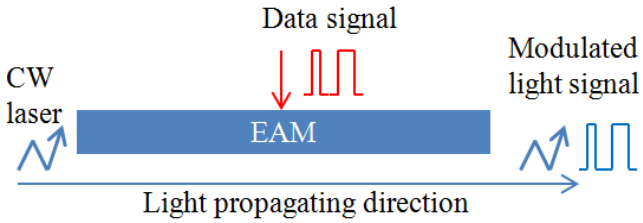


Figure 0.17: EA modulator

The third category of silicon modulator adopts resonant structure such as micro-ring modulator as showed in Figure 2.18[8]. The light is absorbed into the resonant cavity when the ring is not-biased, or path through the waveguide when the ring is forward-biased. The light intensity change at the output of the waveguide represents the logic zeros and ones.

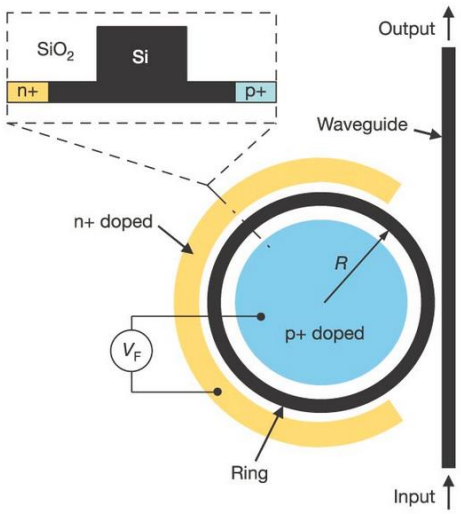


Figure 0.18: Micro-ring modulator [49]

Waveguide based modulators such as EAM or Mach–Zehnder modulators have the benefit of wideband operation, and hence greatly reduced the temperature sensitivity. Resonant structures greatly enhance the relatively weak free-carrier effect, thereby enabling ultra-low power consumption [50]. Moreover, it has the merits of CMOS process compatibility and low driving voltage. However, it has the deficiency of very narrow optical bandwidth which is highly sensitive to temperature and process variation.

2.2.3 Carrier injection VS Carrier depletion

The free carrier dispersion effect can be mainly utilized by two different methods. Modulator that change the carrier density based on majority carrier

movement through the depletion region is classified as depletion type as shown in Figure 2.19(a)[19]; while the modulator that change the carrier density by minority carrier injection through a p-n junction is classified as injection type as shown in Figure 2.19(b).

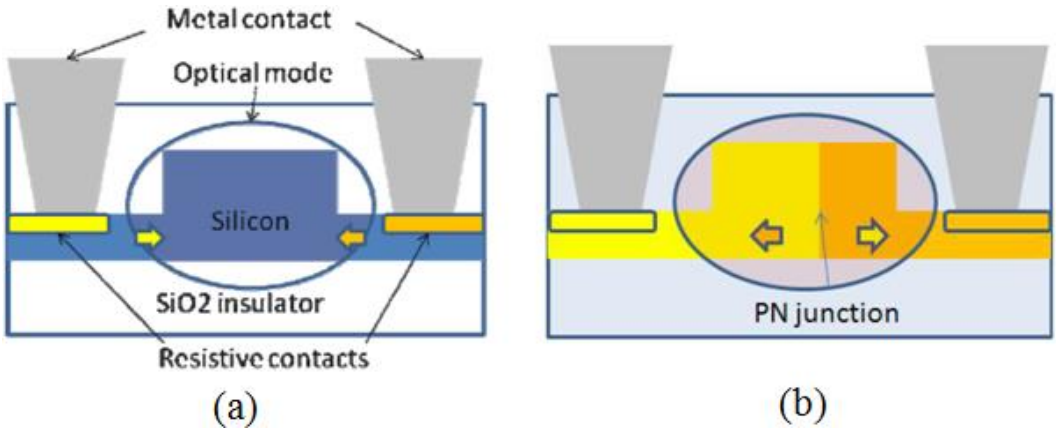


Figure 0.19: Modulator types (a) injection (b) depletion [19]

Both depletion and injection modulators have their merits and deficiencies. Firstly, from the speed perspective the depletion modulators are intrinsically faster than injection modulators because their moving carrier is majority carrier. Secondly, from the perspective of CMOS process compatibility the injection modulators are favorable because the required driving voltage can be 1V or even lower; while the required driving voltage for depletion modulators is usually 3V or higher, which hinders their integration with advanced commercial silicon processes. Thirdly, depletion modulators have better linearity which provides design convenience for high speed drivers. Fourthly, injection modulators intrinsically have much higher free carrier density change, which means the required footprint is much smaller. The low driving voltage and small footprint both lead to better modulation efficiency for injection modulators. Table 2.1 summaries the specifications comparison of depletion or injection modulators.

Table 0.1: Depletion and Injection type modulator comparison

	Carrier depletion	Carrier injection
Bias type	Reverse	Forward
Bias voltage	High	Low
Linearity	Very good	Weak
Footprint	Large	Compact
Modulation efficiency	Low	High
CMOS compatibility	Weak	Good

2.2.4 Ideal modulator

There are five major features a modulator should possess: fast response; low power; wide optical bandwidth; small footprint; and thermal tolerance. Unfortunately these features compromise to each other. For example, depletion modulators usually have fast response because the moving carrier is majority; however, the majority carrier density is low which leads to large device footprint requirement. Figure 2.20 defines the features of an "ideal modulator", which are the design targets for an optical modulator.

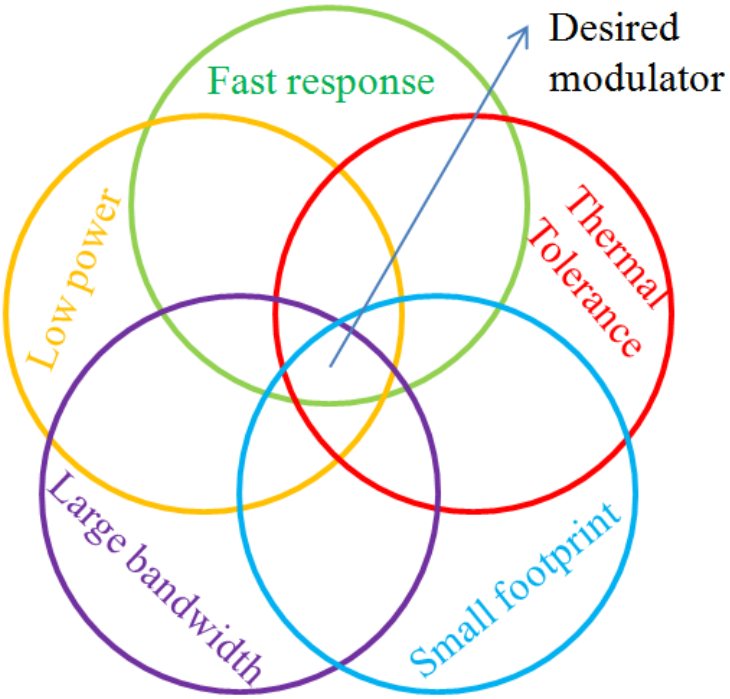


Figure 0.20: Desired modulator features

2.3 SiGe HBT-based Carrier Injection Electroabsorption Modulator

HBT device is a breakthrough innovation for ultra-high speed circuits and systems for its unbeatable gain at high frequency compared to MOSFET. Nowadays the HBT device in commercial BiCMOS process has the transition frequency f_T as high as 200-300GHz. Traditionally, people use pn, p-i-n diodes to realize a optical modulator. In 2009, a group at RPI firstly presented a high speed modulator design based on a HBT device[51]. Based on the device, some researchers have proposed modification and huge improvement which leads to a simulated speed of 80Gbps or more [52][53][54]. This section is going to introduce a newly developed HBT-based modulator design working in the carrier injection mode, which has the merits of high speed, low power, small footprint and wide optical bandwidth.

2.3.1 Device structure

Standard HBT device in a commercial BiCMOS process is depicted in

Figure 2.21. It has two base and two collector contacts and one emitter contact. The symmetrical structure is for better speed and reliability performance. It has deep trench isolating every single HBT device for less coupling, and shallow trench at non-active region for better isolation among the three terminals in a single HBT device. The key of high f_T is the small emitter width which is 120nm, and the small base thickness which is 40nm for this process. Different from SOI process, BiCMOS process is not designed sitting on a insulator layer due to heat dissipation problem because HBT devices are usually power hungry[35]. This feature requires an extra post-processing step to make it a good optical waveguide.

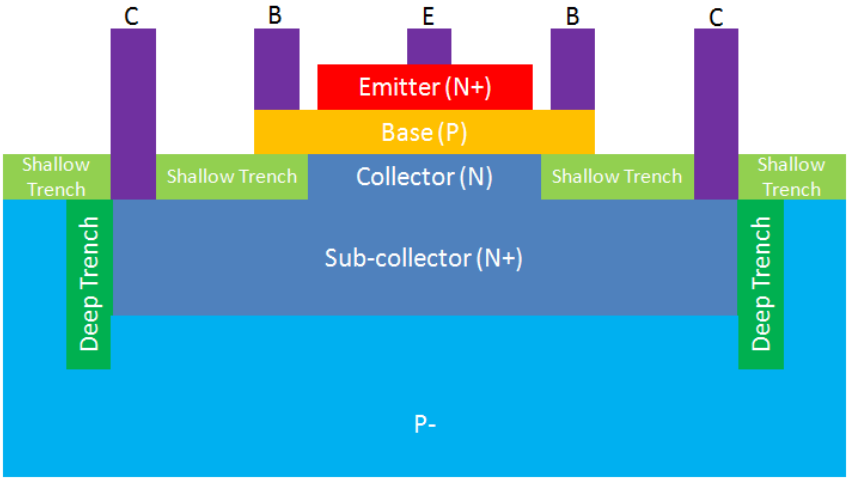


Figure 0.21: HBT-device in a SiGe BiCMOS process

Figure 2.22 depicts the structure of a desired HBT-based modulator. As it shows an insulator layer is sitting under the HBT device which helps to form a optical waveguide and push the center of the light into the base region where the free carrier density change is significant.

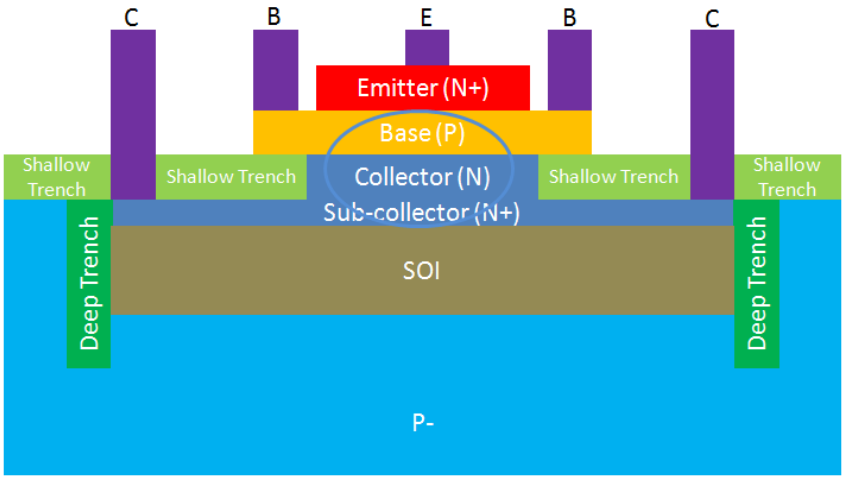


Figure 0.22: Idea of a HBT-based optical modulator

Our collaborators at Rensselaer Polytechnic Institute designed a HBT-based modulator device shown in Figure 2.23 with all the dimensions depicted [55]. The modulator is designed as the similar as possible to the HBT device in IBM SiGe BiCMOS 8HP process based on accessible information from the process design kit (PDK).

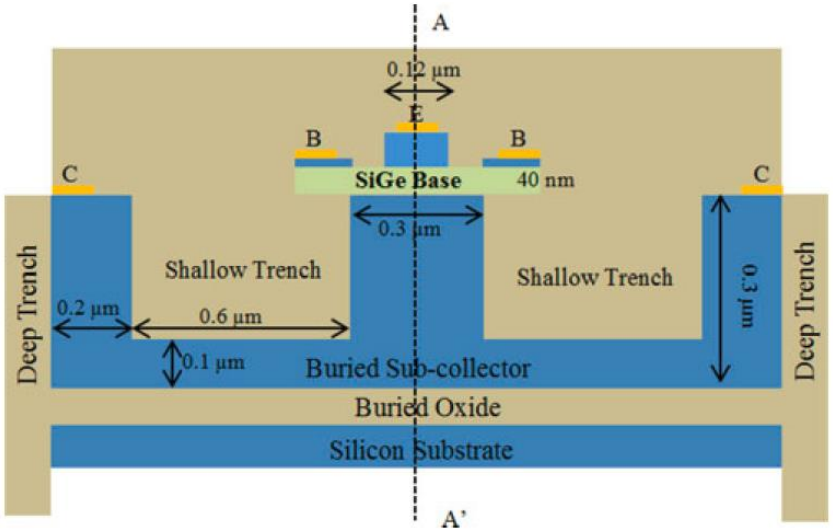


Figure 0.23: Designed HBT-based optical modulator with dimensions [55]

2.3.2 Optical property

The carrier distribution of this device under the "on" and "off" state is

simulated by using Synopsys Sentaurus. Based on the carrier distribution, the refractive index can be calculated by using Soref's equation. Then the optical property is simulated by the Beam Propagation Method (BPM) module in Rsoft and the optical field of Transverse Magnetic (TM) polarization can be achieved which is shown in Figure 2.24. As it shows the optical signal is mainly sitting in the base and subcollector region, which requires large carrier density change in this region in order to get good modulation efficiency.

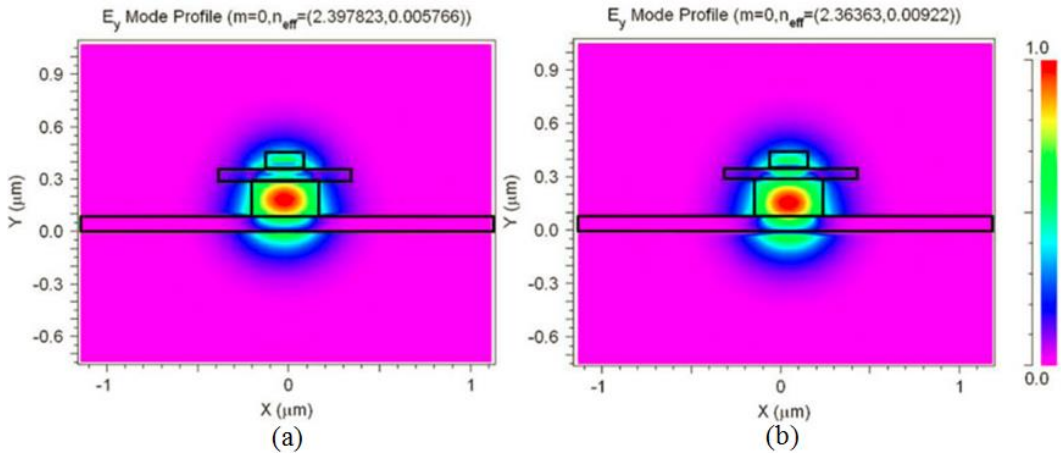


Figure 0.24: (a) TM mode OFF state, (b) TM mode ON state [55]

2.3.3 Speed

For a carrier injection modulator, the switching speed is determined by the speed of carriers injected into the intrinsic region and the speed of carriers swiped out from the intrinsic region to the ground. The intrinsic switching speed of the HBT modulator is around 30Gbps as described by Figure 2.25. It should be noted that the results are achieved under the condition of ideal driver circuit. The "Ideal" driver means the driver has zero output impedance while the driving signal has infinite short rise/fall time.

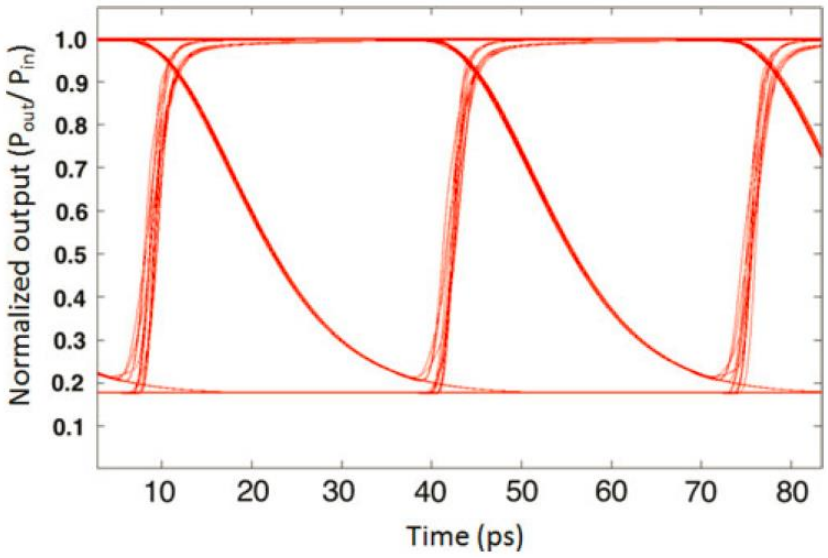


Figure 0.25: Transient response of HBT modulator [55]

For a carrier-injection HBT modulator, the small output impedance of a realistic driver circuit is a critical requirement to achieve a large base-emitter voltage swing V_{be}, which affects the extinction ratio; and to minimize charging/discharging time to achieve high data rates. Thus the performance of driver circuit determines whether the modulator's claimed performance can be achieved or not. Furthermore, there are some commonly used techniques to enhance the modulator's claimed bandwidth from the perspective of driver. Pre-emphasis is a common method to increase the speed of modulator without changing the design of modulator.

2.3.4 Extinction ratio

The HBT-based modulator can be either worked as an EOM in a MZI or as an as an EAM. EAM is mainly discussed here because it is easier to be implemented. The extinction ratio of an EAM is determined by the magnitude of the extra loss when a external electrical field is applied. The unit length loss without external electrical field (or called device intrinsic loss) is about 0.183dB/μm. By applying forward bias voltage of 0.95V cross B-E junction, the unit loss becomes 0.213dB/μm. The extra loss 0.03dB/μm will accumulate along

the modulator and determine the extinction ratio at the output of the modulator. Table 2.2 summaries the unit length loss under different forward bias voltage V_{be}. The relationship between absorption coefficient α and unit length loss can be described by equation (2.5). It can be seen from the Table 2.2 that, if V_{be} is switching between 0.1V and 0.95V, the extinction ratio of this modulator with 180μm length is (0.213-0.183)*180=5.4dB. And the insertion loss is 0.183*180=32.94dB.

$$Loss = \frac{\alpha * 4\pi * 10}{ln(10) * 1.55} \qquad (\text{dB}/\mu\text{m}) \qquad (2.5)$$

Table 0.2: *Loss* Vs V_{be}

V_{be}	Δn *imag*	α	L_π (μm)	*Loss*(dB/μm)
0.01		0.005208		0.183377396
0.1	8E-06	0.00522	96875	0.183805581
0.2	1.7E-05	0.005231	45588.24	0.184176675
0.3	2.9E-05	0.005232	26724.14	0.184233766
0.4	4.7E-05	0.00524	16489.36	0.184490677
0.5	6.9E-05	0.005267	11231.88	0.18546123
0.6	9.6E-05	0.00527	8072.917	0.185546867
0.7	0.000126	0.005299	6150.794	0.186574511
0.8	0.000186	0.005322	4166.667	0.18737379
0.85	0.000275	0.005365	2818.182	0.188886711
0.9	0.000634	0.005549	1222.397	0.195366578
0.91	0.000792	0.005635	978.5354	0.198392419
0.92	0.000967	0.005722	801.4478	0.201475352
0.93	0.001154	0.005836	671.5771	0.205500292
0.94	0.001351	0.005948	573.6491	0.209411049
0.95	0.001557	0.006076	497.7521	0.21394981
0.96	0.00177	0.0062	437.853	0.21837439
0.97	0.001989	0.00634	389.643	0.223341336
0.98	0.002212	0.00648	350.362	0.228165555
0.99	0.002439	0.00662	317.753	0.233103956
1	0.002669	0.00678	290.371	0.238641817
1.01	0.002899	0.00692	267.334	0.243751492
1.02	0.003131	0.00708	247.525	0.249146624
1.03	0.003363	0.00723	230.449	0.254456119
1.04	0.003594	0.00737	215.637	0.259537248
1.05	0.003824	0.00753	202.667	0.265246383

1.06	0.004055	0.00768	191.122	0.270527332
1.07	0.004285	0.00784	180.863	0.275979555
1.08	0.004516	0.00799	171.612	0.28148887
1.09	0.004746	0.00815	163.295	0.286884002
1.1	0.004975	0.0083	155.779	0.29230768

2.3.5 Fabrication

The first step of fabrication is through commercial foundry. By taking advantage of their comprehensive fabrication facility, the HBT structure with 0.12μm feature size is nicely fabricated. After the device is back from foundry there are several necessary post-processing steps need to be finished on the device as shown in Figure 2.26. Firstly, the die substrate is polished from 500μm down to 50μm. Then the substrate is fine etched to 27μm, which makes the subcollector thickness down to 0.1μm as designed. After that an oxide layer with 1μm thickness is grown on the backside of the device. Before polishing and etching, a cladding layer is attached on top of the die to avoid breaking.

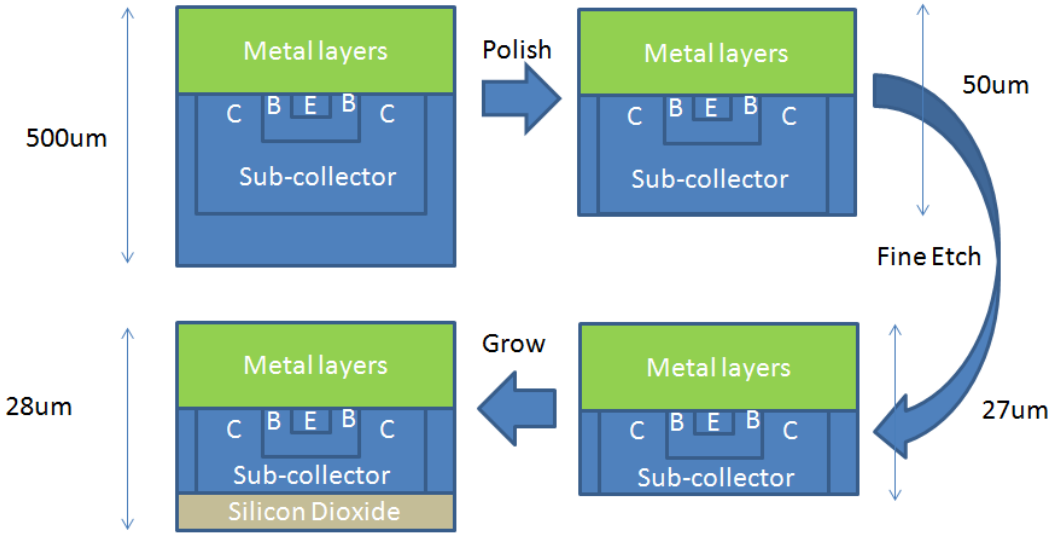


Figure 0.26: Post-processing steps

2.3.6 Electrical Model

Post-processing steps introduce several modifications to the standard electrical model provided by the foundry. The first modification is, the thinner

subcollector will introduce higher parasitic resistance, which value could be estimated as: Firstly, the original subcollector sheet resistance value can be retrieved from process PDK, which is around 8.8Ω/sq; secondly, the thickness of original and polished subcollector are 2μm and 0.1μm respectively. Thus the sheet resistance of polished subscollector should increase by 19 times accordingly, which is 167.2 Ω/sq; Thirdly, with the device length of 90μm and width of 1 μm the parasitic resistance is divided by 90 down to 1.86Ω.

It should be noted that the resistance is divided by 90 times, not multiplied. It is because the current in subcollector flows in the direction as shown in Figure 2.27 so the 90μm means multiple HBTs are paralleled. To account for this parasitic resistance, a 2Ω resistor is serially connected at the collector which gives a pessimistic estimation of the added resistance brought by thinner subcollector.

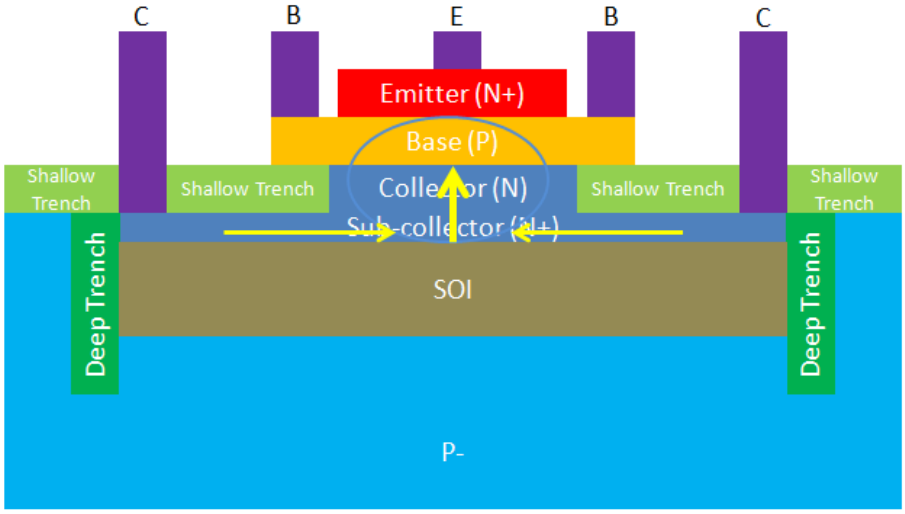


Figure 0.27: Current flow in subcollector

The second modification is, the buried oxide layer will decrease the parasitic capacitance from sub-collector to the ground as shown in Figure 2.28, which is favorable to the speed performance. Thus the simulation based on the existing model should give the pessimistic estimate from the perspective of speed.

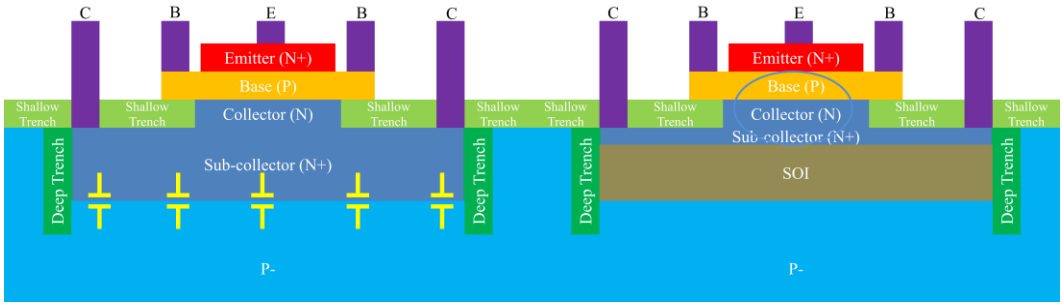


Figure 0.28: Parasitic capacitance from sub-collector to the substrate. Left: original HBT device with large parasitic; right: modified HBT device with small parasitic

The electrical model of the HBT-based EAM and its driving requirement is shown in Figure 2.29. According to Table 2.2, to achieve a 5dB extinction ratio the V_{be} should be around 0.95V[56]. For a carrier-injection modulator, small parasitic resistance R_{on} is a critical requirement as discussed before. In a driver circuit realized by a CMOS inverter, the $R_{on}=1/[\mu_n C_{ox} W/L(V_{gs}-V_{thn})]$ which is directly related to the process node. For the 130nm process, R_{on} is approximately 9Ω and for a 45nm process, R_{on} can be as low as 2Ω. Thus, deep sub-micron processes are favorable for carrier injection modulators.

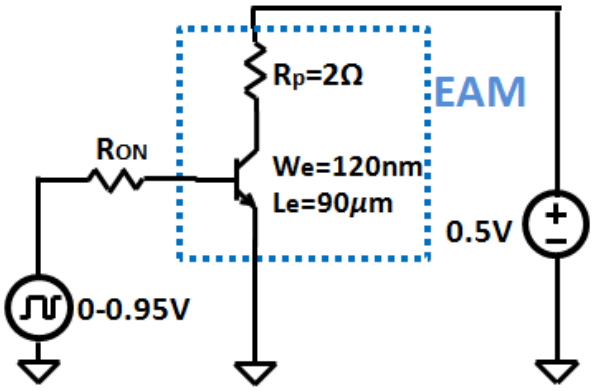


Figure 0.29: Electrical model and driving interface of the carrier injection HBT-based EAM

2.4 Summary

This chapter firstly covers the background information of traditional optical communication systems including the introduction of some major

specifications. Then, silicon optical modulator is took out from the system and discussed in detail. Firstly, the free carrier plasma effect is introduced, which is a major EO effect in silicon material and the fundamental mechanism of this research work. Secondly, the modulator structure varieties are introduced which includes EOM, EAM and resonant cavity based modulators. After that, three different configurations of free carrier plasma effect are introduced: injection, depletion and accumulation. They are compared from different perspectives. And finally the definition of "ideal" modulator is presented.

With the background information of optical modulator, a SiGe HBT-based carrier injection EAM design is introduced in section 2.3. Firstly, the device structure is presented. After that the optical simulation and electrical eye diagram simulation results are discussed. Then the extinction ratio under different bias conditions is presented. Fabrication steps are discussed after that with the introduction of every post-processing step. At the end, the modified electrical model after post-processing is proposed based on some reasonable calculations.

Chapter 3

A 10Gbps monolithic optical transmitter module design

To implement the HBT-based modulator design discussed in Chapter 2 by using IBM SiGe BiCMOS 8HP process, there are a quite a few things needs to be considered but not just drawing the 2D layout in design tool and sending it out to the foundry. This chapter is going to address the complete design process from the physical layout adaption to the post-processing steps. The driver circuit will be discussed in detail and the monolithic transmitter solution will be proposed. At the end of the chapter, some optical and electrical measurement results will be discussed.

3.1 Modulator physical design

Some special treatments are required during the physical design phase of modulator. The layout of HBT PCELL of this process is depicted in Figure 3.1(a). As it shows the device is surrounded by deep trench from all four sides. Due to the deep trench is made of SiO_2 which has considerable attenuation to the light, it needs to be cut off along the light path as shown in Figure 3.1(b). Thus, firstly the layout of standard HBT PCELL is flattened in Cadence layout editor; then the deep trench layer is picked out and sections along light path are cut out.

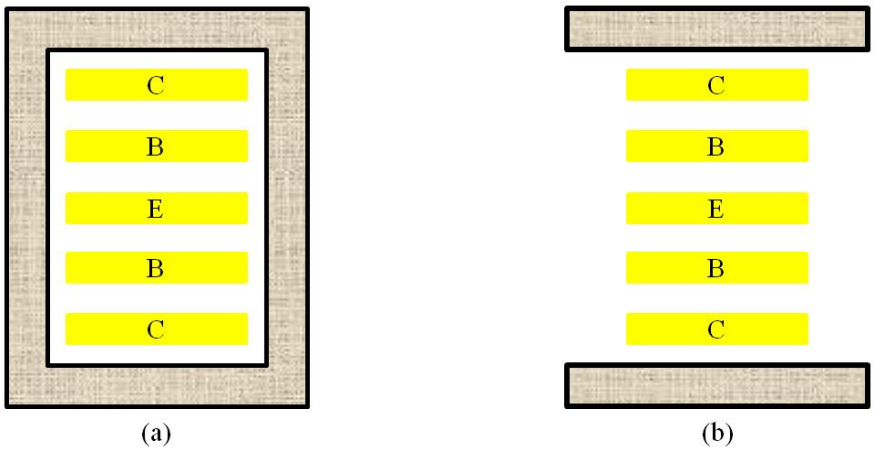


Figure 0.1: Take off deep trench layer along the light path

The second treatment is, the required emitter length for HBT-modulator should be around 90μm to get at least 5dB extinction ratio with driving voltage of 950mV. However, the maximum emitter length of a single HBT modulator in the standard PCELL is 18μm. Thus multiple HBT modulators need to be parallel connected as shown in Figure 3.2.

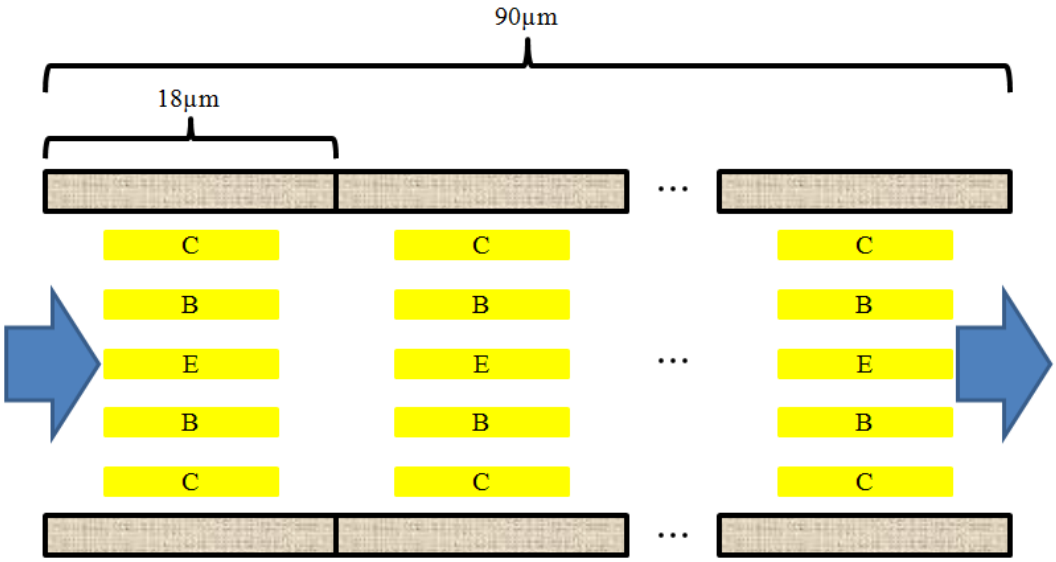


Figure 0.2: Parallel connect multiple HBTs

With the special modifications to the standard PCELL, there emerges some design rule violations. To make sure it can be fabricated, all the class A

errors are corrected out which otherwise will be unacceptable to the foundry. For example, it's desirable to put two short HBT as close as possible to minimize the extra attenuation provided by silicon in between. However, a class A rule exists which limits the minimum distance of two separate HBTs.

3.2 Modulator electrical interface

To characterize the electrical performance of modulator, firstly, the modulator is characterized by sweeping the V_{be} and biasing the V_c and V_e to ground while monitoring I_b, I_c, and I_e. The schematic of simulation setup is shown in Figure 3.3 and results are shown in Figure 3.4. As it shows, when V_{be} is 950mV both B-E and B-C junctions are forward-biased with I_b, I_c, and I_e of 21.4mA, -14.1mA and -7.3mA respectively.

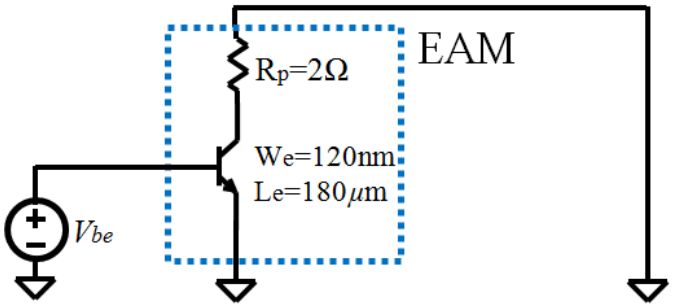


Figure 0.3: DC characterization with sweep of V_{be}

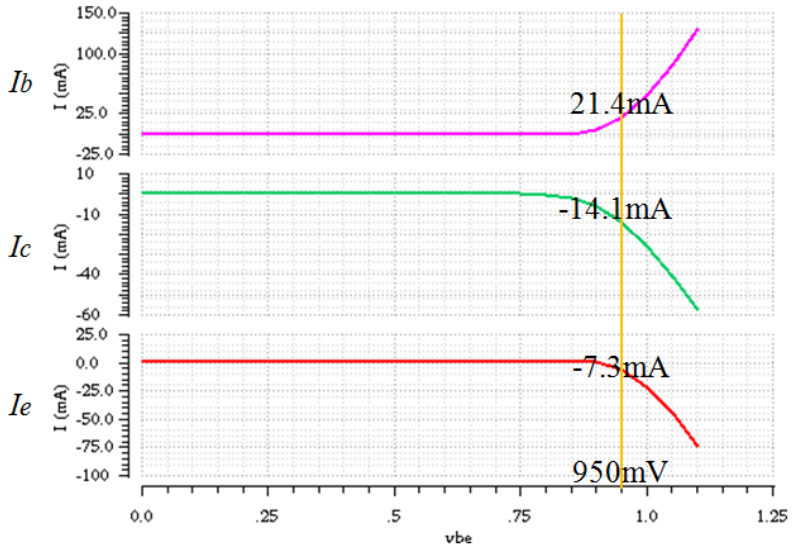


Figure 0.4: DC I_b, I_c, and I_e with sweep of V_{be}

Transient simulation is implemented in order to get a transient behavior of the modulator under different logic state. The configuration is, the V_{be} is stimulated by a 5GHz square wave (50% duty cycle) with 0V to 950mV swing while the V_{ce} is biased at 100mV as shown in Figure 3.5. It should be noted that both the square wave voltage source and DC voltage source are ideal with no parasitic.

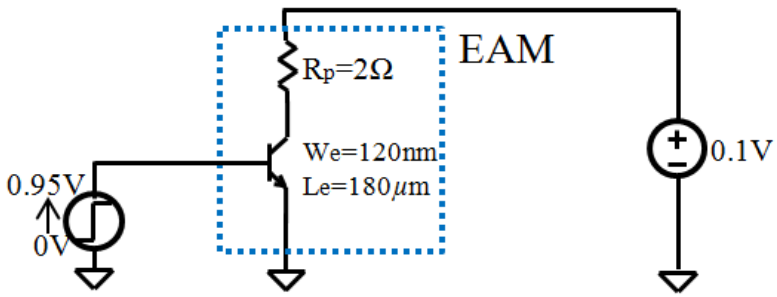


Figure 0.5: Modulator driving interface (ideal)

Under the condition, the transient behavior of the modulator at 5GHz is simulated and results are shown in Figure 3.6. It can be seen that:

1. At time T_1, both B-E and B-C junctions are forward-biased with HBT working in the saturation region. The value of I_b, I_c, and I_e are 88.9mA, -58.2mA and -30.7mA respectively.

2. At time T_2, the base voltage is switched from 950mV to 0V which makes the HBT switched to the cut-off region. The free carriers across the intrinsic region of B-E and B-C junctions are swept out thus a big discharge current peak at the logic '1' to '0' transition can be seen for I_b.

3. At time T_3, the base voltage is stably at 0V so the HBT is stably sitting in the cut-off region. The value of I_b, I_c, and I_e are all very close to zero.

4. At the same bias voltage, the transient current is much higher than the DC current compared to Figure 3.4, which is due to the most of the transient current is used to charge or discharge the 'huge' junction capacitance C_{je} and C_{jc} and the junction oxide capacitance C_{beo} and C_{bco}.

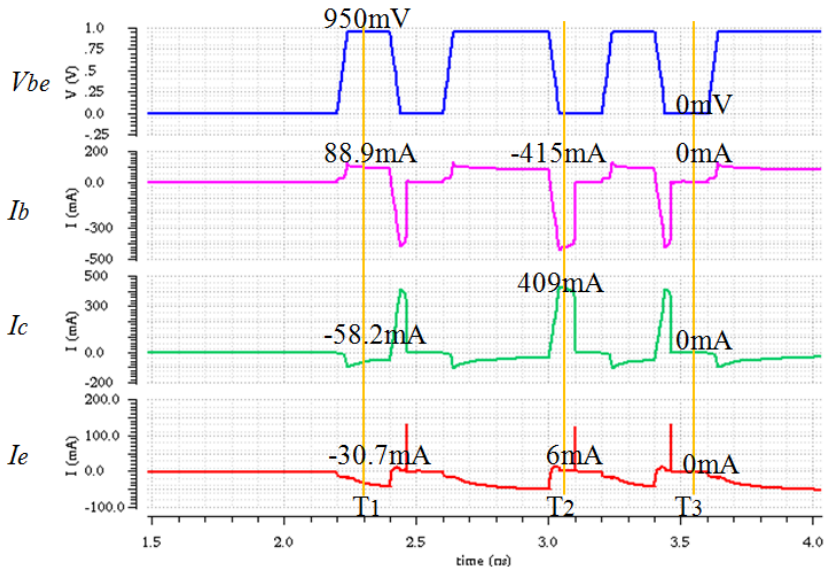


Figure 0.6: Transient I_b, I_c, and I_e

The collector current change is drastically from -58.2mA to 409mA. In reality a non-negligible series inductor will hinder the high speed AC current going through it. Thus, a big decoupling capacitor C_{decpl} is need at the collector to behave as a "charge reservoir" which supplies the AC current as Figure 3.7 shows.

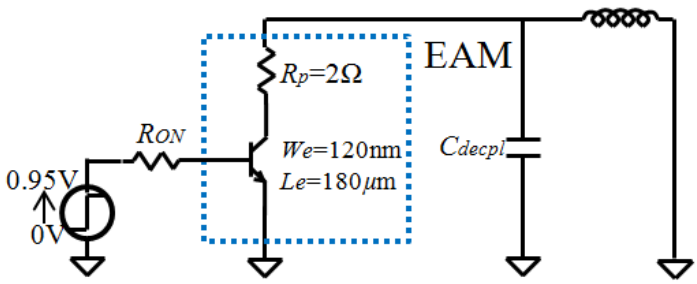


Figure 0.7: Modulator driving interface (realistic)

With C_{decpl} the voltage at the collector is stabilized. As it shows in Figure 3.8, the variance of V_c is kept within -50mV to 90mV which is very close to desired value--0V.

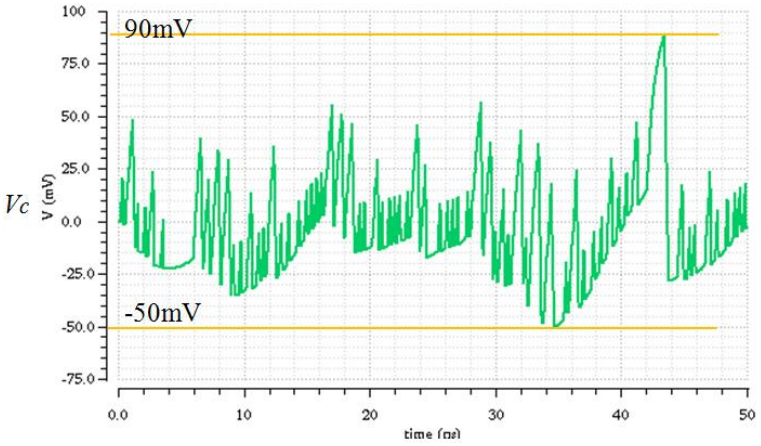


Figure 0.8: Transient simulation with parasitic

It should be noted that, both base and emitter terminals will have considerable AC current, which means they are very sensitive to the parasitic inductance and resistance. Thus, to keep parasitic as small as possible at base and emitter is also very important.

3.3 Modulator driver

The driver needs to supply large current to the base at very high speed according to transient simulation in Figure 3.6. However, according to DC simulation results in Figure 3.4, a large portion of the transient current flows back

and forth across the parasitic junction capacitor, but not into the intrinsic base. This is due to the PN junction capacitance is exponential proportional to the forward bias voltage as described in equation (3.1). Here V_f is the forward bias voltage; V_{bi} is the built in junction voltage; C_0 is the zero-bias junction capacitance; while m is the junction grading coefficient.

$$C_j(V_f) = \frac{C_0}{(1-\frac{V_f}{V_{bi}})^m} \tag{3.1}$$

The large parasitic capacitor considerably slows down the voltage building across it, which slows down the speed of modulator accordingly. To deal with that, in the driver circuit a large buffer stage is needed to provide more current to the modulator. The block diagram of the driver circuit is shown in Figure 3.9.

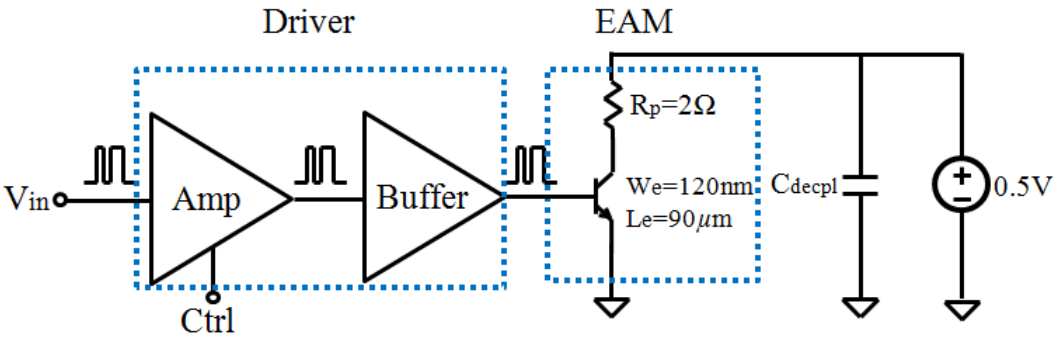


Figure 0.9: Driver block diagram

According to Table 2.1 in Chapter 2, the V_{be} determines the extinction ratio of the modulator. The driver is designed with adjustability to the extinction ratio by making V_{be} adjustable. The schematic of amplifier circuit is shown in Figure 3.10.

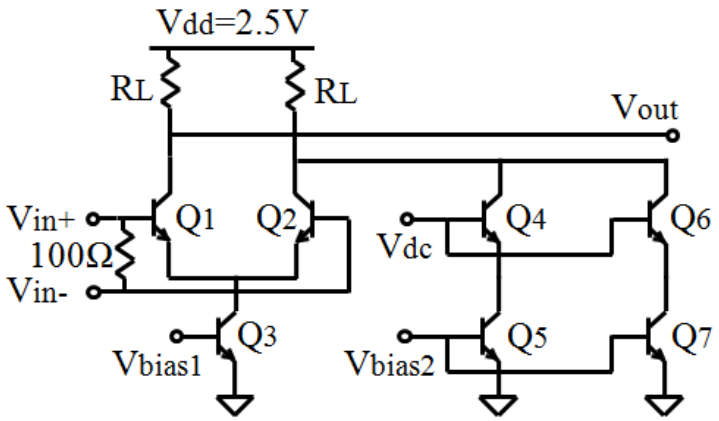


Figure 0.10: Amplifier circuit

Differential PRBS signals are supplied to inputs of the amplifier V_{in+} and V_{in-}, which have 100Ω resistor across them as impedance matching termination. The differential signals are getting amplified by CML stage comprised by Q_1, Q_2 and Q_3. Tail current I_{Q3} is controlled by V_{bias1} with an adjusting range of 10mA to 15mA. The load resistance R_L is selected to be as low as 40Ω to provide small *RC* constant at the node of output node. Thus, the adjustable swing of V_{out} will be 500mV to 600mV. The waveform in Figure 3.11 shows the swing of V_{out} changing with different value of V_{bias1}. As it shows, V_{bias1} is a very sensitive node which requires 'clean' DC signal. Thus, a 10pF decoupling capacitor is added across the node to ground and very close to the base of Q_3, to stabilize the voltage of that node.

Q_1/Q_2 are designed with minimum size to fully switch the tail current. The differential input voltage is set to 150mV while common mode voltage is set to 1.575V. To ensure Q_3 remains in its active region, the power supply voltage V_{dd} is set to 2.5V which provides sufficient headroom for the transistors.

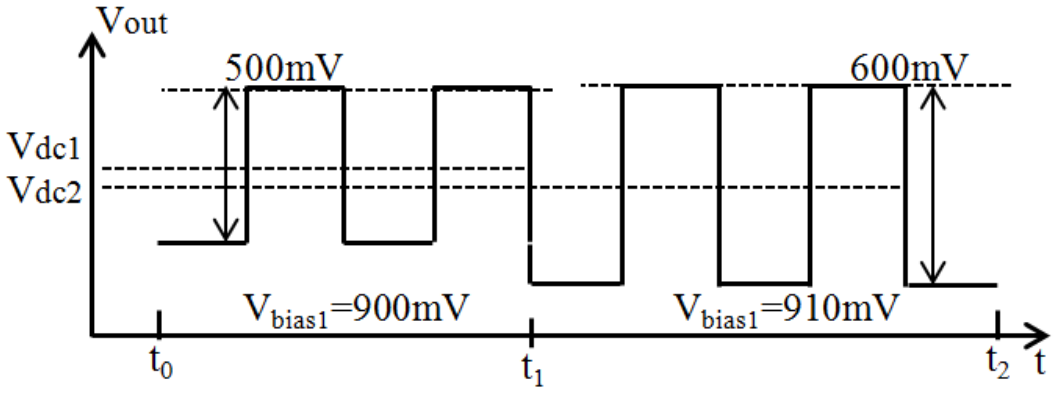


Figure 0.11: V_{bias1} controls the swing of V_{out}

Branches Q_4/Q_5 and Q_6/Q_7 are two precise current sources which designed to achieve precise DC voltage of V_{out}. As a design feature, the DC voltage of V_{out} can be adjusted by changing the value of V_{bias2}. The waveform in Figure 3.12 shows the DC voltage of V_{out} changing with different value of V_{bias2}. The bias current I_{bias} is adjusted 3mA more which introduce 120mV DC voltage drop from V_{dc1} to V_{dc2}. Again, due to the sensitivity of this node a 10pF decoupling capacitor is added across this node to the ground.

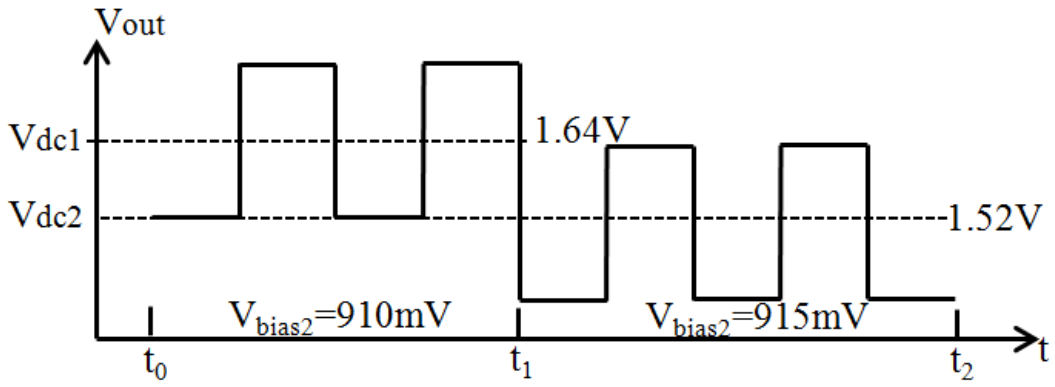


Figure 0.12: V_{bias2} controls the DC bias of V_{out}

To ensure a buffer voltage gain close to unity, a current source is placed at the emitter of the buffer HBT (Q_1) to increase the gain. This current source is also designed to decrease the discharge time. Two topologies using coarse and precise current sources are shown in Figure 3.13. For a precise topology, the transistor stack consisting of Q_2 and Q_3, as shown in Figure 3.13(a), requires a high

collector voltage V_{be} to ensure that the base-to-collector junction of Q_2 is always reverse-biased. Without this condition, the base current of Q_3 will be considerable and the discharge process will be very complex. Therefore, V_{be} should always remain higher than 1V in this case. However, this condition is not acceptable for the modulator device due to reliability concerns. Thus a coarse current source topology is selected for this design. For this design, the collector voltage of Q_3 in Figure 3.13(b) can be as low as 0.5V. And the value of bias current I_{Q3} is about 135mA.

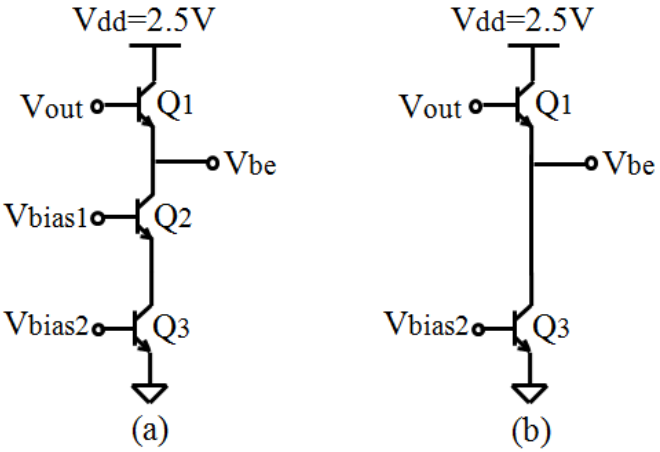


Figure 0.13: Emitter follower buffer (a) precise and (b) coarse current source

Source follower and emitter follower are two common buffer circuit. With the availability of NPN bipolar transistors, the driving capability is much higher compared to same size NMOS transistors, which means the parasitic capacitance is much smaller and the speed performance will be better. In the meanwhile, better speed performance comes with higher power budget, because the required minimum V_{ce} is about 200mV higher than V_{ds} which directly added to the required power supply voltage. The disadvantage for this CML buffer is high DC power consumption because the current source is always turned on. The post layout transient simulation results are shown in Figure 3.14. The difference of base current at logic 'one' and 'zero' is very clear, while the big discharging current peaking at the logic 'one' to logic 'zero' transition is shown as expected.

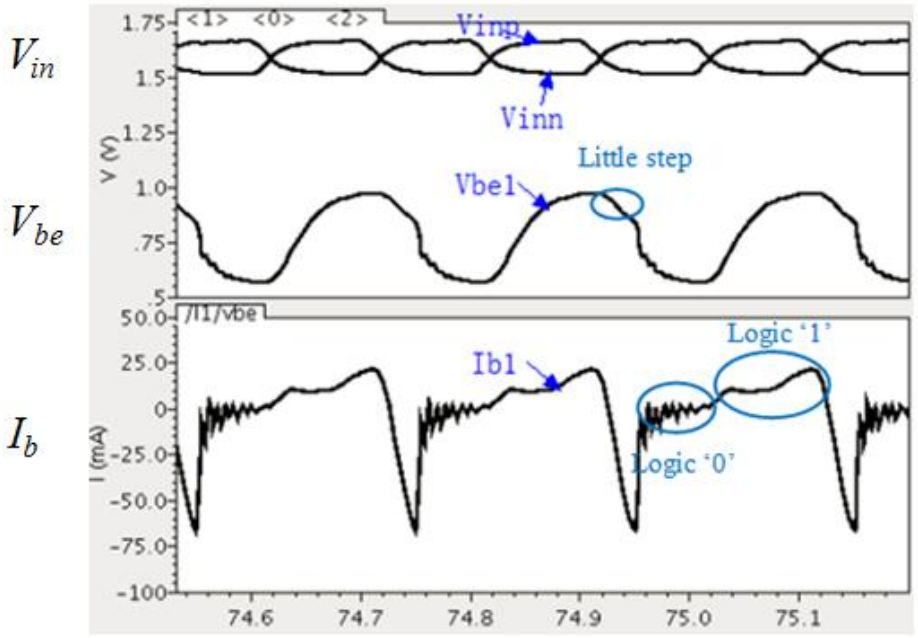


Figure 0.14: post-layout transient simulation results of driver

The total power consumption of this optical transmitter at the data rate of 5Gbps is 450mW, including the amplifier (112.5mW), the buffer (337.5mW). Here the power consumption of the buffer includes the power consumption of the modulator device. The figure of merit (FOM) described in equation (3.2) describes the power efficiency of the driver, which equals to 90pJ/bit.

$$FOM = \frac{Power}{Data\ rate} \tag{3.2}$$

Table 3.1 shows the summary of this driver design. As it shows, this transmitter module has outstanding low driving voltage and comparable speed and extinction ratio. The optical bandwidth is much broader than [50] which is resonant based modulator.

Table 0.1: Comparison of carrier-injection modulator based transmitter

	[30]	[50]	This work
Structure	MZI	Ring	EAM
Speed (Gbps)	10	12.5	5
FOM (pJ/bit)	5	0.3	90
Driving voltage (V)	7.6	3.5	0.95
Extinction ratio (dB)	6-10	10	5.5
Optical bandwidth (nm)	NA	0.1	50

3.4 Layout and fabrication

The optical driver and modulator designed and fabricated monolithically using IBM 130nm SiGe BiCMOS process. The chip microphotograph is shown in Figure 3.15. Two single modulator devices are implemented as test structure in the same chip, which are used for DC characterization of the modulator performance. The die area of transmitter is about 2.4mm×1.4mm. Layout is symmetrically designed to protect the signal integrity. Signal pads are placed on the left side of the chip with DC pads symmetrically placed along the top and bottom of the chip pad frame. Modulator is connected to the driver as close as possible to minimize the parasitic inductance and resistance. For the same reason, the decoupling capacitors are placed as close as possible to the modulator device.

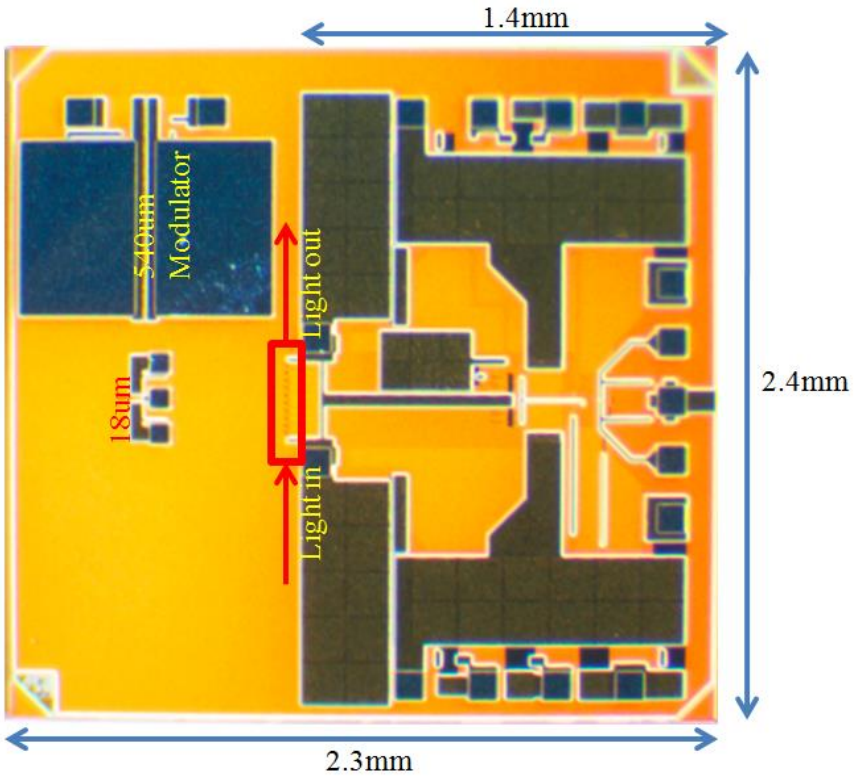


Figure 0.15: The microphotograph of chip layout

A special concern should be treated to the routing between driver and modulator because the large AC current I_b and I_c discussed in section 3.2 may introduce the electro-migration problem to it. Modulator device has five contacts (CBEBC) to be routed to driver with one option of seven layer metals in the process. An extra limitation is, all the routings should go from the same side to the modulator, as Figure 3.16 shows. This is due to the rest of three sides will be used for light coupling or diced out during chip post-processing.

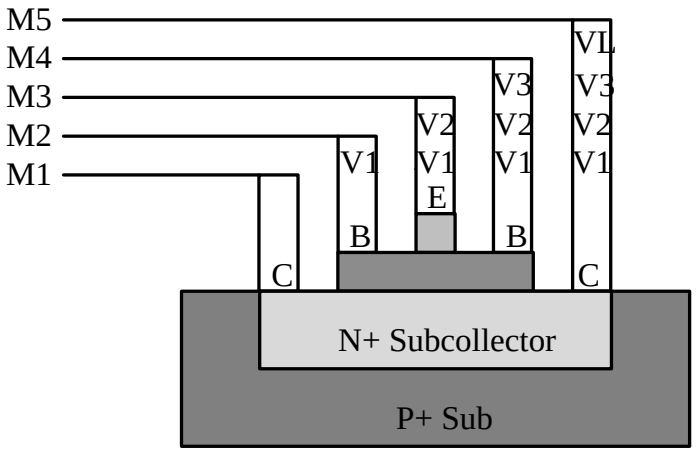


Figure 0.16: Cross-sectional view of routing scheme for the modulator device

Moreover, the two base contacts needs to be routed together and it's the same case for the two collector contacts. A limitation is the wire width needs to be as wide as possible to avoid the possibility of electro-migration. In the meanwhile, the maximum width cannot be larger than the emitter width because the two ends of the modulator device will be used for light coupling. Thus, a special treatment is implemented to connect those contacts while keeping the routing width close to emitter width. Figure 3.17 shows the idea of the scheme. The two collectors are implemented by metal 1 and metal 5 and connected by a stack of vias at the ends of the device, without touching metal layers in between. The two base are implemented by metal 2 and metal 4 and connected together by a stack of vias which go across the intervals of metal 3 strips. The metal 3 strips are used to connect to the emitter contact as show in Figure 3.17.

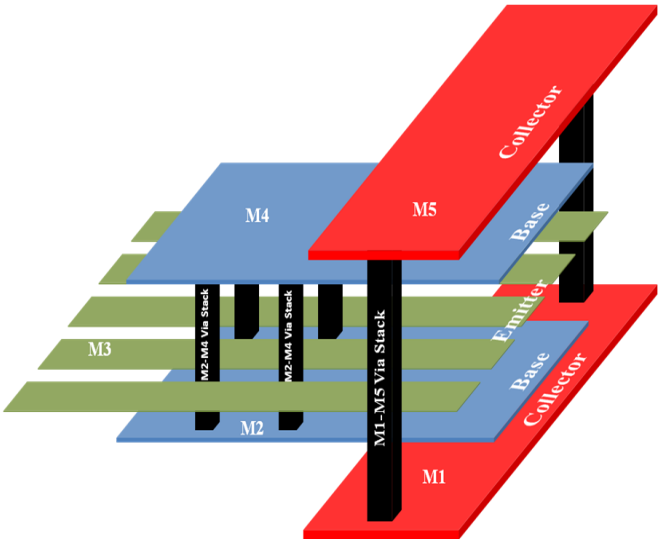


Figure 0.17: Scheme of connecting two bases and collectors together

3.5 Chip post-processing

The post processing includes backside processing steps and front-end laser cutting. Backside post-processing, by sequence, includes polishing, fine etching and oxide growing. Front-end laser cutting is for light coupling. Figure 3.18 shows the SEM picture after backside polishing and fine etch. The deep trenches can be easily seen.

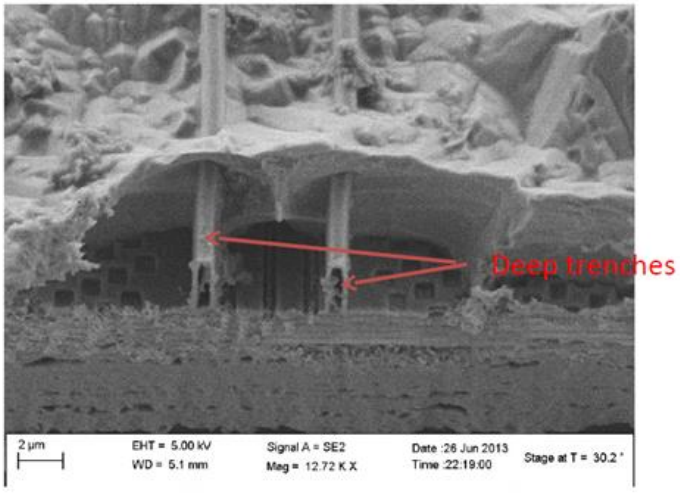


Figure 0.18: SEM picture after backside polishing and fine etch

The chip after the front-end cutting is shown in Figure 3.19. Laser cutting is used but not the dicing saw because it can provide precise traveling distance and can stop at a specific position but not cut through.

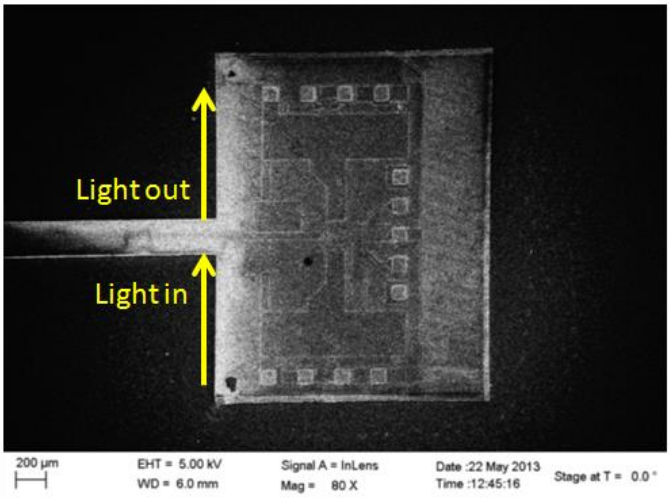
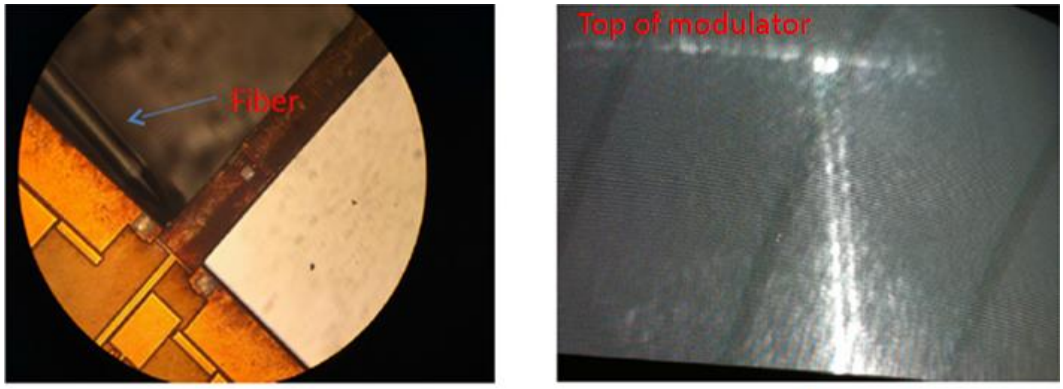


Figure 0.19: SEM picture after front-end laser cutting

3.6 Optical measurement

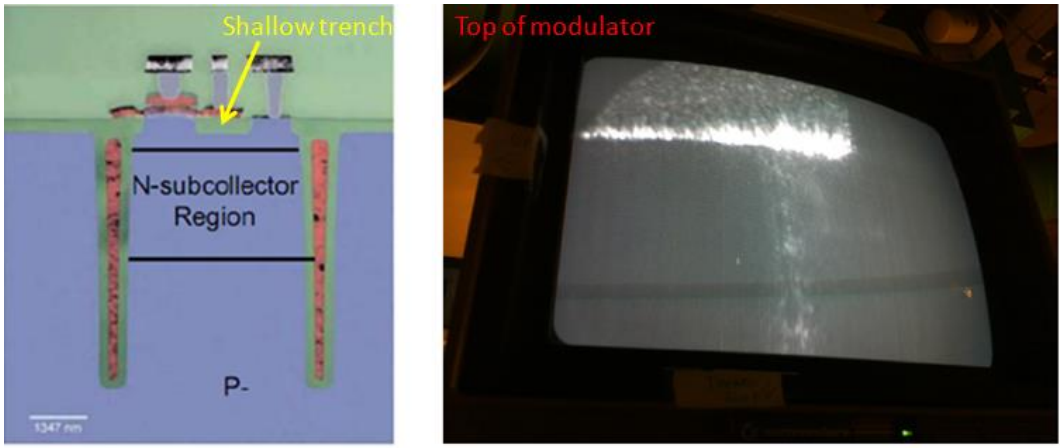
The optical test is implemented after the post-processing steps. Figure 3.20(a) shows a tapered optical fiber is used to couple the light into the modulator. The light is observed on top of the modulator, which is shown in Figure 3.20(b). The light can be seen at the two deep trench area, which proves the light wave-guiding.



(a) (b)

Figure 0.20: Light coupling through subcollector

The light coupling test is also performed in the collector and base area, however, there is no light detected as shown in Figure 3.21(b). The reason we found is, there is a shallow trench layer which covers all the non-active regions. The shallow trench is made of silicon dioxide which is not an optical waveguide material. Unfortunately, different from deep trench, the shallow trench is not a customized layer.



(a) (b)

Figure 0.21: Light coupling through the collector and base area

3.7 Electrical measurement

On the same die we put some test structures of signal HBT devices, which ar not connected to driver circuit as the main design. There structures are used to verify the functionality of the modified HBT PCELL. As Figure 3.15 shows, the HBT emitter length is 540um which is realized by serialize thirty 18μm HBT transistors. The DC *I-V* curve is tested using HP 4155A semiconductor parameter analyzer. The measurement result is shown in Figure 3.22.

Although we could not do AC signal measurements because all electrical AC signals compensate each other inside the chip (We expected to get AC optical results instead). However, we can still do the DC measurements to make sure the fabrication is correct. In the meanwhile, because the HBTs are modified in the

Cadence layout designer as discussed above, the verification of their function is very important.

Instead of using three DC probes, we bonded the 540μm modulator to three random pins of a PGA-144 package to get better connection to the pads. We use HP4155A precise semiconductor parameter analyzer to characterize the long modulator. Firstly, we test the I_c-V_{ce} curve. We get the dataset from HP4156A and plot it by using MATLAB. Figure 3.22 shows the I_c at the case of I_b swept from 1μA to 10μA with 1μA step and of V_{ce} swept from 0V to 1.4V with 10mV step. Figure 3.23 shows the simulation results in Cadence.

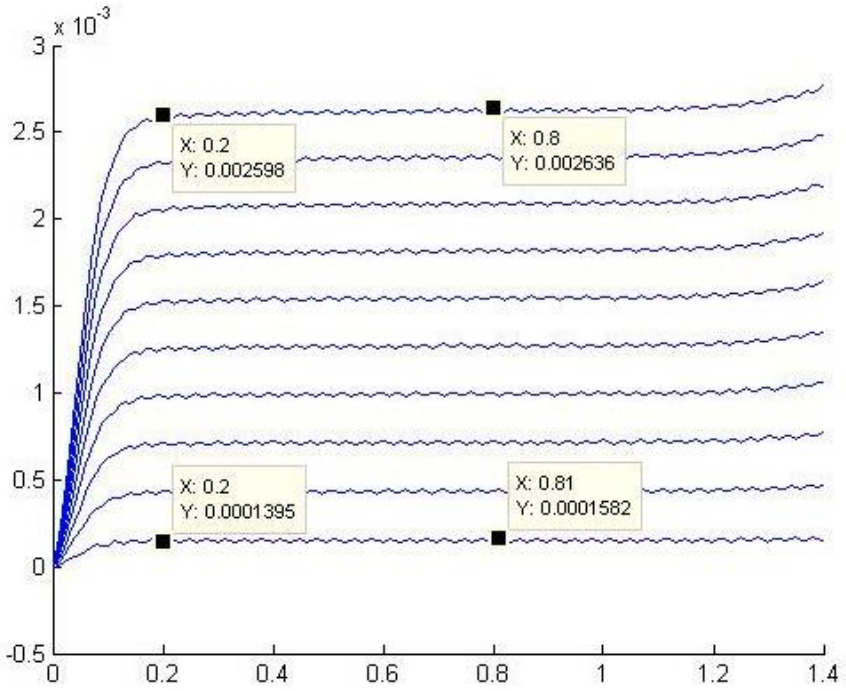


Figure 0.22: Tested I_c vs V_{ce} curves (I_b sweep from 1μA to 10μA with 1μA step)

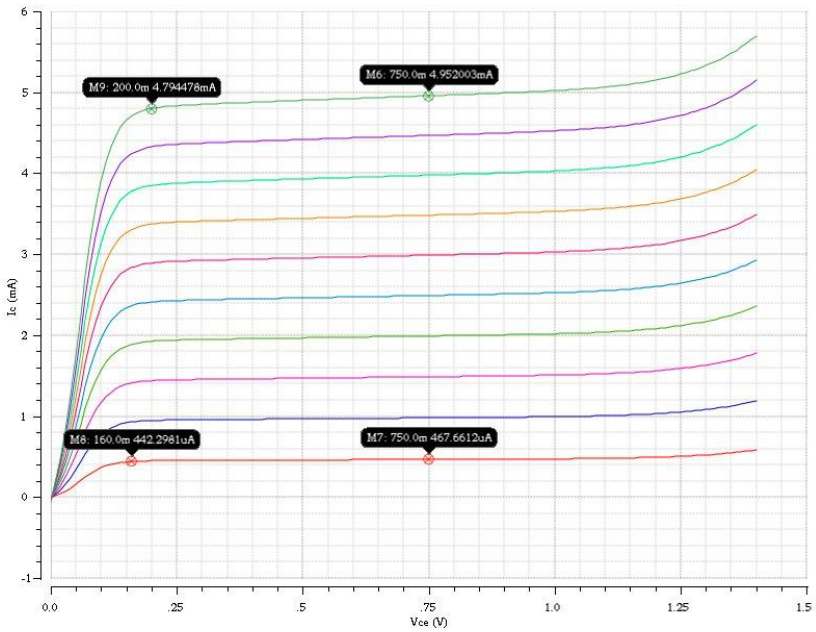


Figure 0.23: Simulated I_c vs V_{ce} curves (I_b sweep from 1μA to 10μA with 1μA step)

The Table 3.2 summarizes the difference of them. As you can find from the Figure 3.22, 3.23 and Table 3.2, the tested β value is considerably smaller than the simulated value.

Table 0.2: Comparison of Figure 3.22 and Figure 3.23

	Tested	Simulated
I_c @ I_b=1μA	158.2μA	467.66μA
β@ I_b=1μA	158.2	467.66
I_c @ I_b=10μA	2.636mA	4.95mA
β@ I_b=10μA	263.6	495

Figure 3.24 shows the I_c at the case of I_b swept from 10μA to 100μA with 10μA step and of V_{ce} swept from 0V to 1.4V with 10mV step. Figure 3.25 shows the simulation results in Cadence.

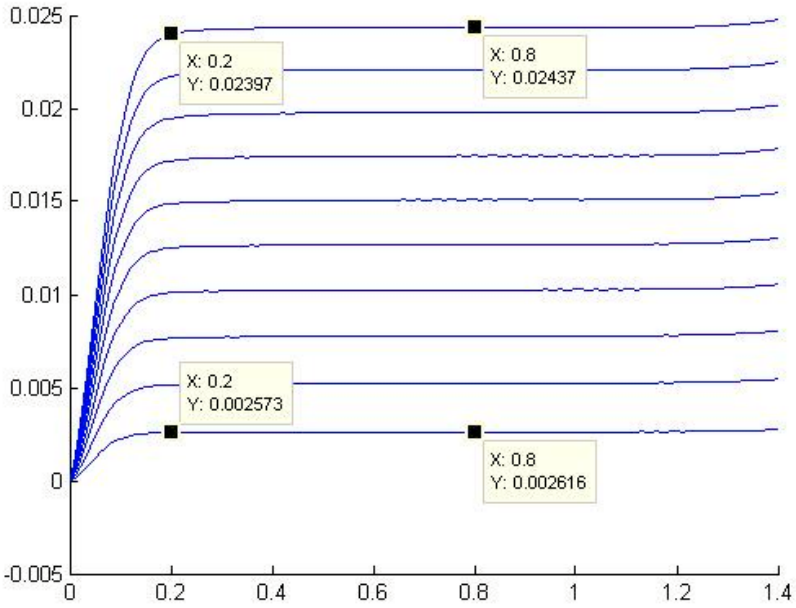


Figure 0.24: Tested I_c vs V_{ce} curves (I_b sweep from 10μA to 100μA with 10μA step)

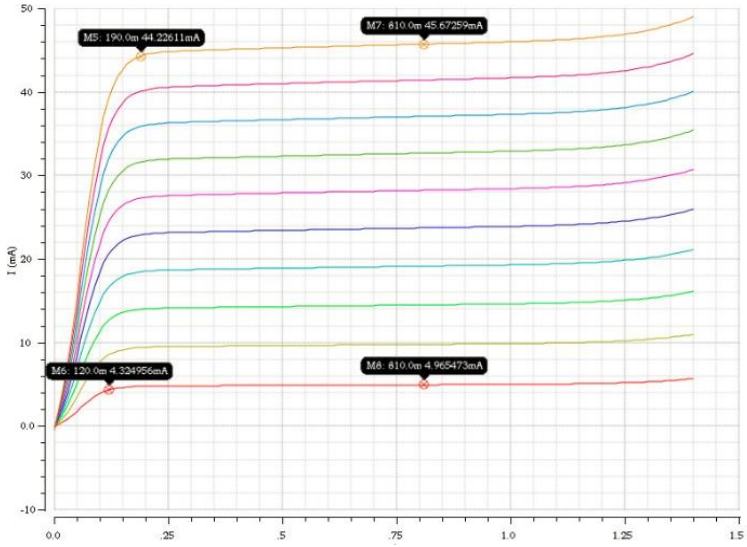


Figure 0.25: Simulated I_c vs V_{ce} curves (I_b sweep from 10μA to 100μA with 10μA step)

The Table 3.3 summarizes the difference of them. As you can see, except the big difference of β, the curve shape and the V_{ce} (sat) are pretty close for the test and simulation results. According to the test results shown in MOSIS website and 8HP model guide, the tested β is in the range of 337 to 510. Because the

results of this run (V21F) has not been posted, we could not get a good reference to determine the origin of the decrease of the β. However, as PDK indicates, the tested β should be probably smaller than simulation.

Table 0.3: Comparison of Figure 3.24 and 3.25

	Tested	Simulated
I_c @ I_b=10μA	2.616mA	4.97mA
β@ I_b=10μA	261.6	497
I_c @ I_b=100μA	24.37mA	45.67mA
β@ I_b=100μA	243.7	456.7

Figure 3.26 shows the tested I_c, I_b and β versus V_{be} curves (or linear scale Gummel plot). As you can see the β reaches its peak 273.4 when V_{be} is around 0.75V.

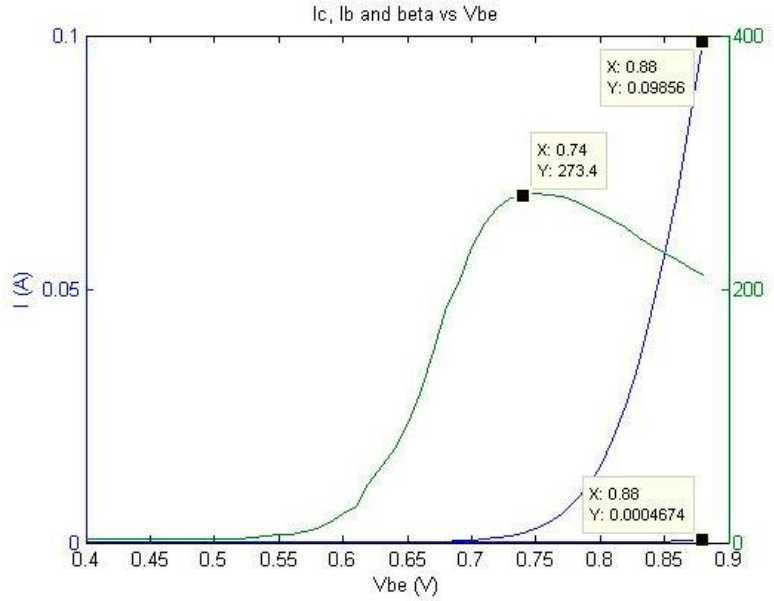


Figure 0.26: tested I_c, I_b and β versus V_{be} curves

3.8 Summary

This chapter discussed a 10Gbps optical transmitter design using a 130nm

SiGe BiCMOS process. Firstly, the physical layout design is discussed, which includes the special modifications to the standard HBT PCELL. Secondly, the electrical model of modulator is simulated by both DC and AC. Based on the result it's aware that the interconnect between modulator and driver is very sensitive to the parasitic inductance and resistance. A 10Gbps driver design by using pure bipolar transistors is discussed by each stage.

A special routing design is presented which takes care of the potential electro-migration issue. After that, the post-processing steps are discussed. Optical measurement results show some expected optical coupling at the collector region, and however, there is no light can be coupled through the sub-collector region, which is not expected. The reason we found is the shallow trench structure block the light in this area. Since shallow trench layer is not a customized layer, it's not feasible to take the layer off unless we find a highly customized foundry service. Although this is an obstacle we cannot overcome currently, it's possible to resume the fabrication if the foundry help is accessible.

Finally the measurement result for some HBT test structures are presented. The measured *I-V* curves show the normal functionality of the modified HBT PCELLS.

Chapter 4

A ultra-low power optical driver design

The two most important specifications of an optical transmitter are speed and power consumption. People have put much effort to increase the speed from hundreds of mega hertz to nowadays tens of giga hertz class by inventing modulator with faster speed, which is usually the limit factor of the system speed. However, the potential of modulator is not always fully achievable due to the strict driving condition. For example, a modulator required an AC driving voltage of 4V means the transistors in driver circuit have to sustain 4V voltage swing, i.e. have breakdown voltage higher than 4V. However, the breakdown voltage and f_T of a transistor are always compromised to each other. In [57], the achieved data rate is 20Gbps with the same limitation.

The other scenario is, sometimes the driving requirement can be realized, but at a high cost. The cost can mean much higher power consumption by using HBT transistors with high breakdown voltage [58], or by using power consuming CML circuits as the design in Chapter 3[59][60][61][62]. The cost can also be much more money by using expensive process such as Indium Phosphide (InP) HBTs [63][64], which cost several times higher than silicon process.

This chapter is going to present an ultra-low power transmitter design by using low cost 0.13μm BiCMOS process. For driver circuit, which is the most power consuming portion of transmitter, the CMOS logic is adopted to save the power. By using 1.5V low voltage transistor, the speed and power consumption have a good comprise to each other.

4.1 Block diagram

CMOS logic, compared to CML, is much more power efficient because it doesn't have static power consumption. At the same time, CMOS logic has rail-to-rail voltage swing. Both merits make CMOS logic circuits as a good candidate for driver circuit design. The transmitter includes a pre-emphasis driver, a pre-driver and an integrated 2^7-1 full rate PRBS generator as shown in Figure 4.1. The PRBS generator adopts CML in order to guarantee the speed performance. A CML/CMOS hybrid logic pre-driver stage is inserted between CML PRBS generator and CMOS logic pre-emphasis driver in order to provide logic transition.

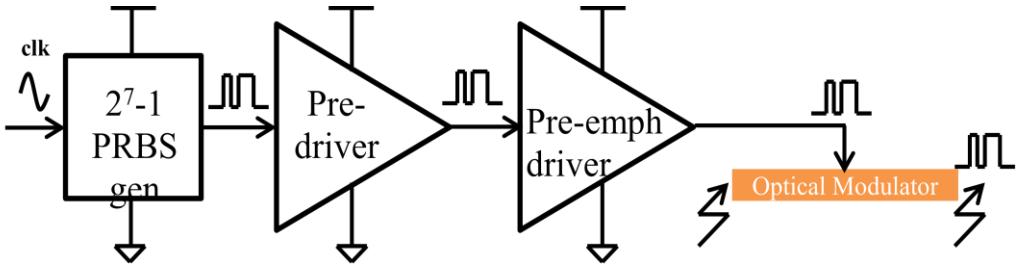
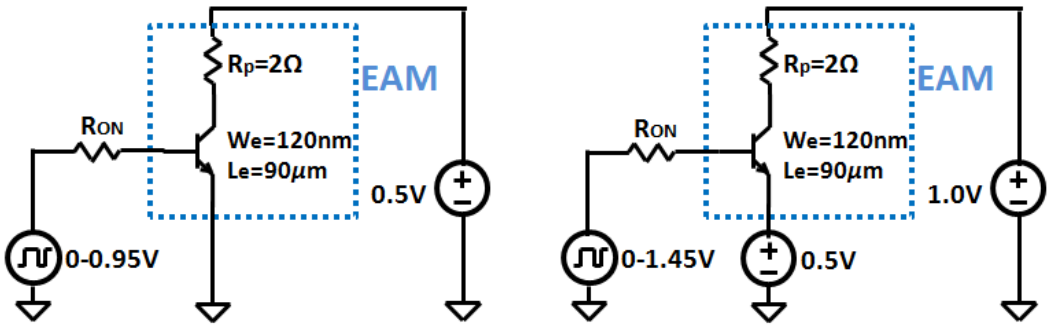


Figure 0.1: HBT-based EAM transmitter circuit

The CMOS pre-emphasis driver can provide 0.95V voltage swing to the base terminal in the regular mode as shown in Figure 4.2(a). Different from it, Figure 4.2(b) shows a new driving interface in which the voltages of the three terminals of HBT are all raised by 0.5V. The new driving interface can provide 1.45V voltage swing to the base terminal with forward V_{be} of 0.95V and negative V_{be} of -0.5V. The modification will generate a negative V_{be} during the discharge period, resulting in a significant increase in speed.



(a) (b)

Figure 0.2: Electrical model and driving interface of HBT EAM (a) regular, and (b) all terminal biases raised by 0.5V

4.2 Pre-emphasis driver

Pre-emphasis is a first order feed forward equalizer which is popularly used for increasing the logic transition speed. The idea of it is to add a positive peaking at the edge of logic zero to one transition and negative peaking at the edge of logic one to zero transition to increase the rising and falling speed. It was firstly proposed to be used for driving a LED in [65]. Nowadays this technology can be broadly applied to many different data communication applications, such as 100Gb/s-Ethernet [66][67], on chip bus [68][69][70], liquid crystal display (LCD) [71], hard disk drive (HDD) [72], LED for visible light communication (VLC) [73][74][75], and vertical cavity surface-emitting laser (VCSEL) communication [76][77][78][79]. The modeling of pre-emphasis driver were discussed in [80][81][82][83] which provide mathematical foundation to the technology.

The pre-emphasis driver for the HBT-based carrier injection modulator is designed and proposed in Figure 4.3. It is comprised of a main driver in parallel with a rising edge pre-emphasis circuit and a falling edge pre-emphasis circuit. Different from the main driver which is always turned on, the rise/fall pre-emphasis circuits only turned on at the edge of logic transition. The short pulses are generated by implementing some delay cells, NAND, and NOR gates.

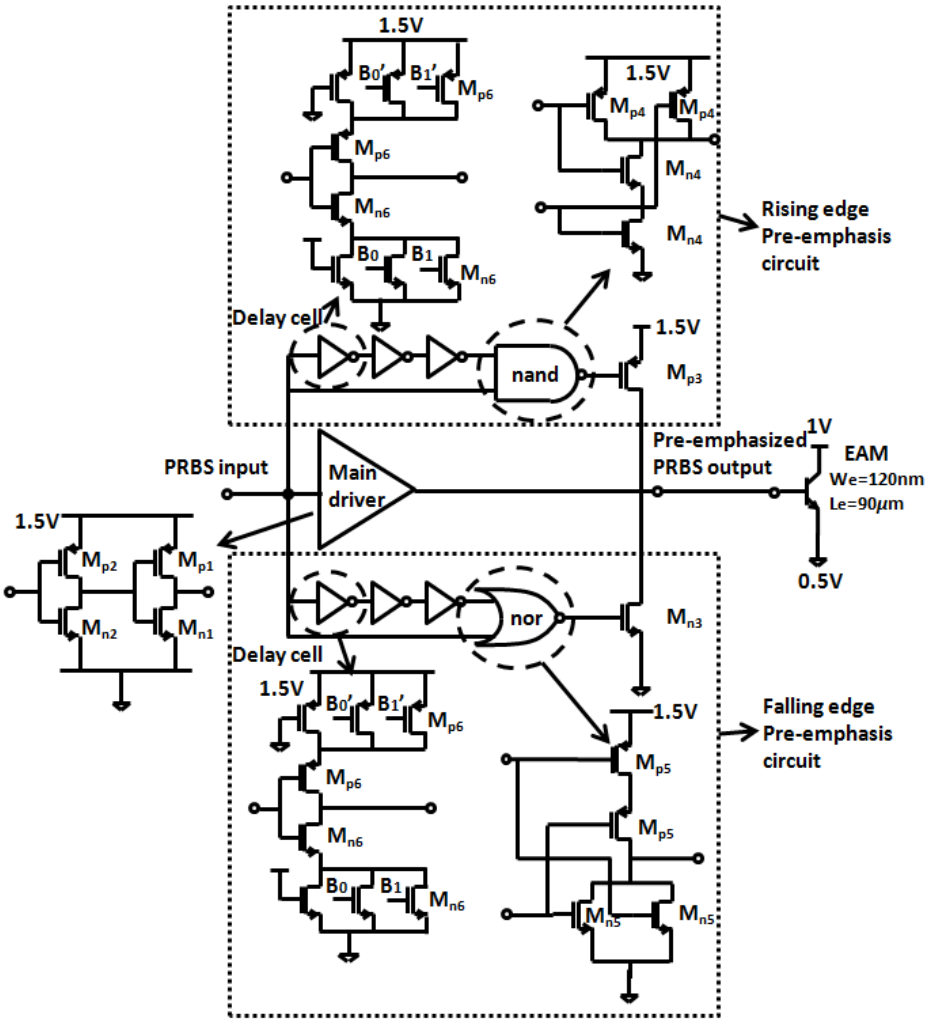


Figure 0.3: Pre-emphasis driver circuit schematic

The load of the pre-emphasis driver is the HBT modulator with 90μm emitter length and 120nm emitter width. As discussed in chapter 2, the output impedance of the driver circuit R_{on} is critical for driving forward-biased P-N junction. In order to reduce the parasitic resistance R_{on}, the transistor M_{p1} in the main driver is designed with a large gate width of 50μm. In a similar manner transistor M_{n1} is designed with a large 18μm gate width to rapidly sweep charges from the HBT intrinsic region to ground at the 1-to-0 transition. The pre-emphasis circuit further reduces the rising and falling transition times. Transistor M_{p3} controls the rising edge peaking, which is activated during the 0-to-1 logic transition. Transistor M_{n3} controls the falling edge peaking, which is activated

during the 1-to-0 logic transition. This peaking duration is set by the total delay of the three identical, cascaded delay cells.

CMOS invertor can be easily implemented as a delay cell with the delay time designed by sizing the PMOS and NMOS. In order to preserve the correct logic the number of delay cell has to be odd. And the total delay should not be more than one bit period otherwise it will cause logic mistake of the next bit. The minimum delay of a signal stage CMOS invertor is determined by the R_{on} and V_{DD}, which both directly relating to the process node and usually the process with smaller feature size has shorter delay. The delay of each delay cell can be set by control bits B_1 and B_0. By turning on a combination of parallel transistors, the equivalent 'ON' resistance is reduced, resulting in a reduction in cell delay. The control bits yield three different delay setting values: 27ps, 30ps and 38ps. The original and delayed data signal drive a NAND/NOR gate, which generates the pre-emphasis pulse at the gate of M_{p3}/ M_{n3}. The component values and transistor dimensions are summarized in Table 4.1.

Table 0.1: Pre-emphasis driver component values*

M_{p1}	M_{n1}	M_{p2}	M_{n2}	M_{p3}	M_{n3}
W=50μm	W=18μm	W=18μm	W=6μm	W=50μm	W=18μm
M_{p4}	M_{n4}	M_{p5}	M_{n5}	M_{p6}	M_{n6}
W=18μm	W=12μm	W=36μm	W=6μm	W=15μm	W=5μm

*the gate length are all 120nm

The design flow of the driver circuit is from the load to the input stage, or from the right to the left. Because following stage is the load for its preceding stage, the size of each stage is tapered from the load to the input stage. In order to switch the load HBT fast the driver should have big size which has higher driving ability. However, it is at the cost of power consumption which is a major consideration of this design. Thus the compromise should be made between power and speed, and circuit should be fine tuned to reach both targets.

4.3 Pre-driver

The pre-driver stage is applied between the PRBS generator and pre-emphasis driver in order to provide CML to CMOS logic transition. As shown in Figure 4.4, the pre-driver consists of three CML differential amplifiers with its output AC coupled into a cascade of CMOS inverters.

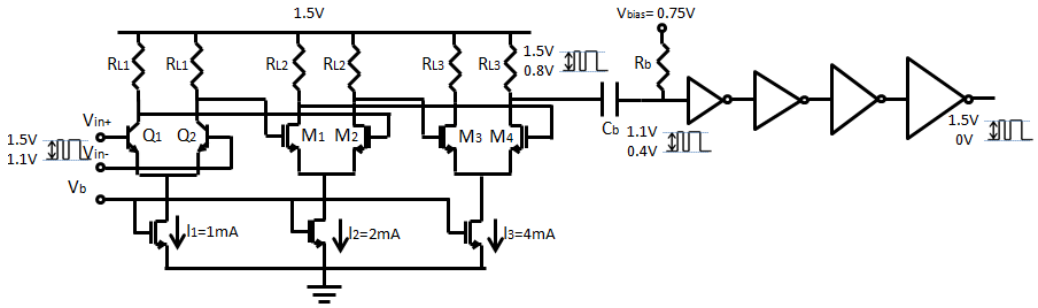


Figure 0.4: Pre-driver circuit

The first differential amplifier utilizes bipolar transistors Q_1 and Q_2, which provide higher transconductance than FET transistors resulting in a relatively smaller load capacitance to the PRBS generator circuit for a given bias current. The 400mV output swing of the differential amplifier is determined by the product of tail current I_1 and the load resistance R_{L1}. Thus, the first stage works like a buffer with unity gain while possessing higher driving capability to the next stage. The second and the third stages utilize FET input transistors to prevent the input transistors being driven into the linear region with a 1.5V power supply. After the third stage differential amplifier the output swing is increased to 700mV.

A cascade of CMOS inverters with increasing size are used to amplify the voltage swing from 700mV to rail-to-rail swing. The threshold of the CMOS inverter chain is designed as half of the power supply voltage. The output signal from the CML differential amplifiers is AC coupled by a high Q metal-insulator-metal (MIM) capacitor, C_b, and level-shifted by biasing a parallel resistor R_b. The value of C_b and R_b are selected to be 5.6pF and 10KΩ respectively with f_{-3dB} as low as 2.8MHz to accommodate the wideband PRBS signal. The component values and transistor dimensions are summarized in Table 4.2.

Table 0.2: Pre-driver component values

Q_1/Q_2	M_1/M_2	M_3/M_4	R_{L1}/R_{L2}	R_{L3}	R_b	C_b
W=120nm L=1.6μm	W=18μm L=120nm	W=36μm L=120nm	0.4KΩ	175Ω	10KΩ	5.6pF

4.4 2^7-1 pseudo-random bit stream (PRBS) generator

To provide a cost-effective means for reliable testing and verification of the modulator and the optical link, a 2^7-1 full rate PRBS generator is designed and monolithically integrated into this transmitter. The block diagram of the PRBS generator circuit is shown in Figure 4.5. One of the seven D-flip-flop (DFF)s is designed with set function to avoid the all zero state.

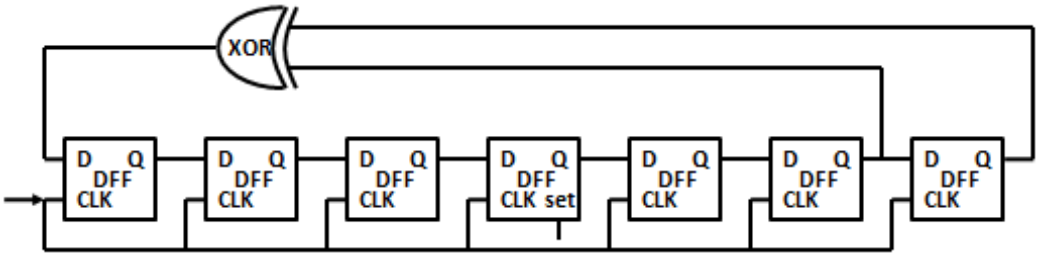


Figure 0.5: 2^7-1 PRBS generator circuit

The traditional CML circuit design is usually based on the current density at peak transition frequency (f_T) to realize the best speed performance. The empirical value of peak f_T current density for MOSFET is approximately 0.3mA/μm. However, according to Figure 4.6, the reducing of current density by 80% to 0.06mA/μm only reduces f_T by 30%, resulting in a substantial power savings. The deeply forward-biased HBT device that forms the backbone structure of the modulator device limits the overall transmitter bandwidth, and therefore, a 30% reduction of DFF speed has minimal effect on the overall optical transmitter circuit performance.

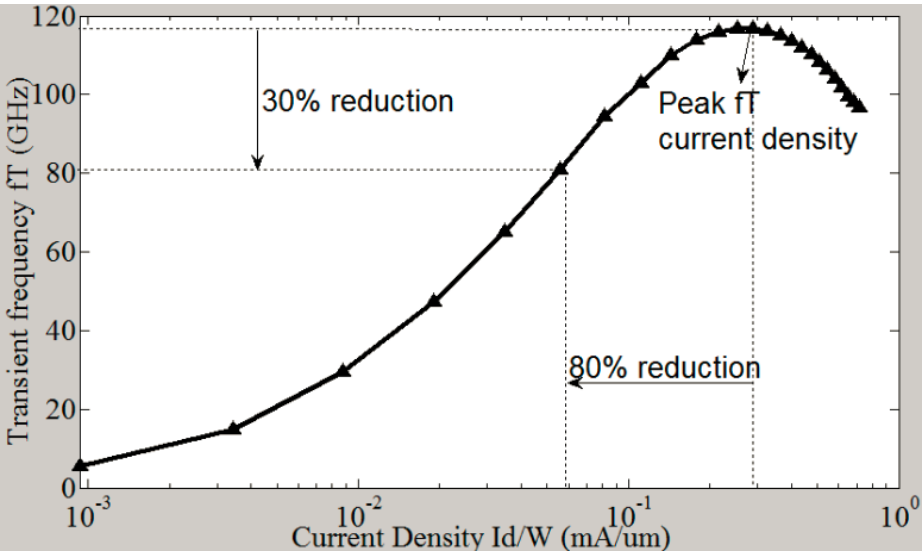


Figure 0.6: Trade-off between current density and f_T of a MOSFET (W=3.2μm, L=120nm) in the 130nm BiCMOS process

The CML D-latch topology is shown in Figure 4.7. Traditional latch designs utilize BJT devices for input transistors M_1 and M_2 to lower the required voltage swing [84][85]. The topology implemented in this work uses MOS transistors, which reduces the voltage drop on the input transistors by 0.2V in a 130nm BiCMOS process. This is very important for power efficiency because the supply voltage is reduced accordingly with the same tail current. Given the bandwidth limitation introduced by the modulator, a series-peaking inductor is not required to boost the speed and conserves die area considerably compared to the D-latch with inductor peaking.

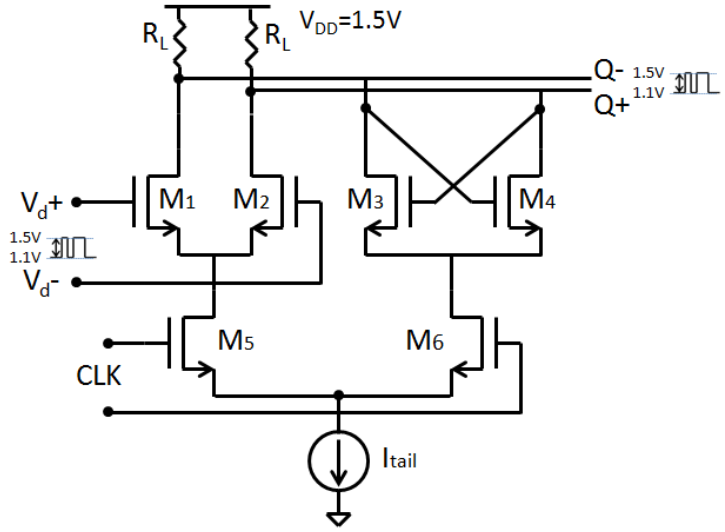


Figure 0.7: CML low-power D-latch

The D-latch tail current is set to 400μA, which results in a total current of 6mA for the 2^7-1 PRBS generator. To be specific, seven master-slave DFF circuits consume 5.6mA and the XOR gate consumes 400μA. The load resistor R_L is selected to enable the latch output voltage to drive the next stage and fully switch the 400μA tail current. A value of R_L = 1KΩ corresponds to an output voltage swing of 400mV. The 400mV output voltage swing is ideal from another two perspectives. Firstly, as the swing will be finally increased to 1.5V rail to rail by CML/CMOS hybrid logic pre-driver stage, the larger voltage swing saves the number of CML stages in the pre-driver, which further minimizes the overall power consumption of the optical transmitter. Secondly, a voltage swing larger than 400mV will push transistors M_1, M_2 or M_5 into the triode region because of the low threshold voltage of the NMOS device (V_{th}~400mV) in the process, which is not desired. After the voltage swing is selected, transistors M_1, M_2, M_5, M_6 are designed with smallest gate width (3.2μm) to minimize the parasitic capacitance while also enabling full switching of the tail current with a 400mV voltage swing at the gate. Furthermore, to minimize parasitic capacitance, the cross-coupled regenerative pair M_3/M_4 is sized with small gate widths equivalent to M_1/M_2. As a result, $g_{m3,4}R_L$ is still larger than unity as calculated by equation (4.1) which guarantees proper operation of the regenerative pair.

$$g_{m3,4} * R_L = \frac{2*I_D}{V_{gs}-V_{th}} * R_L \quad (4.1)$$

Based on the design values, the actual current density J_{MOS} is 200μA/3.2μm=0.06mA/μm. Thus, an 80% power saving is achieved. The component values and transistor dimensions are summarized in Table 4.3.

Table 0.3: CML latch component values

M_1/M_2	M_3/M_4	M_5/M_6	R_L	I_{tail}
W=3.2μm	W=3.2μm	W=3.2μm	1KΩ	400μA

It should be noted that in order to minimize the parasitic brought by layout routings for less discrepancy between schematic and after the physical layout results, the floorplan needs to be carefully designed. Figure 4.8 shows the floorplan of the CML latch. As it depicted, the routings for signal path are kept very narrow width which is just 50% over the calculated width without electromigration issue. The transistors are very close to each other and symmetrically floorplanned.

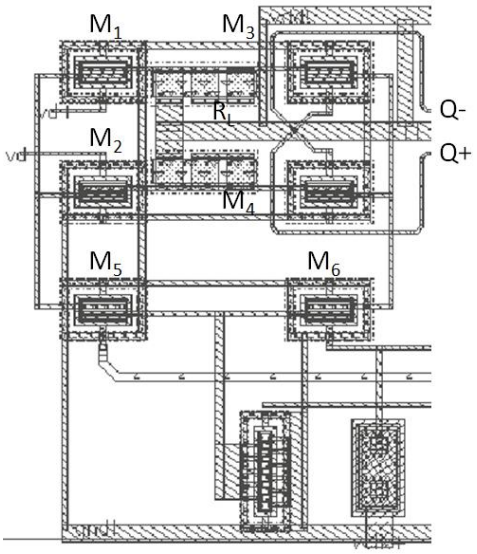


Figure 0.8: floorplan of CML latch

Figure 4.9 shows the post-simulation result of the CML latch. Here V_d+ is a 10Gbps PRBS signal, *clk*+ is a 10GHz clock signal and *Q*+ is the output signal of latch. From the waveform it can be seen that the latch works nicely at 10GHz. Take one clock period as an example, at location ① the latch transits from logic zero to one because the clock signal detects the input data transition from logic zero to one. Thus, the voltage level increase from 1.1V(logic zero) to 1.45V(logic one) when clock is at level of 1.5V(logic one). At the second half the clock period, although clock is at level of 1.1V(logic zero) which turns off transistor M_5, the M_6 will be turned on and regenerative cell will help to keep amplify the output signal to 1.5V as location ② shows.

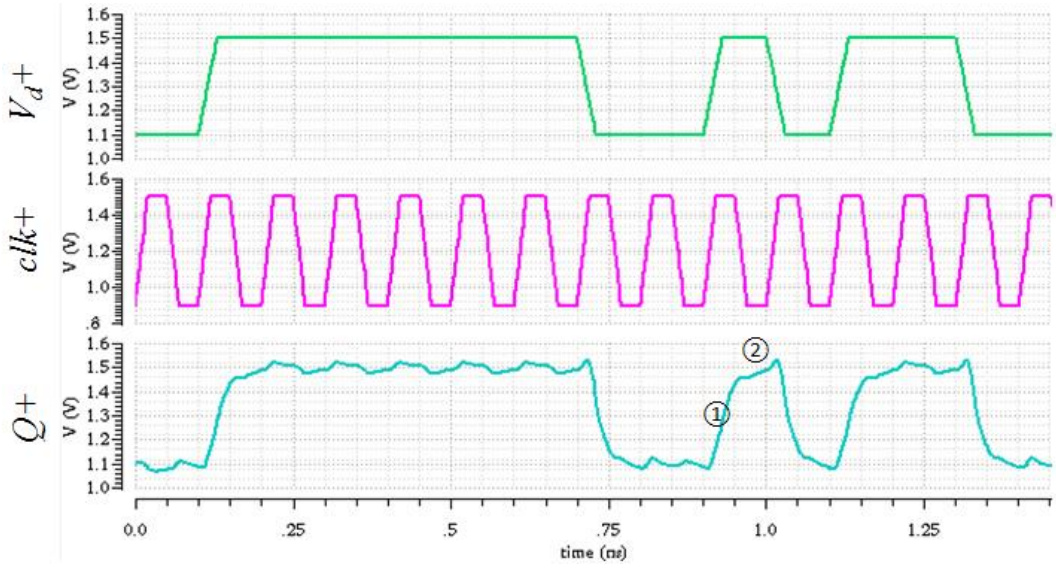


Figure 0.9: post layout transient simulation results of CML latch

Figure 4.10 shows the master-slave DFF based on this latch. The power consumption of this DFF is only 1.2mW at 10Gbps data rate.

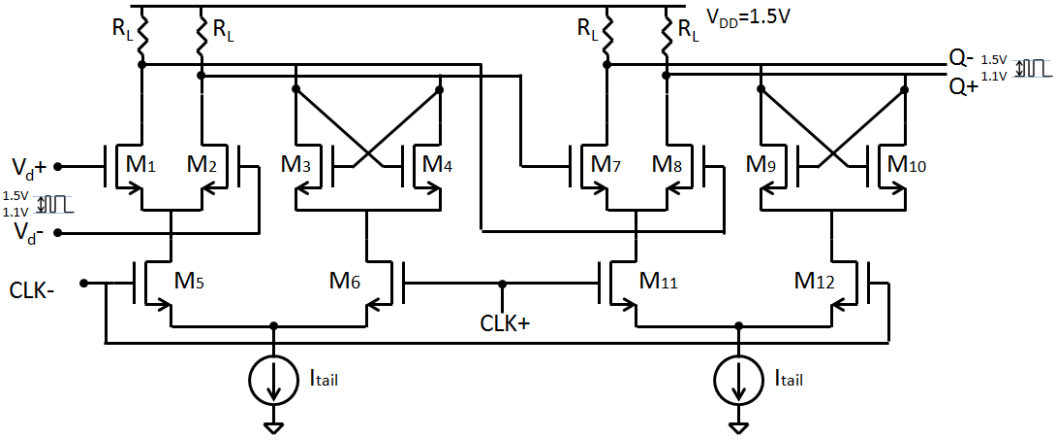


Figure 0.10: Master-slave DFF

As Figure 4.5 shows, one of the seven DFFs needs to have the function to set to logic 'one' in order to avoid all zero state. Figure 4.11 shows the schematic of the unique DFF with SET function. In the master latch, one more stack of transistors (M_7 and M_8) are added which are controlled by SET signal. When SET is logic 'one', the Q+ will be set to logic 'one' no matter the logic of incoming data is; and when SET is logic 'zero', the DFF will become a regular DFF as Figure 4.11.

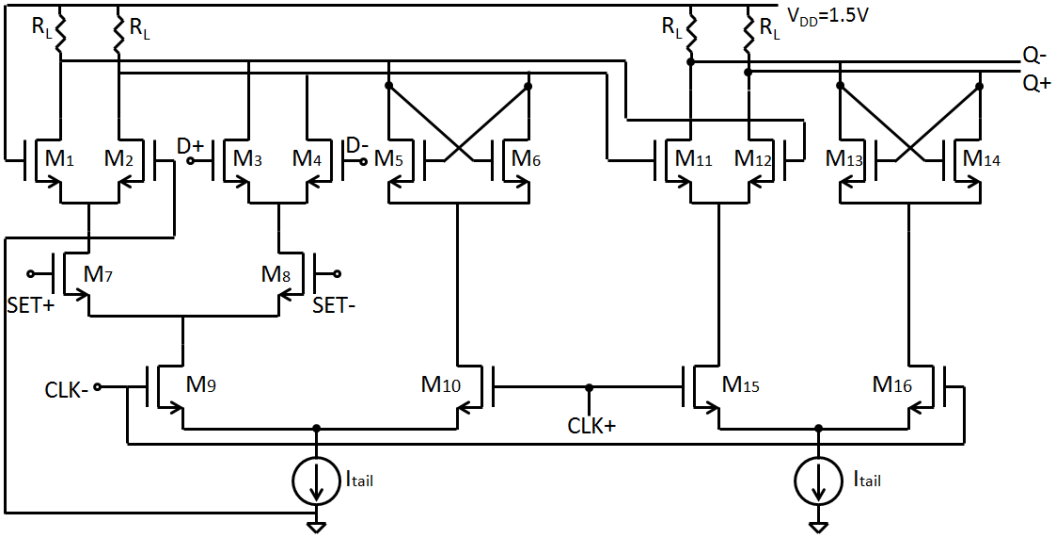


Figure 0.11: DFF with SET function circuit

The component values and transistor dimensions are summarized in Table 4.4.

Table 0.4: DFF with SET function component values

M_1/M_2	M_3/M_4	M_5/M_6	M_7/M_8	M_9/M_{10}
W=3.2μm	W=3.2μm	W=3.2μm	W=9.6μm	W=3.2μm
M_{11}/M_{12}	M_{13}/M_{14}	M_{15}/M_{16}	R_L	I_{tail}
W=3.2μm	W=3.2μm	W=3.2μm	1KΩ	400μA

Function simulation is shown in Figure 4.12. At location ① the rising edge of *clk*+ makes the output *Q*+ follows the input data V_d+ because *SET*+ is not valid at this time. At location ② the *Q*+ is not following V_d+ anymore because *SET*+ now is logic "one" which forces the *Q*+ to logic "one". This forced output logic is kept till last *clk*+ rising edge at which *SET*+ is still valid (location ③). At the next *clk*+ rising edge because *SET*+ is not valid anymore, the output *Q*+ follows the input data V_d+ again. As seen from Figure 4.12 the DFF with SET function can work nicely at 10GHz. The power consumption of this DFF is only 1.2mW.

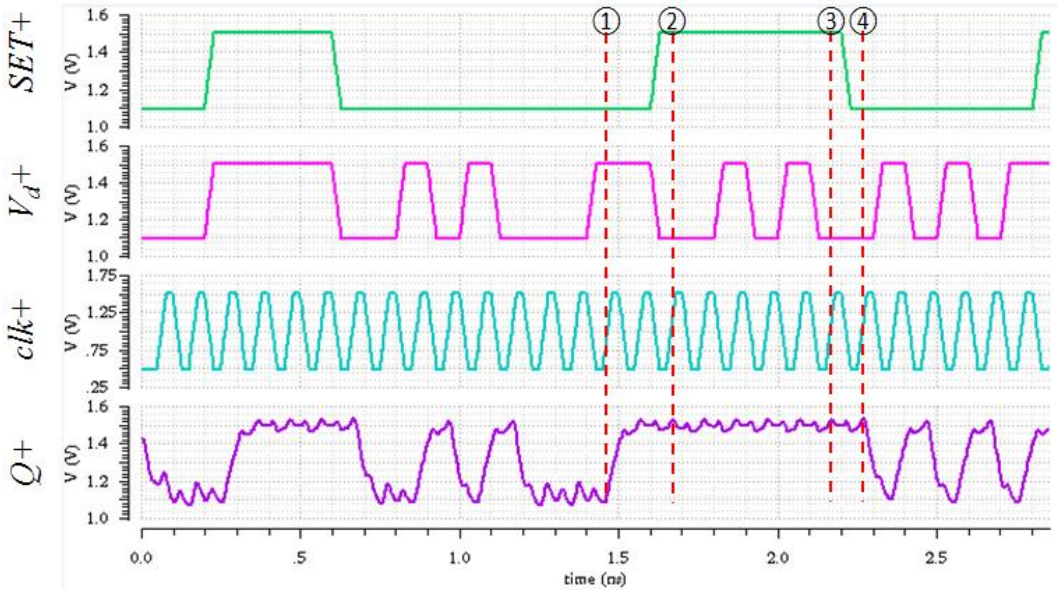


Figure 0.12: simulation results of DFF with SET function

An Exclusive-or (XOR) gate is required to realize the PRBS signal generation as Figure 4.5 shows. The XOR gate should have the feature of: same input and output signal amplitude; fast switching speed; and short gate delay. The schematic of the XOR gate is shown in Figure 4.13. As it can be seen that the circuit is a combinational circuit without timing from clock signal, which helps to reduce the gate delay.

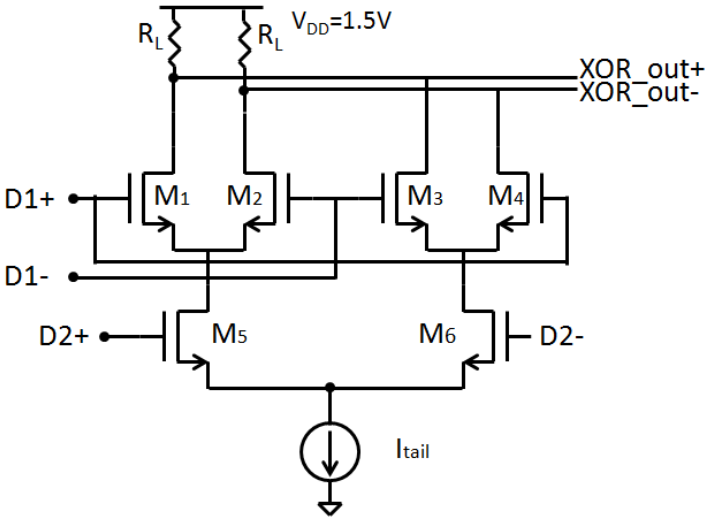


Figure 0.13: XOR gate circuit

The component values and transistor dimensions are summarized in Table 4.5. As it shows, the size of M_5/M_6 is a little larger which is because its gate signal only has the swing of 400mV, different from the *clk+* signal in Figure 4.7 which has 600mV swing. Thus, the size of transistors are set larger to compensate the gain. However, it should be noted that the size of M_5/M_6 should not be considerably increased because they behave as load for one of the DFFs.

Table 0.5: CML latch component values

M_1/M_2	M_3/M_4	M_5/M_6	R_L	I_{tail}
W=3.2μm	W=3.2μm	W=4.0μm	1KΩ	400μA

The layout of the PRBS generator should minimize the parasitic in order to achieve the expected speed performance. Due to the 2^7-1 PRBS has eight components with seven of them triggered by the same clock signal, the floorplan is especially important to shorten the routing between the components. As shown in Figure 4.14, the seven DFFs are not placed in a line but folded at DFF4/DFF5. Thus, the output of XOR can go back to DFF1 with very short routing. Also, the folded layout could make the clock distribution routing much shorter. Here the differential clock distribution is implemented using the two toppest metal layers which have the lowest sheet resistance. To handle the current the width of the clock distribution should not be very narrow, however, too wide will considerably add parasitic capacitor which is also not desirable. Moreover, the three double layer power and ground stripes make good connection to the power plane. With the compact layout design, the area of the PRBS generator is only about 300μm×130μm.

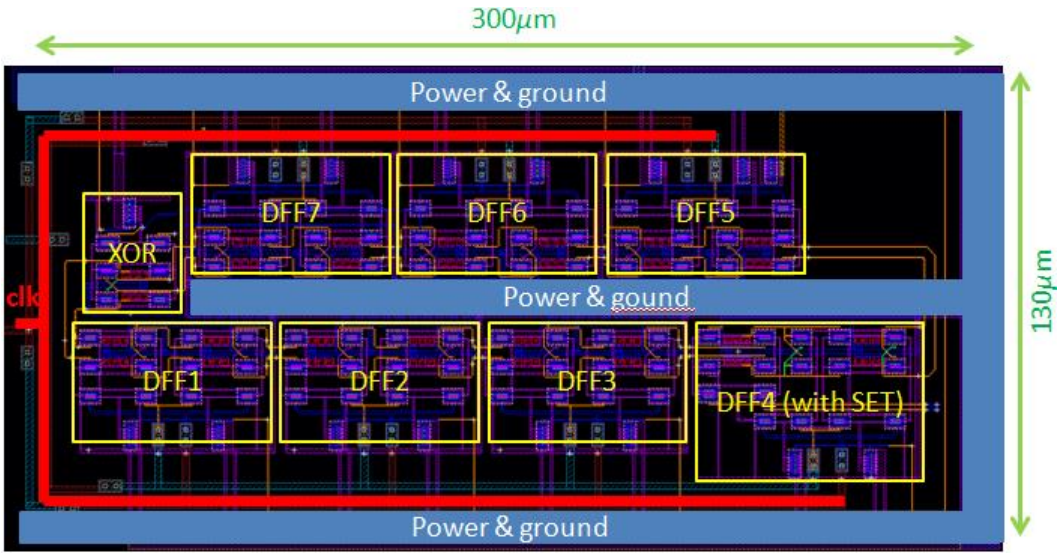


Figure 0.14: the layout of PRBS generator

4.5 Chip fabrication and floorplan

The transmitter driver chip is fabricated in BiCMOS process. Figure 4.15

illustrates the microphotograph of the chip. The total die area is 1920μm×1650μm. The core of PRBS generator occupies only 300μm×130μm. The pre-driver stage occupies an area of 270μm×80μm, while the core circuit of the pre-emphasis driver occupies 200μm×110μm. The total area of the pre-emphasis driver including the 600pF MIM decoupling capacitor is approximately 630μm×1230μm.

The differential clock signal is supplied from the GSGSG pads at the left side. The pre-emphasized output signal goes to the GSG pads at the right side. For characterization purpose, the PRBS signal is monitored through the SGS pads at the bottom. The rest of pads at the bottom and all the pads on the top are DC pads.

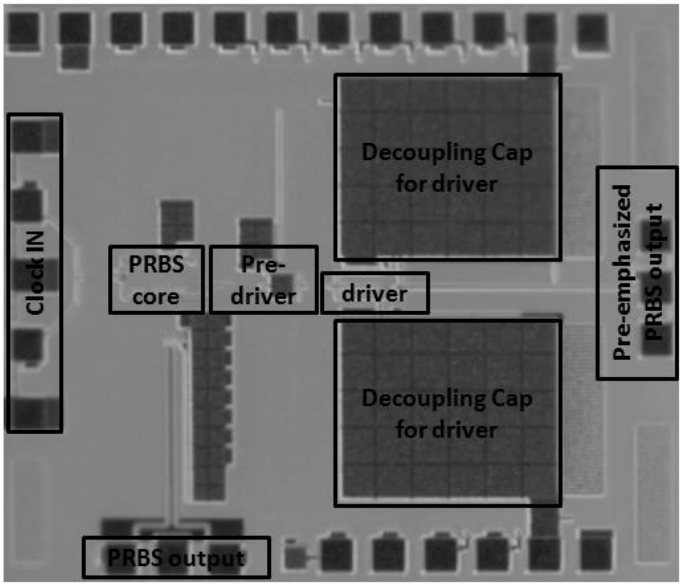


Figure 0.15: Chip microphotograph

4.6 Measurement results

4.6.1 RF PCB testbench

The first testbench was built on a FR-4 PCB with the chip wirebonded to a QFN-52 package. Figure 4.16 shows the block diagram of the testbench. A 50Ω wideband SMD balun (Minicircuit TCM1-83X) is used to provide single-ended to differential-ended conversion. Three 0.1μF ultra-wide band (up to 20GHz) DC blocking capacitor (ATC550L) are used in the differential input and PRBS signal

output. The clock signal is supplied from Agilent E8247C signal generator and the output signals are monitored by Agilent 54855A real-time oscilloscope with 6GHz bandwidth.

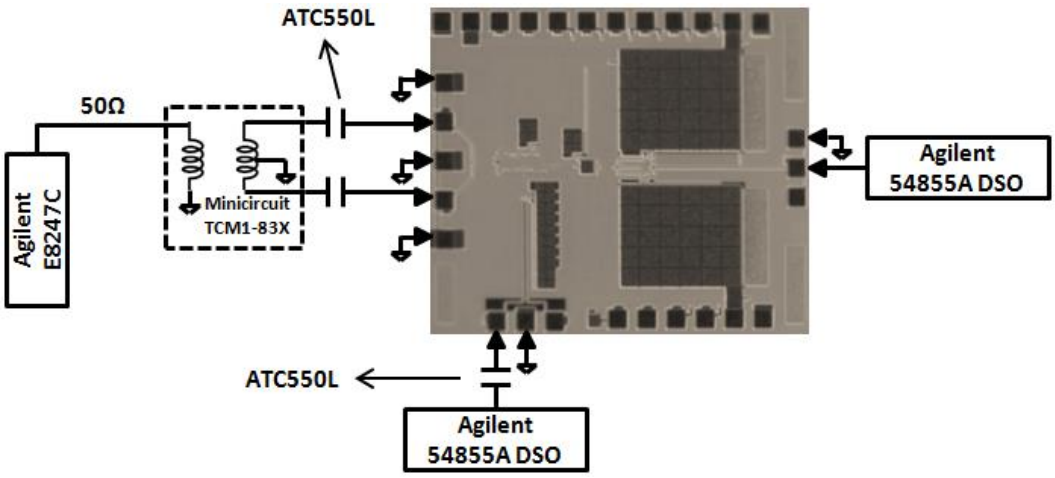


Figure 0.16: PCB testbench block diagram

The picture of PCB testbench is shown in Figure 4.17. The PRBS SET bit is controlled by an ON-MOM pushbutton switch which connects when it's pushed and disconnects when it's released. The pre-emphasis strength bits are controlled by two ON-ON slide switches. Decoupling capacitors are sitting very close to the chip and DC-blocking capacitors are shown in the figure as well.

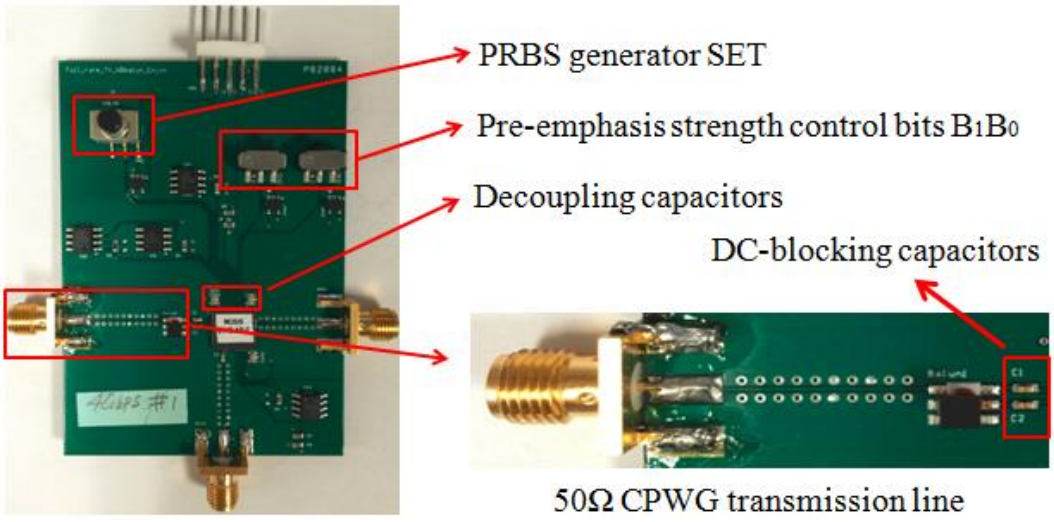


Figure 0.17: PCB testbench picture

50Ω CPWG transmission lines are designed for the input RF and two output RF signals. Figure 4.18 shows the stackup of a four layer (63.5mil thickness) FR-4 PCB. The thickness of each layer is denoted. The top metal is used for signal line routing. In order to get reasonable narrow signal line width, according to 50Ω CPWG model, the ground plane needs to be implemented in layer Mid-1, not bottom layer metal.

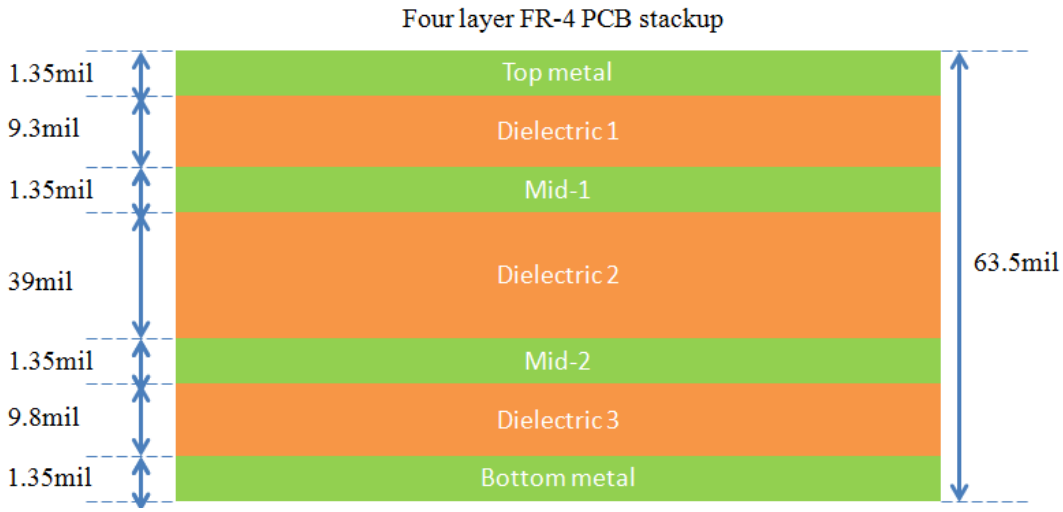


Figure 0.18: Four layer FR-4 PCB stackup

Using ADS transmission line design tool Linecalc, the signal line width (W) and signal to ground plane lateral spacing (G) are designed. As shown in Figure 4.19, by providing PCB substrate information the W and G can be designed to get a 50Ω CPWG transmission line. Here, the designed CPWG has the characteristic impedance of 55Ω.

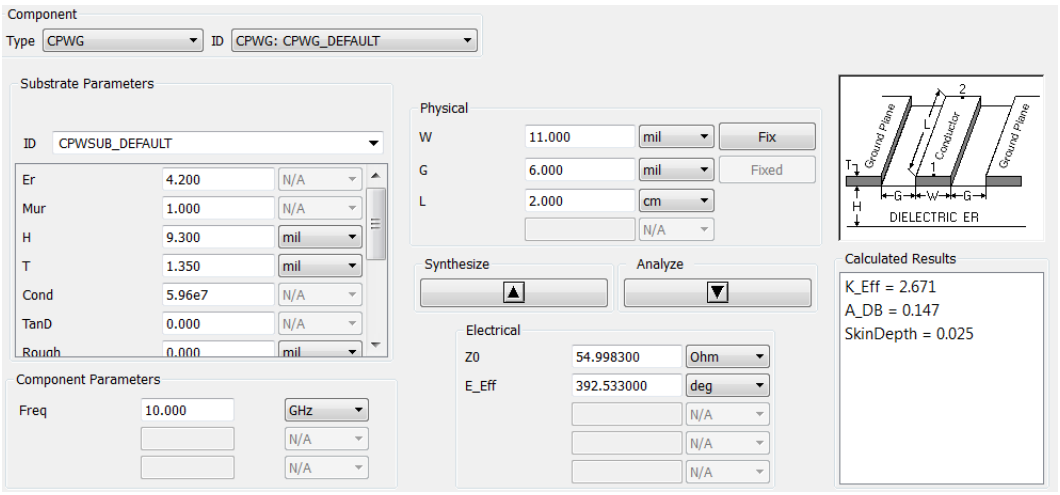
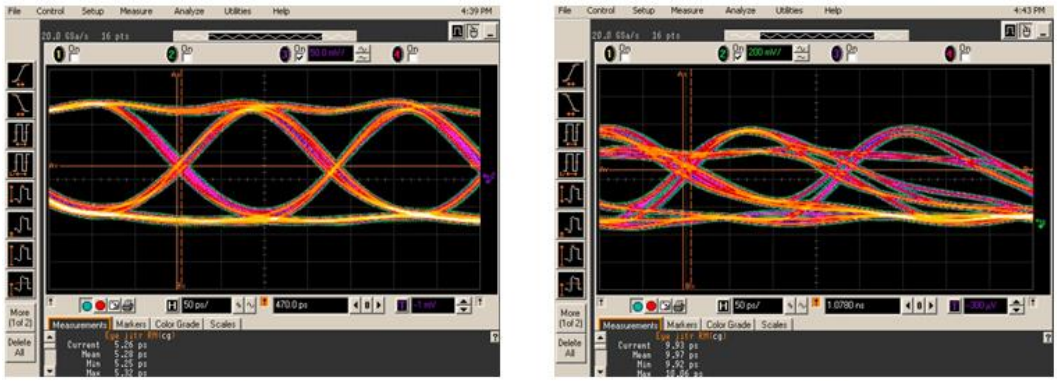


Figure 0.19: CPWG design using ADS Linecalc

The 5.5Gbps eye diagram is measured and shown in Figure 4.20. Figure 4.20(a) shows the 2^7-1 PRBS signal output with 200mV swing and 5.26ps rms jitter. Figure 4.20(b) shows the pre-emphasized PRBS signal with peaking clearly shown. The considerable jitter and rise/fall time is due to the parasitic brought by long bonding wires.



(a) (b)

Figure 0.20: 5.5Gbps Eye diagram of output signals

In order to characterize the chip performance more accurately without the package parasitic, a chip-on-board assembly is implemented as shown in Figure 4.21. Without package, the PCB footprint of the chip is re-designed to be more compact. Due to the soldering pad on PCB is usually nickel which is not

wirebondable, the new PCB is designed and fabricated with Soft-bondable-gold soldering pads. From Figure 4.21 it can be seen that the gold wirebond is bonded nicely on to the bondpads on PCB.

One thing needs to be pointed that, the chip in the last experiment is a big 4mm*4mm chip with three designs on it. In order to reduce the bonding wire length, the chip is diced into three individual pieces. Thus, the small chip size helps to reduce the bonding wire length in further.

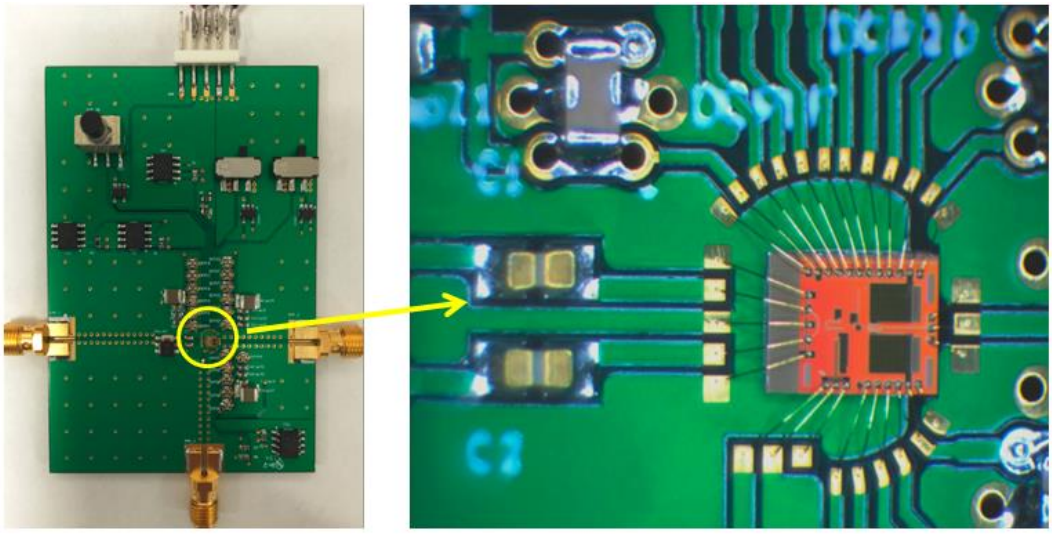
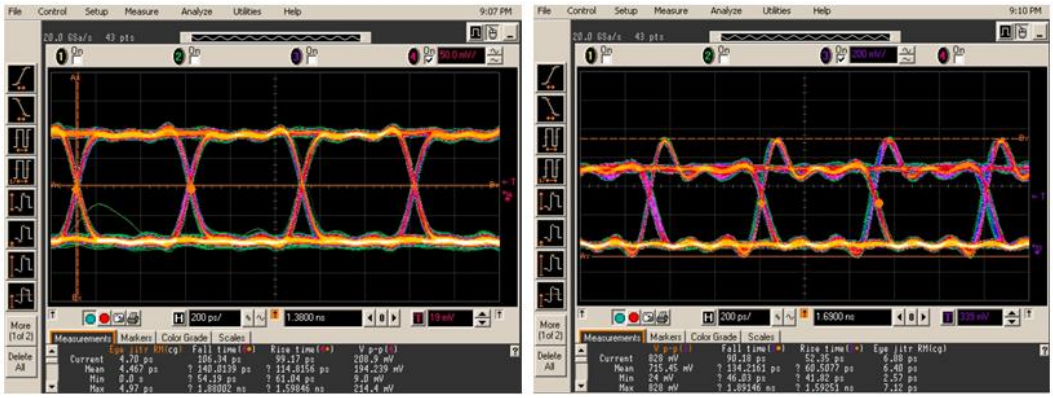


Figure 0.21: chip-on-board assembly

Figure 4.22(a) shows the measured eye diagram of PRBS signal and Figure 4.22(b) shows the pre-emphasized PRBS signal. Compared to Figure 4.20, the new eye diagrams are much clearer. Smaller jitter and rise/fall time can be easily seen.



(a) (b)

Figure 0.22: 2Gbps Eye diagram of output signals

By control the strength of pre-emphasis, the peaking height and duration are different as shown in Figure 4.23. The highest tested data rate from this board is around 2Gbps, which is even much lower than the packaged chip testbench. After careful analysis and debugging, the problem is included from the chip dicing. Because there are three designs fabricated on a same die which are not separated to each other by using guard-ring. Thus, the dicing may cause some minor defects to the AC performance of the circuits according to the foundry.

Figure 0.23: Control the pre-emphasis strength

4.6.2 Probe station testbench

In order to characterize the real chip performance without the effects of bonding wires, board traces, and package parasitic, etc, a probe station testbench is built to do the on-chip testing. The block diagram of the testbench is shown in Figure 4.24. Single-ended clock signal is supplied from the signal generator (Agilent E8247C) and converted into a differential signal by a wideband balun (Hyperlabs HL9402) with SMA connector. The differential clock signal is supplied to the chip by an RF probe (Cascade 40GHz GSGSG). Output signals from the PRBS generator and driver are measured using RF probes (GGB 40GHz GS). DC pads are wire-bonded to an open cavity QFN-52 package and mounted on a FR4 printed circuit board.

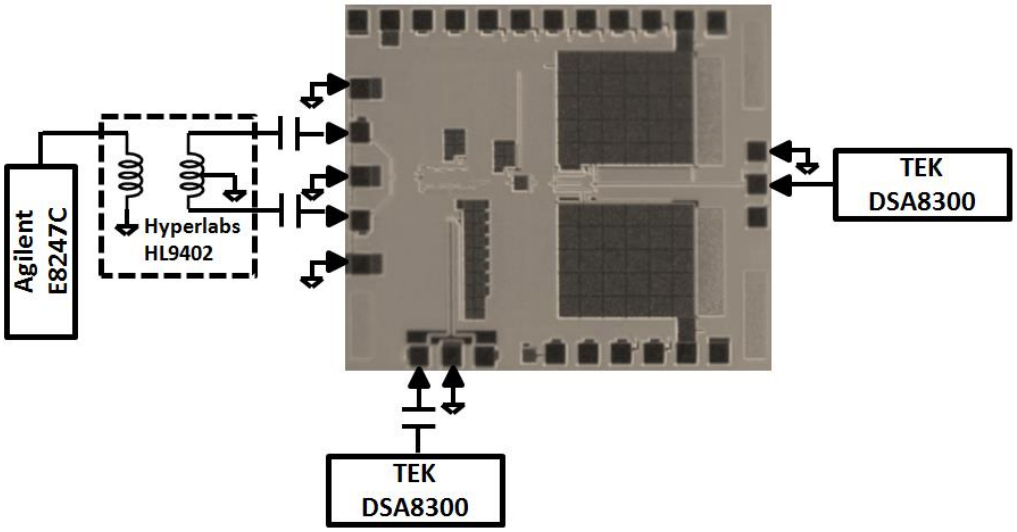


Figure 0.24: Probe station testbench block diagram

The picture of the probe station testbench is shown in Figure 4.25. There are two straight RF probe positioners holding RF probes for input differential clock signal and output pre-emphasized PRBS signal, and an L-type probe positioner is used for holding RF probe for PRBS output signal.

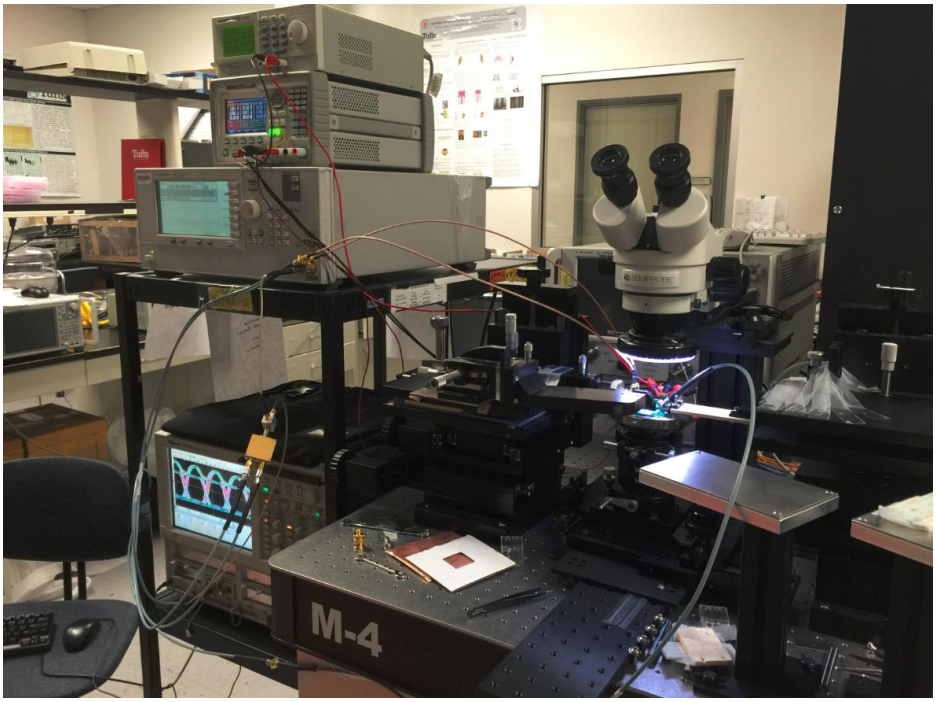
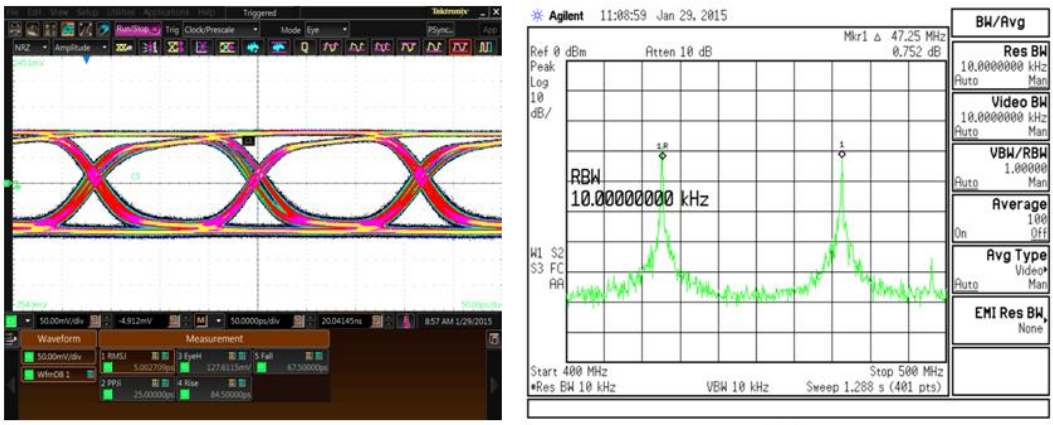


Figure 0.25: Probe station testbench picture

The eye diagram is tested by using Tektronix DSA8300 sampling scope with 20GHz sampling module. Figure 4.26(a) shows 6Gbps eye diagram of the PRBS signal with 5ps root mean square (RMS) jitter. Figure 4.26(b) shows the zoomed spectrum of the 2^7-1 PRBS signal with a tone spacing of 47.25MHz = 6Gbps/127bits indicating the correct pattern is achieved.



(a) (b)

Figure 0.26: 6Gbps PRBS signal (a) eye diagram and (b) spectrum

The eye diagram of the driver output with 50Ω load and with strong emphasis (B_1B_0=11) is shown in Figure 4.27(a). The spectrum is measured by a spectrum analyzer (Agilent E4408B). The 47MHz tone spacing shown in Figure 4.27(b) equals the data rate (6Gbps) divided by the pattern length (127), indicating that the 127-bit PRBS signal pattern is correctly achieved.

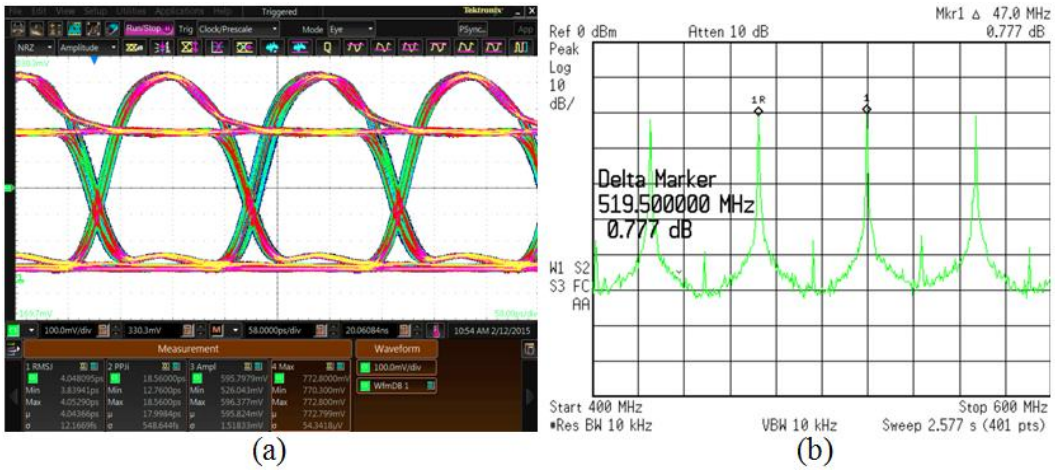


Figure 0.27: 6Gbps pre-emphasis (strong) PRBS signal (a) eye diagram and (b) spectrum

The eye diagram of the driver output with 50Ω load and with weak pre-emphasis (B_1B_0=00) and strong emphasis (B_1B_0=11) are overlapped and shown in Figure 4.28, highlighting the pre-emphasis peaking signal. With pre-emphasis the amplitude is increased from 575mV (nominal) to 670mV (weak peaking) and to 750mV (strong peaking). The peaking duration is 80ps and 115ps, respectively.

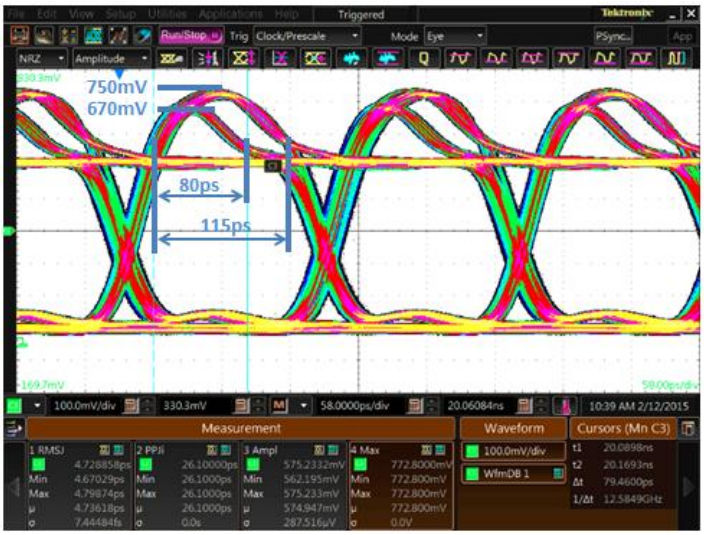


Figure 0.28: 6Gbps pre-emphasis (strong and weak) PRBS signal

4.7 Results with modulator load

To demonstrate the expected performance of the driver circuit with the HBT-based modulator, the circuit is simulated using the electrical load model presented in Figure 4.2(b). The simulated eye diagram at 6Gbps is shown in Figure 4.29. As shown, the 0.95V forward-bias satisfies the design specification which will guarantee the modulator extinction ratio of 5dB. It is shown that the -0.5V voltage for the base-to-emitter junction shortened the falling edge.

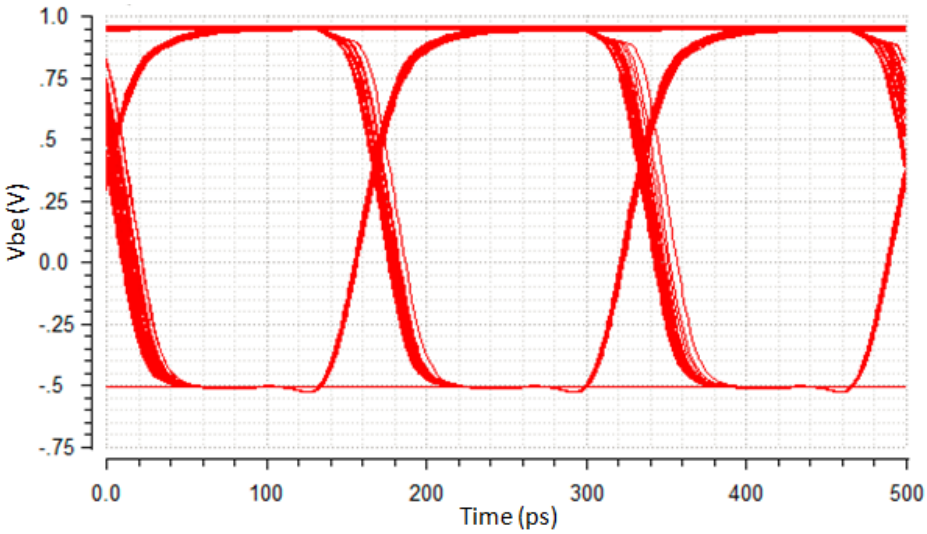


Figure 0.29: 6Gbps driver output signal at HBT modulator load

4.8 Performance comparison

The designed transmitter circuit is compared to other similar works from the perspectives such as speed, power consumption, etc. Power efficiency is a specification absorbing the speed and power consumption information. Thus, it is the main specification to be compared. Firstly, the PRBS generator is took out from transmitter and compared separately. For fair design comparison, a figure of merit (FOM) is introduced in equation (4.2). Here R_{bit} represents the highest tested bit rate.

$$FOM = \frac{Power}{Log_2(Length) * R_{bit}} \tag{4.2}$$

The FOM of this PRBS generator and other similar works are summarized in Table 4.6. The total power consumption of 42.75mW accounts for clock buffer (18mW), PRBS generator core (9mW), and 50Ω output buffer (15.75mW). By comparison this work has the highest FOM among the state-of-art low power PRBS generator designs, which is mainly due to the ultra-low power CML latch design. It should be noted that if the power consumption of the output buffer is excluded, which is applied only for the reason of characterization, the FOM advantage of this work compared to other works will drastically increase [86].

Table 0.6: Comparison of state-of-art low power PRBS generators

Specification	This work[86]	[84]	[87]	[88]
Power (mW)	42.75	243	194	393
Data rate (Gbps)	6	23	24	5
Length	2^7-1	2^7-1	2^7-1	2^{31}-1
FOM (pJ/bit)	1.01	1.5	1.15	2.53
Process	130nm BiCMOS	130nm BiCMOS	130nm BiCMOS	180nm CMOS

Secondly, the complete transmitter circuit is compared. The total power consumption of this optical transmitter at the data rate of 6Gbps is 44.5mW, including the PRBS generator (27mW), pre-driver (10.5mW) and pre-emphasis driver (7mW). The FOM given by equation (4.3) is adopted to evaluate the performance of the transmitter driver circuit, which generates FOM = 7.41pJ/b for this work.

$$FOM = \frac{Power}{Data\ rate} \tag{4.3}$$

Table 4.7 [89] summaries the performance comparison to some published carrier injection silicon optical transmitters. Compared to the other types of silicon EA or EO modulator based transmitters, this work is based on a silicon HBT-based EA modulator and is designed by using a cost-effective 130nm BiCMOS process. The results show good speed performance and power efficiency.

Table 0.7: Transmitter performance comparison

Specification	[90]	[91]	[30]	This work[89]
Modulator type	Ring	MZI	MZI	EAM
Data rate (Gbps)	2.5	20	10	6
Power (mW)	3.125	90	51*	44.5
FOM (pJ/bit)	1.23	4.5	5*	7.41
Process	45nm SOI	40nm CMOS	Custom	130nm BiCMOS
PRBS generator	2^{31}-1	2^{31}-1	N/A	2^{7}-1

*exclude the power at driver

It should be noted that by using process with smaller feature size, the speed of transmitter can be boosted while the power consumption can be reduced as the designs in [90][91]. Ring modulator [90] is much more power efficient than interferometer based modulator [91][30] and the carrier injection modulator

presented in this work due to its special resonant mechanism but at the sacrifice of very narrow optical bandwidth and high sensitivity to temperature and process variation.

4.9 Summary

This work presents an ultra-low power optical transmitter module design for a HBT-based carrier injection optical EA modulator. The main features of the transmitter are the low power high speed driver with configurable pre-emphasis and the monolithic integrated PRBS generator. The chip is fabricated using a cost-effective 130nm SiGe BiCMOS process. Measurement results at 50Ω load show the transmitter can work up to 6Gbps with configurable pre-emphasis strength. The FOM of this transmitter module is similar to other similar works while the FOM of PRBS generator has outstanding performance. Moreover, the speed and power consumption of the transmitter can be improved by using more advanced processes.

Chapter 5

300Mbps LED Link with Bandwidth Enhancement by using Pre-emphasis driver

With years of improvement LED is universally used for lighting application and soon or late it will be the dominant replacement for traditional incandescent bulb due to its high power efficiency and being environmentally friendly as well as its high switching speed. At the same time, researchers are using the LED as a media for communication by switching and modulating data onto it. Some companies invented different kinds of "smart bulb", which can be used as a WiFi hotspot to communicate with smart phone besides its basic function of lighting. With the requirement for ever increasing data speed, the LED based link meets bottleneck because its bandwidth rarely exceeds 100MHz, which is due to its large physical size. Micro-LED is an idea which is used to increase the bandwidth by decreasing the size of LED[92], however, it's at the sacrifice of light intensity and high cost.

On the other hand, pre-emphasis is a cost-effective method to boost the LED bandwidth without sacrificing light intensity[65]. There are some other techniques presented in the literature which emphasize on the usefulness of pre-emphasis technique in enhancing the LED bandwidth. In[93] a pulse amplitude modulation technique is applied to a 4 x 4 LED array. The 16-level PAM modulation scheme increases the data transmission rate from 10Mbps to 40Mbps. The other bandwidth enhancements is using time interleaved method[94]. This method not only mitigates the low bandwidth issue of commercially available LEDs, but also provides sufficient light output as well. As described and implemented in details in[94], the interleaved method allows each LED to be ON for 100ns rather than 10ns that would be required for 100Mbps transmission. Post-equalization can be utilized to further enhance the bandwidth and the data

rate of the link. In [95] a post-equalization circuit is used to improve the bandwidth of phosphor white-LEDs by 50 times. In [96] interleaving technique is applied on Expurgated Pulse-Position Modulation (EPPM) to increase the transmission rate of bandwidth-limited white LEDs. There are some attempts going on in the device optimization to increase the bandwidth of LEDs as well. For instance, by an appropriate device design, it has been demonstrated that the green GaN-based LEDs with a mesa diameter of 75μm exhibit the highest 3-dB frequency bandwidth of 463 MHz at 5mA[97]. Upon commercialization of these LEDs, the proposed pre-emphasis technique would be a great fit to be used in plastic optical fiber as well as visible light communication.

This chapter is going to present a red-LED based optical link design. The pre-emphasis driver module discussed in Chapter 4 will be used to drive the LED. It will show that by using the pre-emphasis driver, the optical link which is based on a 70MHz bandwidth red-LED works well at 300Mbps. The BER calculation shows it has been improved at least 10 times compared to the setup with regular driving signal at the data rate of 300Mbps. This chapter is organized as the following: section 5.1 will introduce the LED based data transmission link; section 5.2 will present the LED-module; section 5.3 will discuss the measurement results while section 5.4 will be the summary.

5.1 LED data communication link

The LED data transmission link is built based on IF-E99B red LED from Industrial Fiber Optics which claims 70MHz -3dB bandwidth and 156Mbps data rate[98]. To the authors' best knowledge, this is the fastest LED on the market. A comparison experiment is designed to study the features brought by pre-emphasis transmitter. Figure 5.1 shows the reference setup, which has the transmitter signal from a bit error rate testing (BERT) system with regular PRBS signal. By comparison, Figure 5.2 shows a setup with transmitter signal from pre-emphasis driver module.

Thorlabs optical receiver PDA10A which has 180MHz bandwidth is used

as receiver in this transmission link. Due to its analog output, the difference of the two optical signals can be monitored with good fidelity. The signal from LED is coupled to the receiver by Super Eska^{TM} SH4001 1000μm core plastic fiber with compatible connection to the LED housing and the receiver.

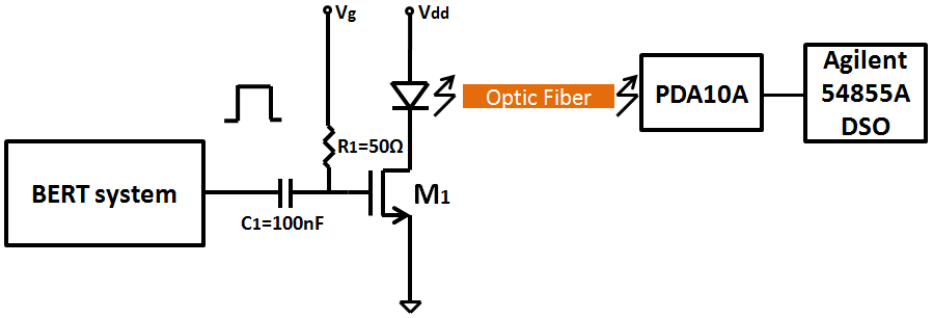


Figure 0.1: Data transmission link with regular transmitter

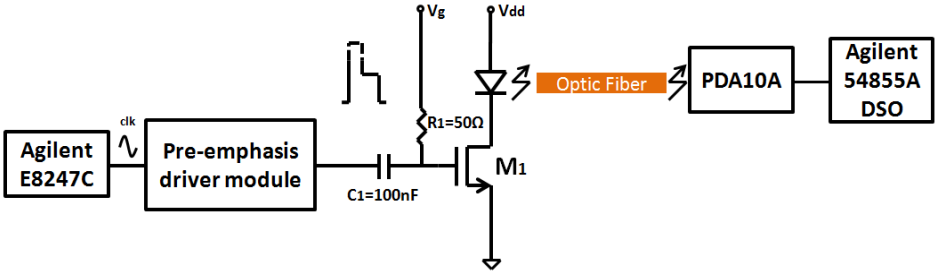


Figure 0.2: Data transmission link with pre-emphasis transmitter

5.2 LED module

The *I-V* curve of the LED is measured by using Keithley 2400 sourcemeter. The results are shown in Figure 5.3. The threshold of this LED is around 1.8V. By biasing the LED with 35mA (2V) instead of 20mA (1.95V) DC current, the LED has smaller small signal resistance which is favorable to its maximum switching speed.

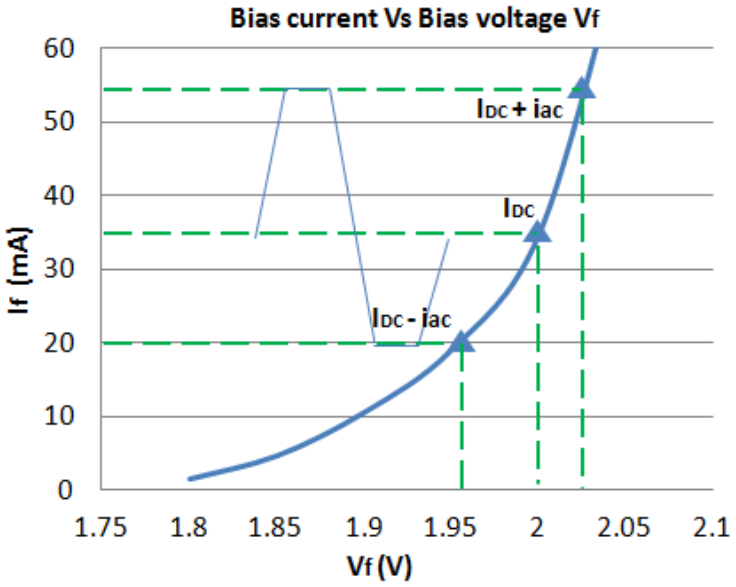


Figure 0.3: I-V curve of LED

The switching of LED is controlled by MOSFET M_1 which is connected to the cathode of LED as shown in Figure 5.4. In order to reduce the extra parasitic brought by it, a 0.5-26.5GHz ultra-high bandwidth MOSFET is implemented[99].

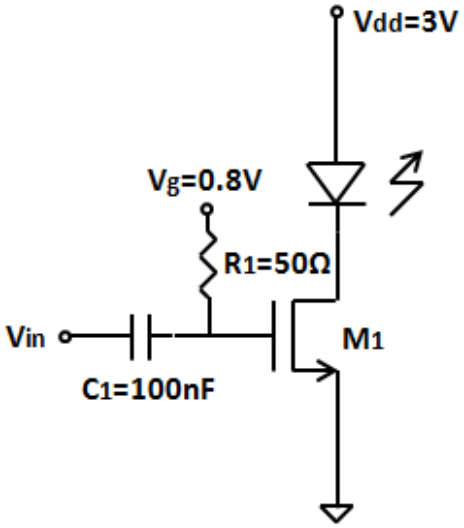


Figure 0.4: LED and switch schematic

The *I-V* curve of the MOSFET is measured and shown in Figure 5.5. The

DC operating point is selected to make 35mA DC current as required by LED, which corresponds to a gate voltage V_g of 0.8V. The current swing $\pm i_{ac}$ is decided by the swing of input voltage V_{in}, which is about 350mV according to the output of pre-emphasis driver at 50Ω load. From Figure 5.5 it can be seen that the V_{in} will generate (20mA-55mA) current swing, which will modulate the LED on and off. In addition, the peaking will be as high as around 600mV for 75ps, which will supply around 90mA instant current to the LED, as expected according to Figure 5.3. This short period of current injection helps to speed up the LED driver by reducing the rise time.

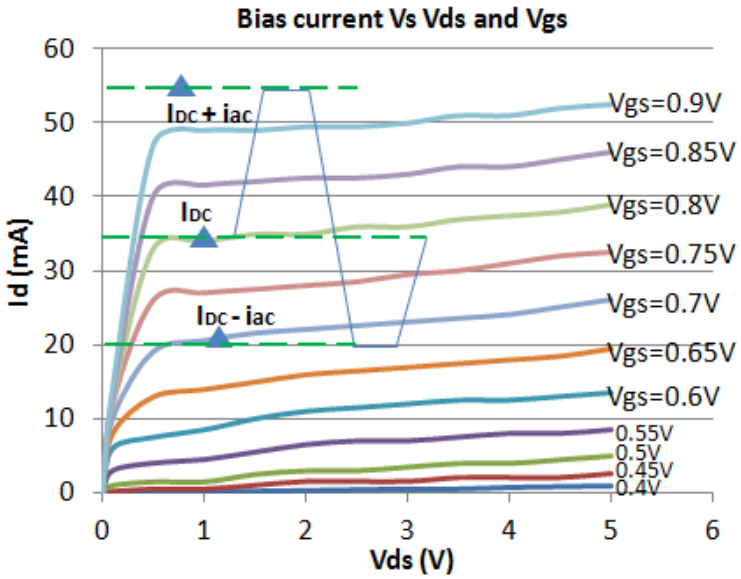


Figure 0.5: I-V curve of MOSEFT switch

According to Figure 5.3, the voltage drop on LED V_f is around 1.95-2.02V, while it is required to have a minimum of 0.7V drop on M_1 in order to keep it working in the saturation region. Thus the V_{dd} is selected to be 3V, which can guarantee the operation of LED and M_1 while save the power consumption. The output of pre-emphasis driver is AC coupled to the gate of M_1 by using an ultra wide band American Technical Ceramic (ATC) 550L capacitor [100] which has 16kHz-40GHz bandwidth and is ideal for PRBS signal. In the meanwhile, an ATC 504L 50Ω RF resistor R_1 is parallel to the gate of M_1. The gate bias voltage is

supplied through R_1 while it provides 50Ω impedance matching to the pre-emphasis driver.

5.3 Testbench and measurement

Two PCBs are fabricated for the pre-emphasis transmitter module. As shown in Figure 5.6, the output of pre-emphasis driver is connected to the LED module by a 50Ω coaxial cable. The light from LED is coupled to the commercial receiver by a plastic fiber. The length of the fiber is about 20cm with negligible attenuation to the light.

In comparison, a BERT system based testbench has the BERT output directly connecting to the LED module. The optical link portion is the same.

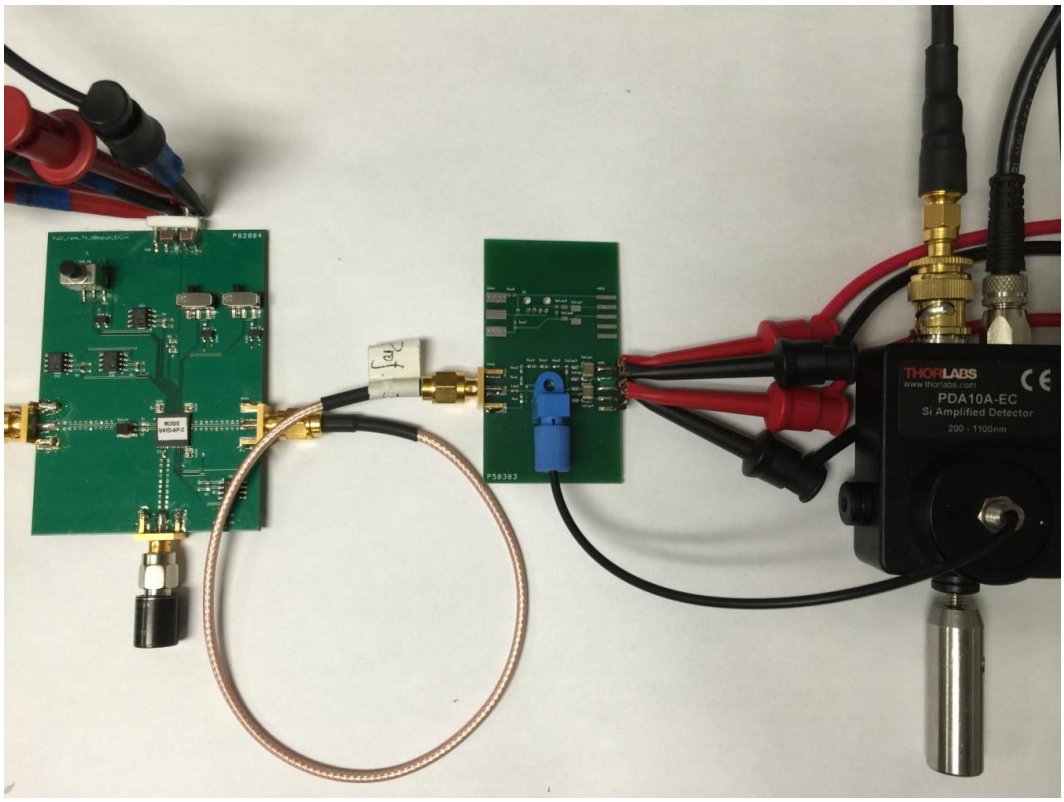


Figure 0.6: PCB testbench (with input from pre-emphasis driver)

In order to prove the benefits brought by pre-emphasis, a comparison experiment is implemented. The BERT system is setting to supply a regular 2^7-1 PRBS signal with the same output swing as pre-emphasis driver, which is 350mV as describe above. Anritsu MP1008A signal analyzer is used to provide 2^7-1 PRBS signal. The output eye diagram from the receiver is measured by an Agilent infiniium 54855A DSO with 6GHz analog bandwidth. In order to manifest the benefit of pre-emphasis, the pre-emphasis strength is configured to be strongest by setting control bits B_1B_0=11. While the logic one level is 350mV, the peaking is around 600mV. The attenuation brought by 50Ω interconnect of both cases are matched by using the same length coaxial cable.

The 200Mbps eye diagram is shown in Figure 5.7(a)(b) with the same scale. With regular driver signal the eye diagram has height of 120mV and width of 3ns. By using pre-emphasized driver signal, the eye diagram shows the eye height is increased from 120mV to 170mV by 41.6% while the eye width is increased from 3ns to 4ns by 33%.

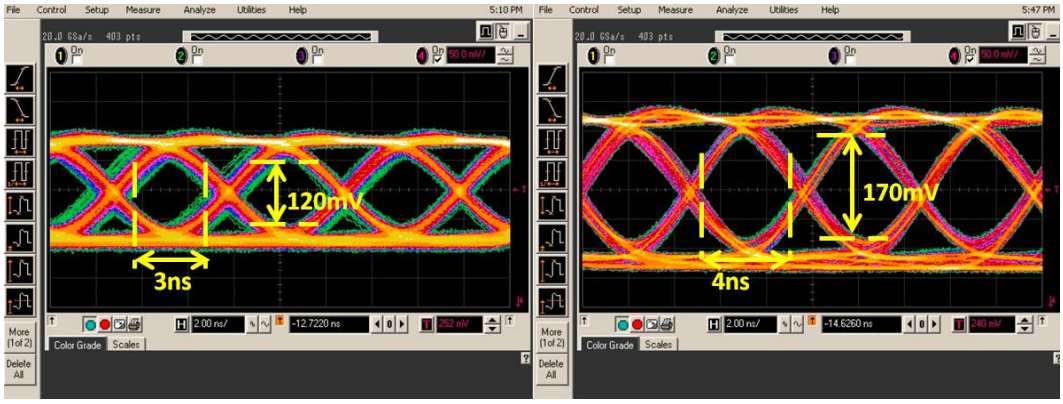


Figure 0.7: 200Mbps eye diagram (a) with input from BERT system (b) with input from pre-emphasis driver

The signal to noise ratio (SNR) can be estimated according to equation (5.1)[44]

$$SNR = \frac{eye\ level\ one - eye\ level\ zero}{rms\ noise\ level\ one + rms\ noise\ level\ zero} \quad (5.1)$$

Based on SNR, the bit error rate (BER) can be determined according to equation (5.2) [45]. Figure 5.7(a) indicates the BER is around 10^{-15} while Figure 5.7(b) indicates the BER is as good as 10^{-18}

$$BER \approx \frac{1}{SNR*\sqrt{2\pi}} e^{\frac{-SNR^2}{2}} \tag{5.2}$$

Figure 5.8 shows the 250Mbps eye diagram of both setups with the same scale. Using the pre-emphasis driver, the eye height is increased from 70mV to 120mV by 71.4% while the eye width is increased from 2.3ns to 3ns by 30.4%. The results show the extinction ratio of the received optical signal is considerably improved by using the pre-emphasis driver. By calculation the BER is improved from 10^{-8} to 10^{-14}.

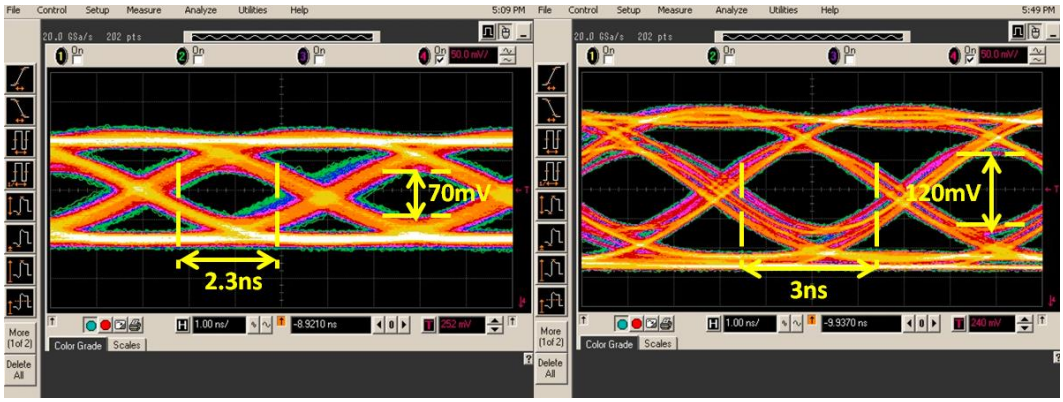


Figure 0.8: 250Mbps eye diagram (a) with input from BERT system (b) with input from pre-emphasis driver

Figure 5.9 shows the 300Mbps eye diagram of both setups. As it shows in the regular setup the eye is almost closed at 300Mbps. However, the eye diagram is still open when using pre-emphasis driver. The eye height is increased from 20mV to 50mV by 150% while the eye width is increased from 0.75ns to 1.75ns by 133%. By calculation the BER is improved from 10^{-2} to 10^{-3}.

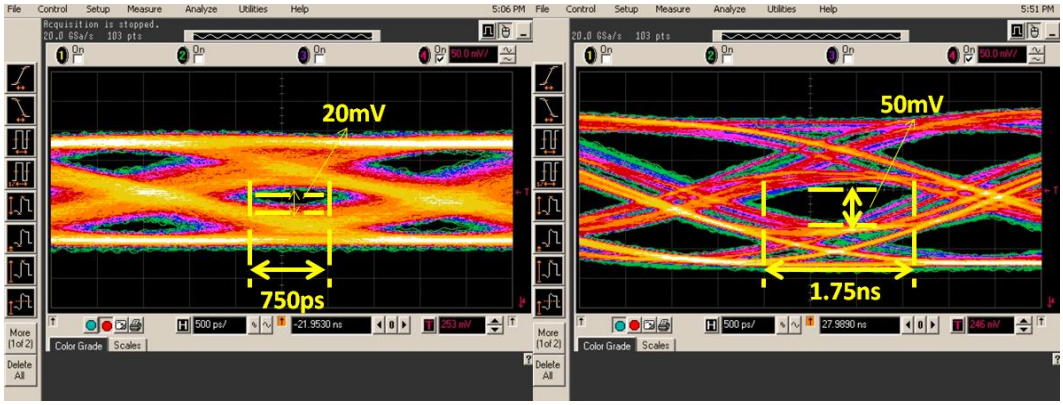


Figure 0.9: 300Mbps eye diagram (a) with input from BERT system (b) with input from pre-emphasis driver

By testing the eye diagram at different data rate with both setups, the BER is summarized in Figure 5.10. It can be seen that the BER getting worse with the increase of data rate, while the BER of pre-emphasis bench is at least ten times lower than the regular bench [101].

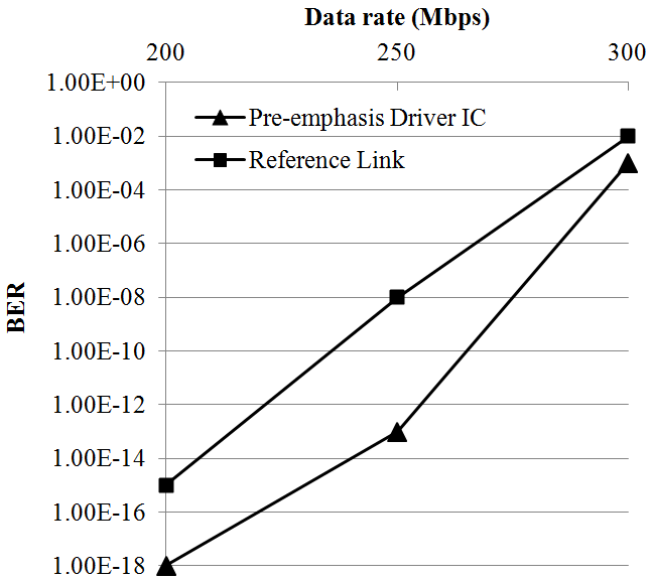


Figure 5.10: BER VS data rate comparison of regular and pre-emphasized PRBS

5.4 Summary

Pre-emphasis is a commonly used method for enhancing the bandwidth of data communcation. By producing a peaking at rising edge and falling edge of data signal, the LED can be quickly switched on and off with better signal to noise ratio. A RF-MOSFET switch based LED module is designed. A comparison experiment shows by using the pre-emphasis driver, the eye diagram is much more clear than the results with regular driver. At data rate of 300Mbps, the setup with pre-emphasis driver still has open eye. The BER calculation shows it has been improved at least 10 times at the data rate of 300Mbps. The experiment results show that the pre-emphasis is a effective method to enhance the LED bandwidth.

Chapter 6

A traveling wave electrode electroabsorption modulator (TWE-EAM) design in a commercial process

As discussed in Chapter 5, the speed of modulator can be enhanced by using advanced process with smaller feature size. It is expected that the modulator can work at intrinsic speed as high as 30Gbps[55] and even higher when HBT with smaller feature size is adopted for modulator device[54]. When the data rate is 20Gbps or higher, the parasitic *R* and *C* along the interconnection between driver and modulator will be considerable and they will slow down the speed of modulator.

One method to minimize the parasitic *R* and *C* is to utilize traveling wave electrode (TWE), which is designed as a distributed component with parasitic *L* and *C* absorbed into the characteristic impedance Z_0. Before silicon modulator is invented, TWE is spread used in $L_iN_bO_3$ modulators by numerical field simulation employing the method of lines [102][103] and finite element method (FEM) [104][105] or building equivalent circuit model [106][107][108][109]. Quasi-static equivalent circuit model is generated based on Quasi-TEM waveguide approximation which is favorable over numerical field simulation method because it requires less computing resource while the physical insight is more clear [110]. In recent years there are quite a few silicon electro-optic modulator (EOM) invented with bandwidth enhanced by using TWE such as [111][112][113][114][115][116][117][118]. Some polymer material based modulator also adopt TWE such as [119]. At the same time, the TWE applied into EAM helps to enhance the bandwidth to 50GHz and above [120][121][122][108]. Moreover, TWE can also be applied to build a traveling wave photodetector array (TWPDA) [123].

The other method to minimize the load effect of the electrode is to use

quasi-TWE. Different from traditional TWE which is focused on electrode physical design, quasi-TWE put its effort on using multiple driver cells along the electrode with their output signal with particular phase difference [124][125]. However, the application of multiple driver cells is at the cost of high power consumption.

For traditional TWE-EOM and TWE-EAM, the TWE is usually designed in a manner of quasi-TEM waveguide by using the configuration of ground-signal or ground-signal-ground. It is difficult to be implemented into our work because our modulator device is a five contact HBT device. In the meantime, the distributed model of modulator device is quite different in our case because it's working in carrier-injection mode but not carrier-depletion mode. The third distinction is the TWE design will not be home-made but fabricated through commercial silicon VLSI process. Thus the TWE is designed under the restriction of layer stack availability. With the three major differences, a brand new TWE-EAM model and design methodology is required to be built.

This chapter is going to present a 3D TWE structure design for a carrier-injection HBT-based EAM device. Before TWE is designed, an equivalent model of the EAM device is built. Then a design methodology of TWE is going to be built within the restriction of commercial VLSI process. After TWE is designed, a 3D full wave simulator (CST Microwave Studio) is used for validation.

6.1 TWE-EAM distributed model

The cross-section view of the HBT-based EAM depicted in Chapter 2 is shown again in Figure 6.1. A TWE is required to be designed for the five contacts (CBEBC) of the 180μm HBT device.

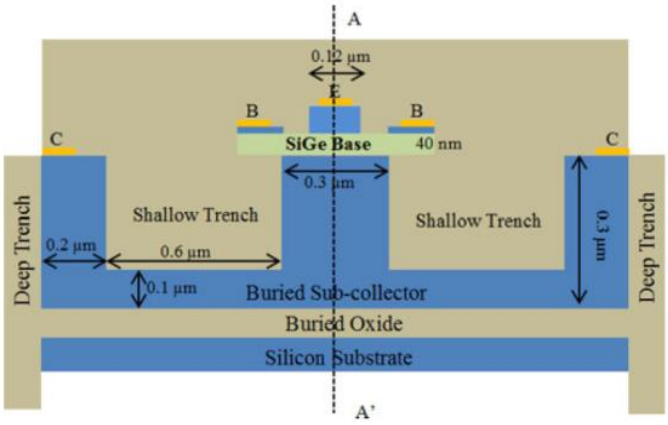


Figure 0.1: Cross-section view of HBT-based modulator

The side view of the modulator at the A-A' plane is depicted in Figure 6.2. For simplicity, only emitter, base, collector region and the buried cladding layer and silicon substrate are shown. In the figure the base-emitter (BE) and base-collector (BC) junction diodes are depicted. The RF signal from driver circuit travels along the TWE in the direction of *x*-axis, while light is traveling in the same direction with intensity continuing to be attenuated along the modulator.

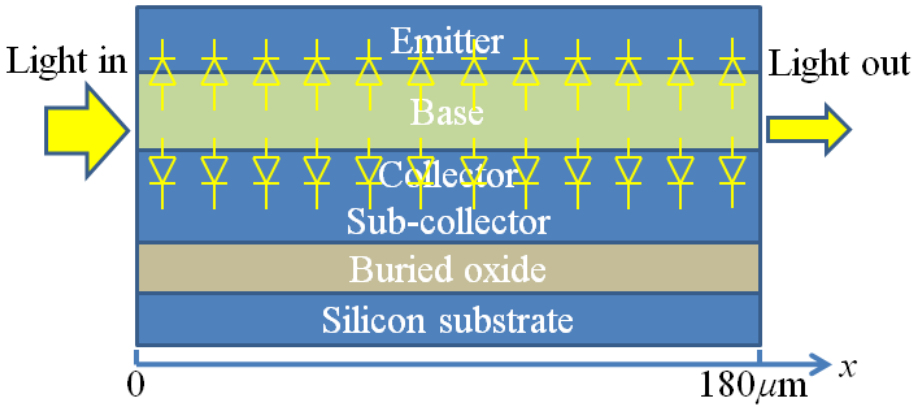


Figure 0.2: Side-view of modulator at A-A'

Before discussing the distribute model, the lumped EAM model with driving interface which has been discussed in Chapter 2 is reviewed here. Figure 6.3(a) shows the electrical interface of the lumped HBT-based modulator. The base terminal is driven by a PRBS signal which referenced to the grounded

emitter terminal. The collector terminal is biased to the ground. As the PRBS signal drives the base terminal the HBT will switch between saturation region and cut-off region, generating a large switching current at the collector terminal. Thus a large value high Q capacitor C_{decpl} is placed in proximity to the HBT device to supply the AC current, as shown in Figure 6.3(b). The self-resonant frequency of the capacitor should be higher than the frequency of interest.

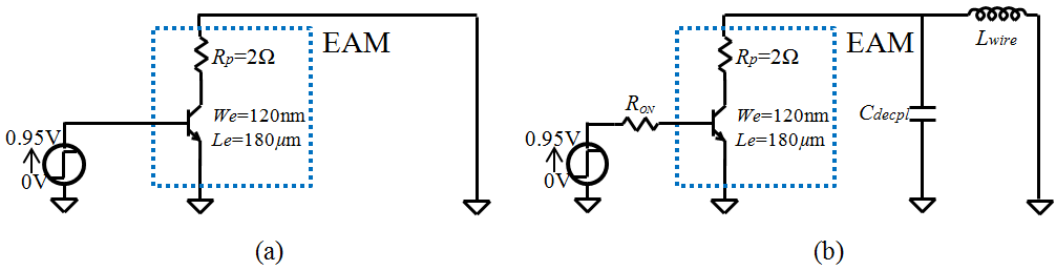


Figure 0.3: Lumped electrical model of HBT-based modulator. (a)Simplified model (b) Realistic model with L_{wire} and on-chip C_{decpl}

When frequency of interest is as high as making the signal wavelength comparable to the device physical size, for example, the wavelength is only 20 times device length or even shorter, then the distributed model of the device is required. Theoretically, the modulator can work at a speed up to 80Gbps or even higher. If the signal bandwidth is selected as 100% of the data rate, which is 80GHz. Then the wavelength

$$\lambda = \frac{v}{f} = \frac{c}{\sqrt{\varepsilon_r} * f} \tag{6.1}$$

is around 1.88mm. While the modulator length is around 180μm, it needs to be distributed modeled according to the "20:1" criteria.

In Figure 6.4 the distributed model of the HBT-based modulator is presented. As it shows, the lumped HBT-based EAM model is distributed into ten sections along the TWE which means there are totally ten small (18μm) HBTs with L_{wire}, C_{decpl} divided by ten for each of it. It should be noted that ΔR_p=10R_p because the R_p is paralleled connected.

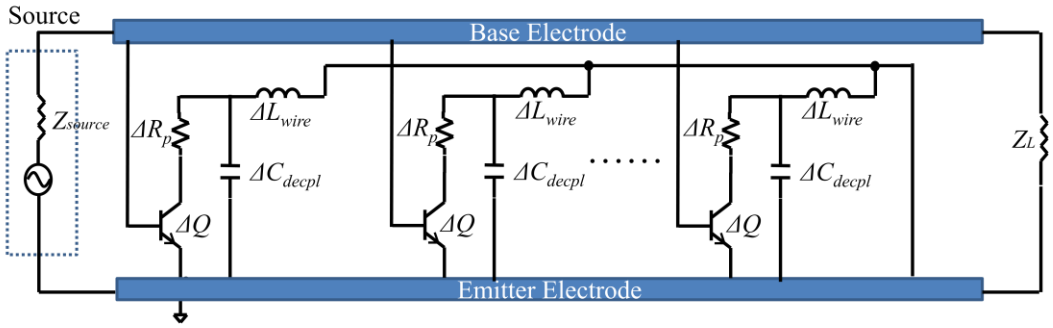


Figure 0.4: Distributed model of HBT-based modulator with source and load

By converting the base and emitter electrodes into distributed *R*, *G*, *C*, *L* components, the distributed model of TWE-EAM system can be depicted by Figure 6.5.

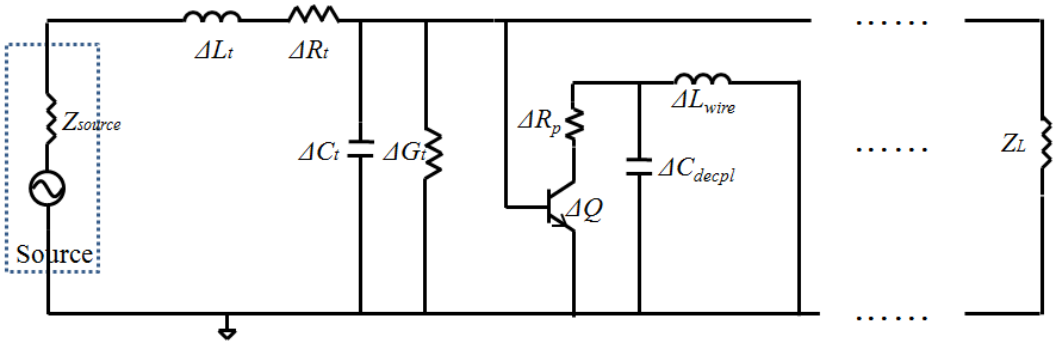


Figure 0.5: distributed model of TWE-EAM device

By using the equivalent model shown in Figure 6.5 to design the TWE-EAM system, the value of all the *R*, *G*, *C*, *L* components are desired to be voltage independent. It's obviously that the ΔR_t, ΔG_t, ΔC_t, ΔL_t satisfy the criteria because they are part of TWE which is passive. However, ΔQ is a section of a HBT device works in between saturation and cut-off region, which is an active device. Thus, its equivalent model is highly voltage-dependent. Figure 6.6 shows a simplified large signal HBT VBIC model [126] in which the parasitic HBT formed by substrate(p+), collector(n+) and base(p+) is neglected.

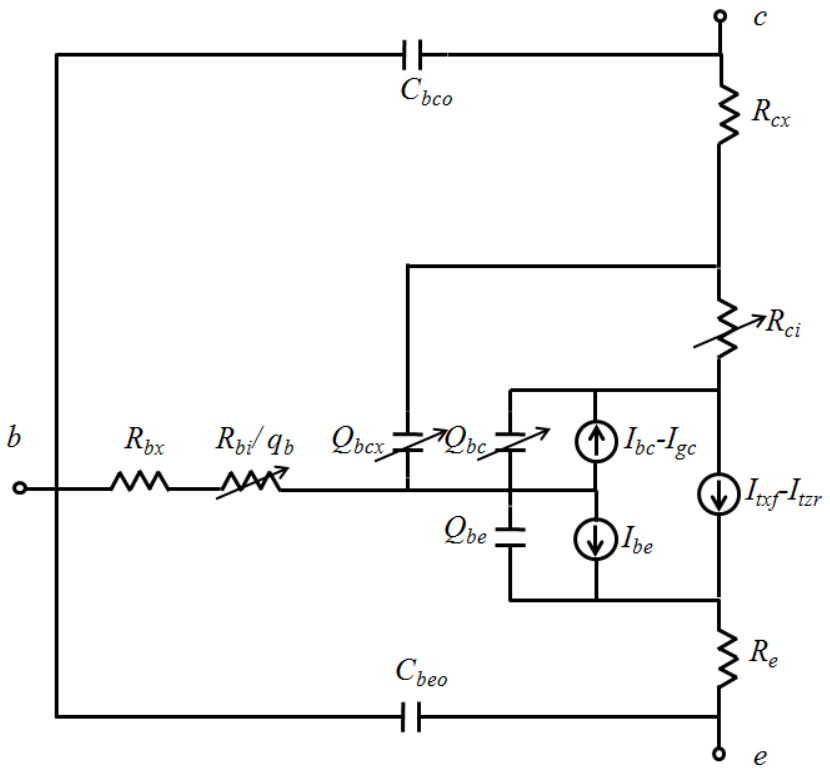


Figure 0.6: HBT VBIC model

The description of each component is summarized in Table 6.1 with some values are denoted for a HBT with drawn emitter dimension of 0.12μm*18μm. It should be noted that the value of C_{be}, C_{bc}, R_{bi}, R_{ci}, I_{be} and I_{bc} are voltage dependent. I_{txf} and I_{tzf} are neglected here because the collector and emitter are biased at the same voltage (ground) in our HBT configuration.

Table 6.1: VBIC component explanation and value

Component	Explanation	Value[1]
C_{beo}	BE Oxide (overlap) Capacitance	28.02fF
C_{bco}	BC Oxide (overlap) Capacitance	16.8fF
C_{be}	Intrinsic BE capacitance	26.64fF[2]
C_{bc}	Intrinsic BC capacitance	14.94fF[2]
C_{bcx}	Extrinsic BC capacitance	2.466fF[3]
R_{bi}/q_b	Parasitic base resistance (modulated)	3.51Ω[4]

R_{bx}	Extrinsic base resistance (fixed)	8.71Ω
R_{ci}	Intrinsic collector resistance (modulated)	4.3Ω
R_{cx}	Extrinsic collector resistance (fixed)	2.45Ω
R_e	Emitter resistance (fixed)	0.82Ω
I_{be}	Intrinsic BE current	N/A[5]
I_{bc}	Intrinsic BC current	N/A[5]
I_{gc}	BC weak avalanche current	N/A[5]
I_{txf}	Forward transport current, with excess phase	N/A[5]
I_{tzf}	Forward transport current, zero phase	N/A[5]

1. Value is for a HBT with drawn emitter dimension of 0.12μm*18μm
2. Intrinsic BE and BC capacitance value here is at zero bias voltage
3. Different from C_{bc} which is related to depletion and diffusion charges, C_{bcx} is related to diffusion only.
4. R_{bi} value here is at zero bias voltage
5. These values are bias voltage related

The following section will quantitatively discuss these components. Firstly, the *I-V* relationship of a PN junction with reverse-bias voltage or low forward bias voltage can be simply described by equation (6.1). The component I_{be} and I_{bc} in Table 6.1 approximately conforms to the equation which depend on bias voltage V_{be} and V_{bc} respectively.

$$I = I_s(e^{\frac{v}{v_T}} - 1) \tag{6.1}$$

For component C_{be} and C_{bc}, they are comprised of two components: junction capacitance C_j and diffusion capacitance C_d, according to equation (6.2). Junction capacitance C_j is due to the majority carrier charges displaced by the depletion region width. If the PN junction is deeply forward-biased, an excess of minority carrier charges will appear close to the depletion region edges which leads to diffusion capacitance C_d. In the equation C_{de} and C_{dc} are diffusion capacitance related to emitter region and collector region respectively.

$$\begin{cases} C_{be} = C_{je} + C_{de} \\ C_{bc} = C_{jc} + C_{dc} \end{cases} \tag{6.2}$$

The dependence of junction capacitance C_j to the bias voltage can be describe by equation (6.3). Here, V_b is the bias voltage; V_i is the built in junction voltage; C_0 is the zero-bias junction capacitance; while m is the junction grading coefficient. As it shows C_j is exponential proportional to the bias voltage.

$$C_j(V_{be}) = \frac{C_0}{(1-\frac{V_b}{V_i})^m} \tag{6.3}$$

Diffusion capacitance can be described by equation (6.4), which is derived by differentiate the minority charges close to the depletion region Q_d with respect to the bias voltage V_b. As it shows it's proportional to the bias current I_b. Because Q_d is originated from minority carriers, C_d is only considerable at deep forward bias but negligible at zero or reverse bias.

$$C_d = \left[\frac{dQ_d}{dV_b}\right]_{V_b} = \tau_T \left[\frac{I_b}{V_T}\right]_{V_b} \tag{6.4}$$

In VBIC model, the six component C_{je}, C_{de}, C_{jc}, C_{dc}, C_{beo}, C_{bco} are absorbed into five components C_{be}, C_{beo}, C_{bc}, C_{bcx}, C_{bco} according to Table 6.1. While R_{ci}, R_{cx}, R_e, I_{bc}, I_{be} are pretty small, the model shown in Figure 6.6 can be simplified into the model in Figure 6.7.

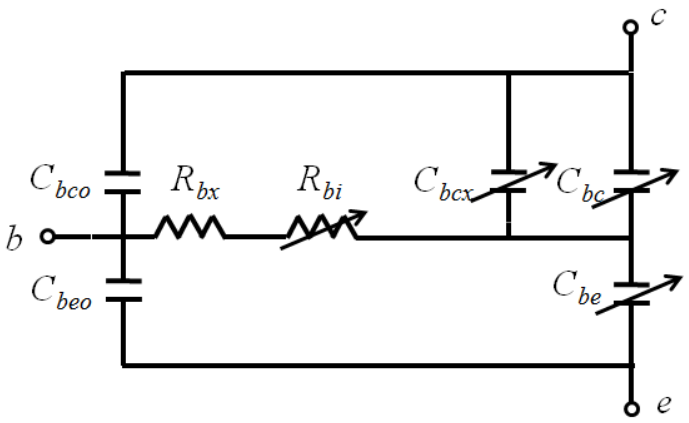


Figure 0.7: simplified HBT VBIC equivalent circuit

For the variables in Figure 6.7, which are C_{be}, C_{bc}, C_{bcx}, R_{bi}, bias voltage V_{be} is swept to characterize the their values under different bias condition. In Cadence spectre simulator, the value of C_{je} and C_{jc} can be monitored directly as primitive parameters which correspond to C_{be} and C_{bc}+C_{bcx} respectively. The curves of C_{je} and C_{jc} versus V_{be} are plotted and shown in Figure 6.8. As it shows the C_{je} and C_{jc} are nearly constant when V_{be} is lower than 0.85V. Based on the simulation, for an 18μm HBT working with the bias voltage lower than 0.85V, the value of C_{je} and C_{jc} are 440fF and 160fF respectively. Thus, V_{be} is required to be lower than 0.85V when the modulator is working in the TWE-EAM system.

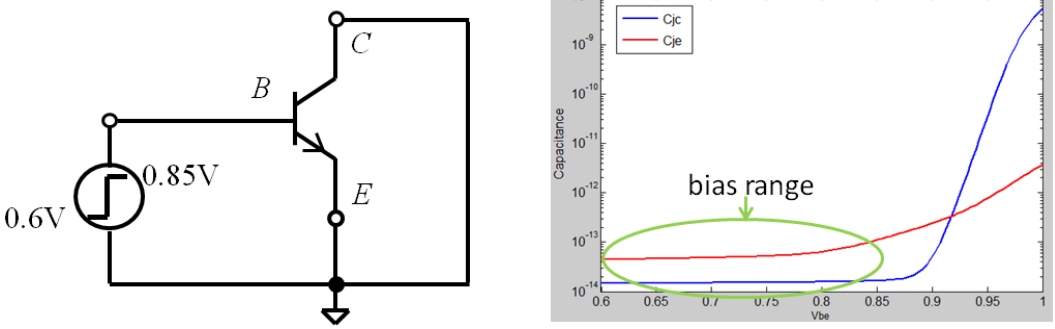


Figure 0.8: C_{je} and C_{jc} VS V_{be} of an 18μm HBT in the 130nm BiCMOS process

Within this operating range, the complete small signal model of the HBT-based TWE-EAM system is shown in Figure 6.9. Besides C_{je} and C_{jc}, the junction

oxide capacitance C_{beo} and C_{bco} are included with the values denoted in Table 6.1. This model is the fundamental for the following design and EM simulation.

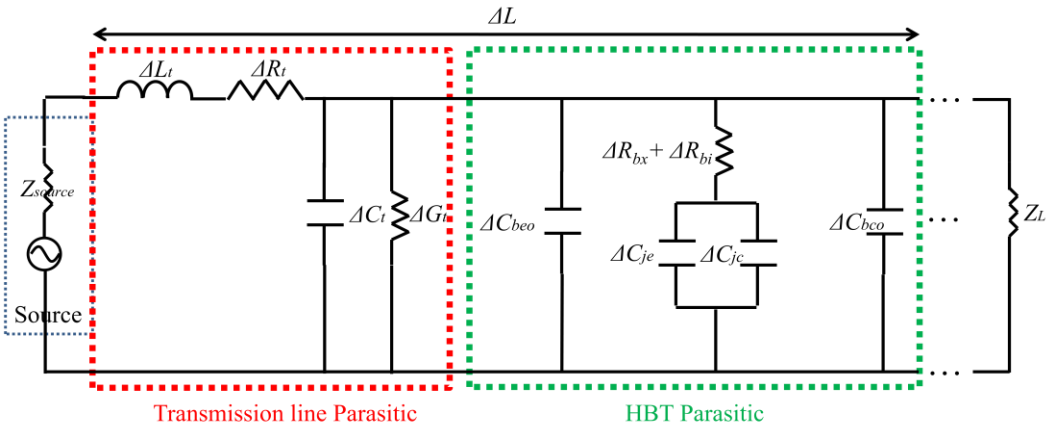


Figure 0.9: Complete small signal model of HBT-TWE

6.2 Design target

Generally speaking, the TWE applied for optical modulator usually has three major design targets [110].

A. Phase velocity matching

In a TWE-EAM system, the electrical wave and optical wave travel in parallel along the waveguide with phase velocity denoted as $\mu_{p,e}$ and $\mu_{p,o}$ respectively. It is desirable to ensure that the electrical and optical phase velocities are closely matched to improve the optical extinction ratio and increase the modulation bandwidth with low BER.

B. Impedance matching

As a special case of the transmission line, the TWE-EAM also requires impedance matching both at the source and load for maximum power transmission.

C. Insertion Loss

While the optical signal insertion loss has already discussed in Chapter 2, the electrical signal insertion loss is going to be discussed in this chapter. It mainly has three origins. The first origin is the lossy dielectric material around the TWE-EAM device. However, since the loss tangent of SiO_2 in the selected commercial 130nm process is as low as 0.00-0.001, the loss from the dielectric material can be neglected and the ΔG_t is set to zero in the following discussion.

The second origin is the lossy silicon substrate (for the selected process, ρ=11-16 Ω-cm and σ=7.41S/m). The energy coupling to the lossy substrate can be reduced by moving the electrodes away from it, i.e. the TWE implemented by high layer metals has lower loss due to the substrate. Secondly, the loss can be minimized by using microstrip structure because the ground plane helps to confine the signal energy between the electrodes but not leaking to the lossy substrate.

The third loss origin is the electrode itself because it is not a perfect conductor. Since the resistance of metal is inversely proportional to the thickness, the loss is lower if the electrodes are implemented with higher layer metals because higher layer metals are always thicker in commercial processes.

6.3 HBT-based TWE-EAM design methodology

The methodology is proposed with some constraints brought by commercial VLSI process by using which the whole TWE-EAM device is expected to be fabricated. As illustrated in Figure 6.10, the number of metal and dielectric layers are fixed according to the options provided by the process. In the meantime, the thickness of each layer is fixed without any tolerance to be adapted.

Figure 0.10: layer stackup of a seven metal layer commercial BiCMOS process

A flow chart of the design methodology is depicted in Figure 6.11. Custom circuit design tool Cadence Virtuoso and 3D full wave simulator CST Microwave Studio are co-simulated for this TWE-EAM design. To our best knowledge, this is the first work using this hybrid design methodology.

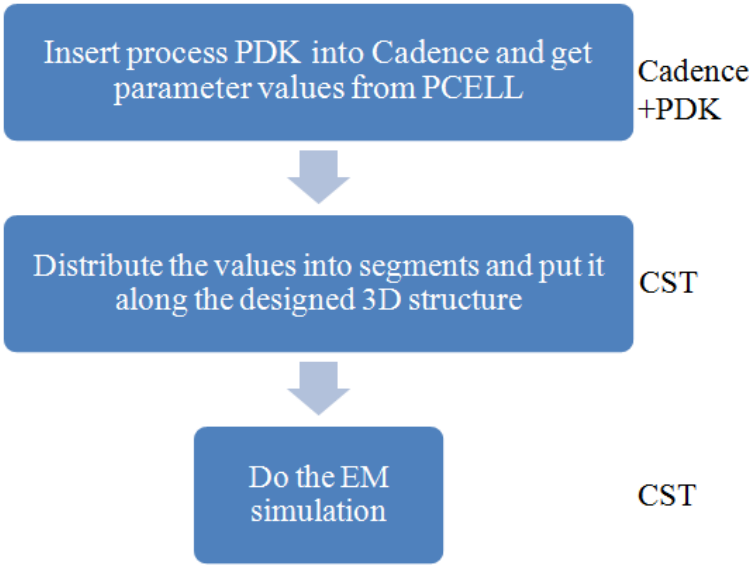


Figure 0.11: Cadence and CST Microwave Studio Co-simulation

6.3.1 $\mu_{p,e}$ design

As discussed in section 6.2 the electrical wave phase velocity $\mu_{p,e}$ should

be matched to the optical wave phase velocity $\mu_{p,o}$ for optimum extinction ratio and minimum BER. The $\mu_{p,o}$ is determined by the refractive index of the modulator waveguide described by equation (6.5).

$$\mu_{p,o} = \frac{C_0}{n} = \frac{3\times10^8}{2.375} = 1.26 \times 10^8 \text{ (m/s)} \tag{6.5}$$

The wave phase velocity $\mu_{p,e}$ of a microstrip transmission line in a silicon process is determined by the effective relative permittivity of the dielectric material (SiO_2 has $\mathcal{E}_r$=4), which is described in equation (6.6). Different metal layer combination changes the L_t and C_t separately but their product is kept constant only if the waveguide is still TEM. It results a constant $\mu_{p,e}$ with value only determined by $\mathcal{E}_r$.

$$\mu_{p,e,MSP} = \frac{1}{\sqrt{L_t * C_t}} = \frac{C_0}{\sqrt{\varepsilon_r}} = \frac{C_0}{2} = 1.5 \times 10^8 \quad \text{(m/s)} \tag{6.6}$$

Since the HBT-based TWE-EAM waveguide is designed as a TEM waveguide, the $\mu_{p,e}$ is still determined by parasitic inductance L and capacitance C according to equation (6.6). However, the parasitic capacitance C not only includes C_t from TWE, but also the C_{je}, C_{beo}, C_{jc} and C_{bco} which are determined by the EAM device. The $\mu_{p,e}$ for the TWE-EAM is described in equation (6.7), with L_t and C_t are design parameters determined by TWE structure.

$$\mu_{p,e} = \frac{1}{\sqrt{L*C}} = \frac{1}{\sqrt{L_t*(C_t+C_{je}+C_{beo}+C_{jc}+C_{bco})}} \quad \text{(m/s)} \tag{6.7}$$

Combining equation (6.6) and (6.7) yields equation (6.8), which indicates the $\mu_{p,e}$ of TWE-EAM could be manipulated by choosing metal layer combination of the TWE microstrip. Here, the value of L_t can be retrieved from the 130nm BiCMOS process.

$$\mu_{p,e} = \frac{1}{\sqrt{L_t * [\frac{(1.5\times10^8)^{-2}}{L_t} + 3.36\times10^{-9}]}} \quad \text{(m/s)} \qquad (6.8)$$

It's easy to find that for a 7 metal layers process there are 21 (C_7^2) different metal combinations {[M(x), M(y)], x, y∈1, 2,…,7 and x>y} to implement the TWE microstrip. By solving equation (6.5) and (6.8) the target value of L_t is calculated to be 5.7 nH/m. The target value of L_t is pretty small so only 6 out of the 21 options with the format of {[M(x), M(x-1)], x=2,3,…7} are still under candidate list because the six options have the neighbor metal combinations which have large C_t and small L_t.

The calculated $\mu_{p,e}$ values for the 6 options are plotted in Figure 6.12. The x-axis of the plot is the L_t which corresponds to the 6 options. The y-axis shows the $\mu_{p,e}$ which is referenced to the phase velocity in vacuum C_0. The dotted red line shows the optical wave phase velocity $\mu_{p,o}$ which is the design target for $\mu_{p,e}$. The six triangular markers at the top show the phase velocity is the same for the 6 options without EAM model, which conforms to equation (6.6). The arrows indicate the slowdown of phase velocity when the EAM model is included calculated by equation (6.8). As shown in Figure 6.12, the combination M7-M6 and M6-M5 are not good options because of the low $\mu_{p,e}$. Since metal layers 1, 2, 3 are thinner and more resistive which will generate more losses, the combination M5-M4 is selected.

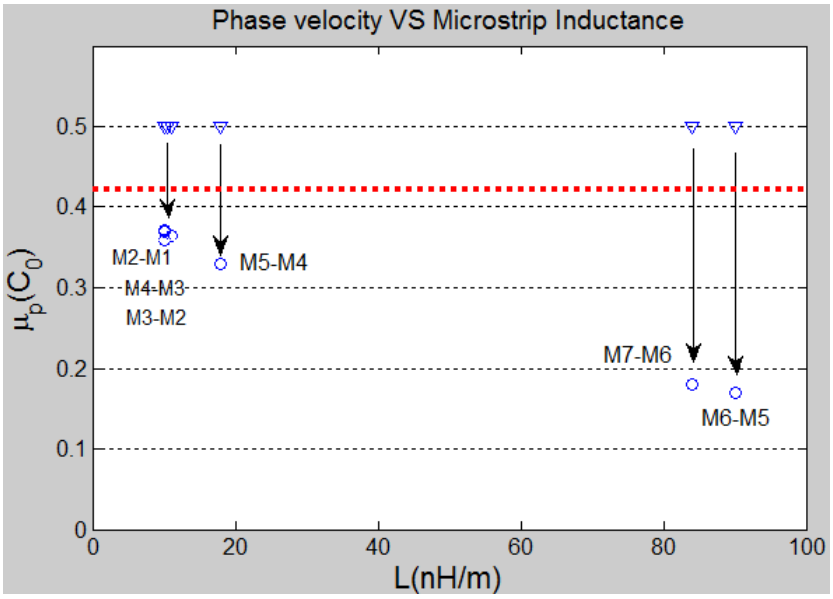


Figure 0.12: Phase velocity Vs microstrip inductance (triangular marker: without EAM model, circular marker: with EAM model)

The TWE structure is constructed based on the combination of M5-M4 and shown in Figure 6.13. Metal 5 is the signal plane which connects to the base terminal while Metal 4 is the ground plane which connects to the emitter terminal. The light blue area is the HBT-based EAM, which is constructed by P-material with high conductivity of 7.41 S/m, yielding the worst-case estimation of energy loss. The distributed components shown by dark blue cones are used for modeling the HBT-based EAM and inserted between the emitter and two base electrodes. It needs to be noted the real $\mu_{p,e}$ will be a little lower than the value calculated by equation (6.8) because extra capacitor C_{extra} exists at many locations in this quasi-microstrip structure as shown in Figure 6.13.

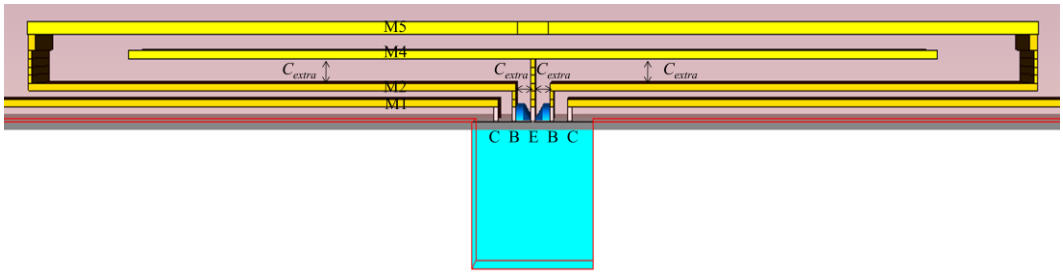


Figure 0.13: Cross-section view of TWE for the HBT-based EAM

The routing shows the base and emitter electrodes form a quasi-microstrip structure. The emitter electrode goes up vertically with a stack of vias to Metal 4 and then spreads to both sides to form the wide bottom plate of the microstrip with width of 40μm. This width is determined by the electro-migration limits of Metal 4. The two base electrodes travel vertically with a stack of vias to Metal 2, then spread both sides and up again with a stack of vias to Metal 5. Finally, the base electrodes travel around the emitter electrode and connect to each other to form the top plate of the microstrip. The two collector electrodes spread to both sides and travel vertically with a stack of vias to Metal 7 and connect to the MIM capacitors, which are not shown here for simplicity and will be shown later.

According to equation (6.8) the calculated $\mu_{p,e}$ should equal to $0.96*10^8$m/s. Actually, limited by the routing requirements of the five electrodes the additional parasitic capacitance C_{extra} exists at many locations as shown in Figure 6.13. These extra parasitic will change the effective ε_r of the TWE-EAM waveguide and subsequently change the $\mu_{p,e}$, which will be proven in simulation results in Section 6.4. It will be proven that the TWE-EAM waveguide is still a quasi-TEM waveguide.

6.3.2 Impedance matching design

For a TEM waveguide, both the characteristic impedance Z_0 and the phase velocity $\mu_{p,e}$ can be separately designed only if the dielectric material can be randomly selected. However, the dielectric material is fixed to SiO_2 in the commercial SiGe process. Thus, the Z_0 is set according to equation (6.9) after the $\mu_{p,e}$ is set according to equation (6.8)

$$Z_0 = \sqrt{\frac{L_t}{C_t+C_{je}+C_{jc}+C_{beo}+C_{ceo}}} = 1.76 \quad (\Omega) \tag{6.9}$$

The output impedance of the driver circuit is designed and matched to the calculated Z_0. Due to the small Z_0 value, a large buffer stage is required in the

driver circuit. The buffer circuit topology adopted and shown in Figure 6.14 is an emitter follower. The S_{22} of the driver circuit is simulated from 0-60GHz and the result is shown in Figure 6.15. It shows the driver can handle power transmission to the HBT-based TWE-EAM with small power reflection up to 60GHz. Also, as Figure 6.4 shows, a 2Ω resistor Z_L is implemented at the far end of the HBT-based TWE-EAM to minimize the power reflection at the load.

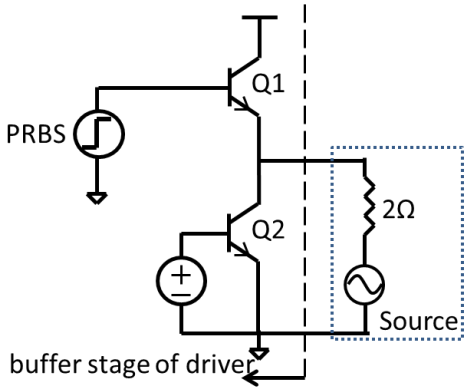


Figure 0.14: simulation setup of S_{22} of driver

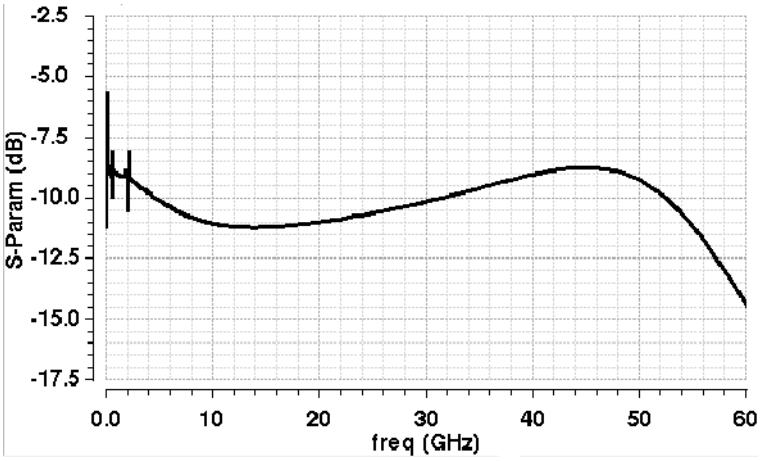


Figure 0.15: Simulation results of S_{22} of driver

6.3.3 C_{decpl} design

A capacitor operating at 60GHz frequency is designed as the decoupling capacitor shown in Figure 6.3. There is a thin dielectric layer fabricated with Si_3N_4 supported by this commercial process. Because for parallel plate capacitor

thin dielectric layer means high unit area capacitance, the Si_3N_4 layer is used for MIM capacitor design.

Figure 6.16 shows the 3D structure of the 300fF MIM capacitor. It uses metal 6 as the bottom plate, Si_3N_4 as the dielectric layer, and metal 7 as the final top plate (Immediate top plate is a very thin metal layer called QY specifically used for MIM capacitor fabrication). Multiple vias are applied to reduce the lead resistance which raises the self-resonant frequency of this MIM capacitor. Each pair of capacitor is closely placed along both side of an 18μm HBT-EAM as shown in Figure 6.20. There are ten pairs of 300fF MIM capacitor thus the total value of MIM capacitor along the both sides is 300fF*2*10=6pF.

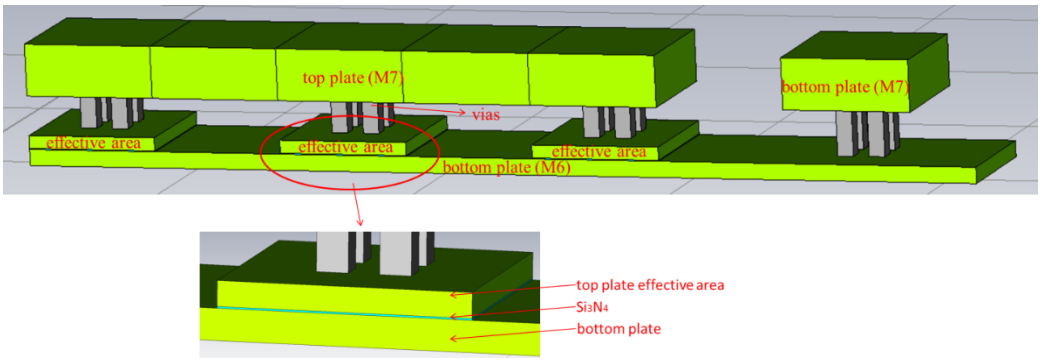


Figure 0.16: 300fF MIM capacitor works up to 90GHz

6.4 Results

6.4.1 MIM Capacitor C_{decpl}

The imaginary part of admittance versus frequency is plotted in Figure 6.17 after 3D full wave simulation. It is easy to be seen that the self-resonant frequency is boosted up to 90 GHz by using multi-vias to decrease the lead impedance. The expression of admittance described in equation (6.10) shows the slope of imaginary part is the capacitance. From Figure 6.17 it can be seen that the 300fF capacitance is nearly constant from DC up to 60GHz.

$$Y_c = G + jB = G + j\omega C \tag{6.10}$$

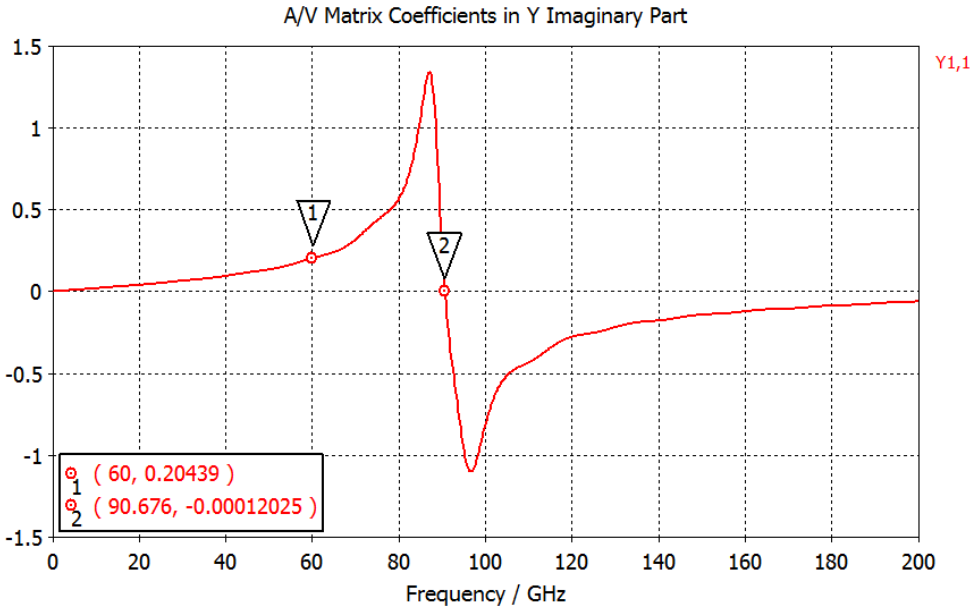


Figure 0.17: Imaginary part of admittance of the 300fF MIM capacitor

6.4.2 TWE-HBT-EAM simulation

The 3D view of the HBT-based TWE-EAM is shown in Figure 6.18[127]. The 180μm HBT-based EAM is placed along the *x*-axis. It has the same post-processed layers as Figure 6.1, thus it can be seen that the thickness of the subcollector area is etched down to 0.3μm and a 1μm SiO_2 layer is grown on the bottom of it. The quasi-TEM TWE is constructed with Metal 5 and Metal 4 and shown in yellow color. The twenty 300fF MIM capacitors are placed along the both sides of the EAM device. Waveguide ports are used at the front and the end of the TWE-EAM for simulation.

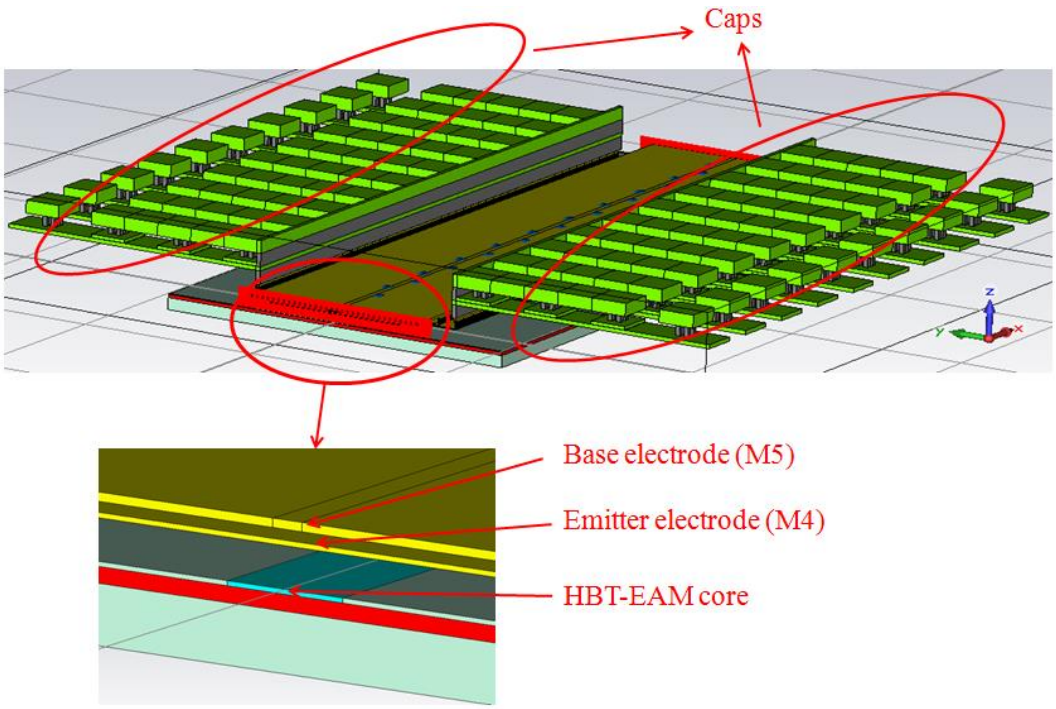


Figure 0.18: The 3D view of TWE-HBT-EAM (left: the whole structure, right: zoom-in of the HBT-EAM region)

Figure 6.19 presents the simulated E-field distribution of the HBT-based TWE-EAM. Result shows the wave is concentrated between the B-E microstrip and between the via stacks of B-E near the EAM which is in accordance with the design target. Two treatments are applied to minimize the extra capacitance C_{extra}. Firstly, the dimension '*d*' in Figure 6.19 is comparatively large. Secondly, Metal 2, but not Metal 3, was used to route the lower plane of the base electrode. Both treatments are used to minimize the C_{extra} which undesirably brings down the $\mu_{p,e}$.

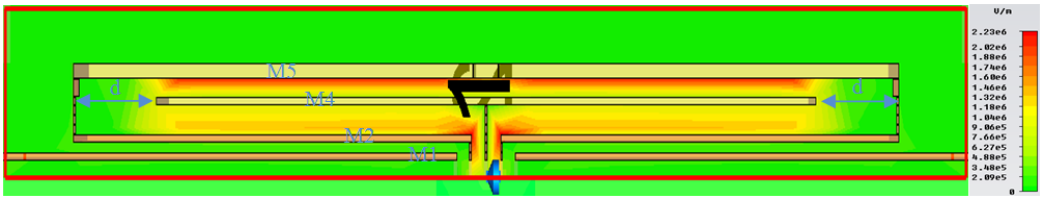


Figure 0.19: E-field of the TWE-HBT-EAM

The C_{extra} existing between the via stacks of base and emitter electrodes introduces a strong E-field around this area. The non-uniform E-field changes the effective ε_r and in further changes the $\mu_{p,e}$ of the TWE-EAM waveguide. However, it can be proved that it is still quasi-TEM waveguide by simulating the $\mu_{p,e}$ versus frequency. Moreoever, the $\mu_{p,e}$ can be characterized from the phase information of S_{21} results. In Figure 6.20 the green curve of phase shift versus the frequency shows the waveguide is non-dispersive up to 200GHz because the slope is constant. The value of $\mu_{p,e}$ can be calculated from equation (6.11). For example, marker number five shows at 60GHz the phase shift $\Delta\varphi_{shift}$ equals to 35.472 degree (in rad is 0.619). With L=180μm the $\mu_{p,e}$ can be calculated which equals to 1.1*10^8 (m/s). Due to the C_{extra} the effective ε_r' is higher than 4 thus the $\mu_{p,e}$ is lower than which of regular microstrip. The effective ε_r' of the TWE waveguide can be calculated by equation (6.6), which gives ε_r' equals to 7.44 for this TWE structure. Since it is proved that the waveguide is still quasi-TEM, the design methodology discussed above is valid.

$$\mu_{p,e} = \frac{\omega \cdot L}{|\Delta\varphi_{shift}|} \tag{6.11}$$

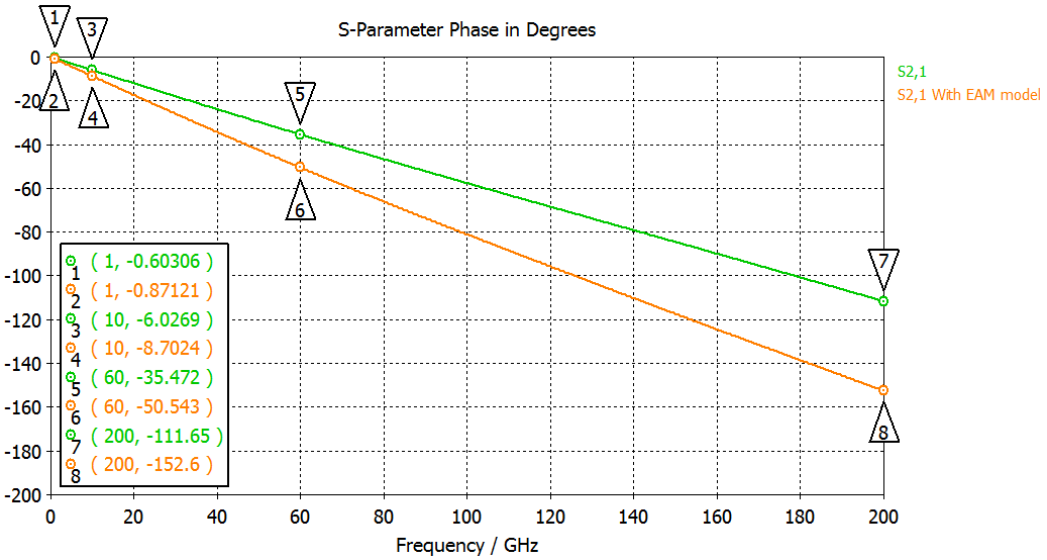


Figure 0.20: Dispersion simulation of TWE waveguide (green: without HBT-

EAM model; orange: with HBT-EAM model)

According to equation (6.7) the $\mu_{p,e}$ will be decreased in further after the HBT-based EAM model is added, which is proved by simulation result shown by orange curve in Figure 6.20. It's easily to be seen the waveguide is still non-dispersive. The new calculated $\mu_{p,e}$ $0.77*10^8$ (m/s) is lower than $0.96*10^8$ (m/s) which is due to the C_{extra}. Although the $\mu_{p,e}$ is only about 61% of the target $\mu_{p,o}$ ($1.26*10^8$ m/s), this is still the best option among all the options using the commercial process.

The S-parameter simulation referenced to 2Ω impedance is shown in Figure 6.21. The result shows the HBT-based TWE-EAM system has a S_{11} lower than -15.31dB and a S_{21} better than -0.96dB covering a bandwidth from DC-60GHz. Combined with the capacitor simulation results, it can be concluded that the TWE-EAM can enhance the bandwidth of the HBT-based EAM up to 60GHz with low insertion loss.

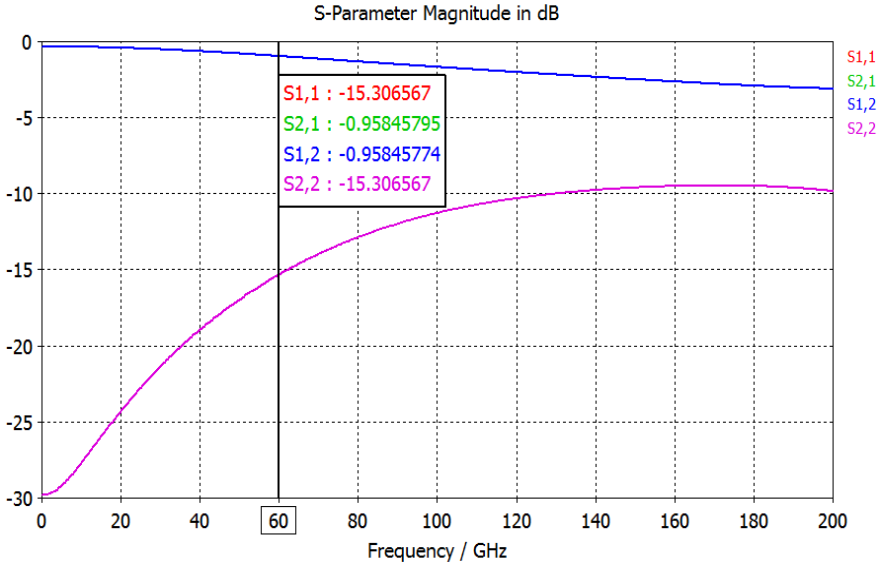


Figure 0.21: The S-parameter simulation of TWE-HBT-EAM

A 60Gbps eye diagram is simulated and shown in Figure 6.22. The eye is neatly opened with the amplitude is attenuated 0.34dB which is in accordance with S-parameter simulation results.

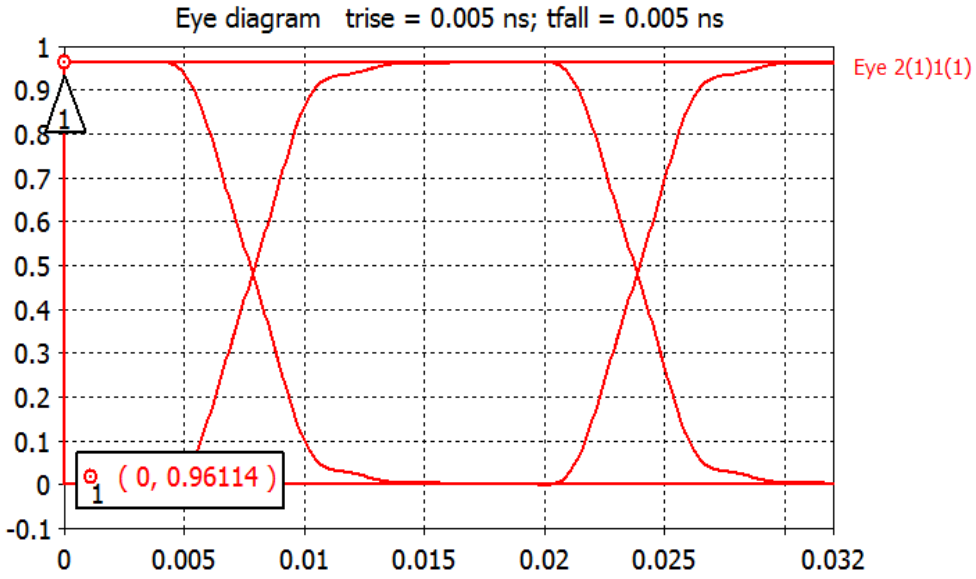


Figure 0.22: 60Gbps Eye diagram of the HBT-based TWE-EAM

6.5 Summary

A traveling wave electrode (TWE) modulator structure is presented in this chapter, including a novel design methodology to address process limitations imposed by a commercial silicon fabrication technology. Results from 3D full wave EM simulation demonstrate the application of the design methodology to achieve specifications, including phase velocity matching, insertion loss, and impedance matching. The TWE waveguide design is presented in detail, which includes the comparison and selection of metal combination for quasi-microstrip (Figure 6.12), phase velocity analysis and simulation (Figure 6.20), S-parameter simulation (Figure 6.21), and eye diagram simulation (Figure 6.22), etc. The 300fF AC current battery capacitor is designed and simulation shows it can work quite linearly up to 60GHz with resonant frequency around 90GHz. With the TWE, the modulator has the potential to work at data rate of 60Gbps and above.

Traditionally the TWE is only used for carrier-depletion type optical modulator. To our best knowledge, this is the first TWE design for a carrier-injection EAM to increase its modulation speed. Compromise is made to lower the V_{be} from 0.95V to 0.85V for better linearity but at the sacrifice of 3dB less extinction ratio. However, the extinction ratio can be made up to by increasing the length of modulator.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

Ever increasing data rate demands for high-performance computers and data centers have accelerated the need for inter-board or inter-chip input-outputs (I/O) supporting speeds beyond 100Gbps. Optical interconnect, which has much less dominant frequency-related loss, is favored over electrical interconnect for tera-scale computing application with lower loss, lower latency and higher power efficiency. The demand drives the feasibility of integration of optical communication system in the chip level. Traditionally the integration is 'hybrid' which means the optical components and electrical components are separately designed and fabricated before integrated electrically. It has the merit that each component can be custom tailored but has the deficiency of higher cost on multi-process fabrication and chip packaging. Silicon photonics has rapidly developed over the past two decades producing monolithically integrated photonic devices and electronic VLSI systems onto the same die realizing cost effective building blocks for optical interconnects.

Optical modulators are a key component of integrated silicon photonic chips for optical I/O. Due to very weak Pockels or Kerr effect, most silicon EO modulators utilize the free carrier plasma effect to manipulate the refractive index. By taking advantage of free carrier dispersion effect in silicon, there are three main categories of modulators. The first category is represented by Mach-Zehnder Interferometer (MZI) which uses phase change to realize amplitude modulation. The second category is called electroabsorption modulator (EAM). Different from MZI, it takes advantage of the light intensity change but not the phase change to realize the modulation. The third category of silicon modulator adopts resonant

structure such as micro-ring modulator. The micro-ring modulator structure is widely used and has several merits, including CMOS compatibility and ultra-low power operation. However, the narrow optical bandwidth and high sensitivity to temperature and process variation minimizes the robustness of the micro-ring structure. The implementation of tuning circuitry to improve the performance of this structure contributes considerable overhead power and increases system cost.

The free carrier dispersion effect can be utilized by three different methods. Modulator that change the carrier density based on majority carrier movement through the depletion region is classified as depletion type; while the modulator that change the carrier density by minority carrier injection through a p-n junction is classified as injection type. There is a third category called carrier accumulation which adopts an oxide layer in between PN junction forming a capacitor like modulator. From the perspective of CMOS process compatibility the injection modulators are favorable because the required driving voltage can be 1V or even lower. In the meanwhile, injection modulators intrinsically have much higher free carrier density change, which means the required footprint is much smaller.

This work presents a novel HBT-based carrier-injection modulator exhibiting wide optical bandwidth, high speed, low power, low drive voltage, small footprint, and high modulation efficiency. The HBT-based device is implemented in a commercial SiGe process, showing promise for a monolithic optical modulator solution. In this dissertation we have made the following contributions:

1. We built an electrical model of the post-processed HBT modulator. By using this model, the driver and other circuitry in the transmitter are designed and optimized.

2. We implemented the HBT-based modulator using a commercial BiCMOS process by adapting the HBT-device into a modulator. Several modifications has been made in the layout design phase and some other post-processing steps are carried out after the die is coming back from foundry.

3. We proposed a 10Gbps monolithic transmitter solution based on the HBT-based modulator. We tested and characterized the electrical and optical

performance of the modulator and analyzed the problems. To our best knowledge, this was the first monolithic optical transmitter design based on HBT modulator.

4. We designed and characterized an integrated 6Gbps ultra-low power transmitter driver module to provide drive signals for the silicon HBT-based modulator structure. The main features of the transmitter circuit are high speed, low power and high efficiency. An ultra-low power 2^7-1 PRBS generator is included on chip for high-speed testing which has outstanding power efficiency. A configurable pre-emphasis feature improves speed performance. The chip is realized in a 130nm SiGe BiCMOS process. Measurement results with a 50Ω load demonstrate transmitter modulation up to 6Gbps with digitally-tuned pre-emphasis strength.

5. We applied the ultra-low power driver to a red LED based communication link. By using the pre-emphasis feature, the data rate the link is enhanced to 300Mbps with the LED bandwidth of only 70MHz.

6. We designed a traveling wave electrode (TWE) for the HBT-based carrier-injection modulator which helps to enhance the data rate to 60Gbps and above. The TWE design proposed a new design methodology within the restriction of commercial process, which helps to realize the design targets such as phase velocity match, low insertion loss simultaneously.

7.2 Future work

For our future versions of optical transmitter module design, the improvements can be applied to leverage the performance from the following perspectives.

1. To realize the modulator fabrication effectively and efficiently, we need to coordinate an external foundry which can customize each layer of our device design.

2. Better process has lower supply voltage, higher f_T and lower R_{on}. By using better process, the transmitter speed can be enhanced with other performance improved.

3. If within power consumption budget, several changes can be applied to realize a transmitter module with higher speed. Some examples include: increase the tail current of PRBS generator and reduce the load resistance of the CML latch; use bipolar transistor instead of CMOS transistors; use multi-channel drivers, etc.

4. For traveling wave electrode design, different electrode structures can be experimented to produce a better phase velocity matching performance. In the meanwhile, quasi-TWE systems (multi-driver with specific phase delay to each other) can also be a good solution.

Bibliography

[1] CISCO systems, “Annual Global IP Traffic Forecast,” presented at the IEEE International Solid State Circuits Conference (ISSCC), 2012.

[2] Megaphase, “Phase3 Cable Datasheet.”

[3] ARC Electronics, “Calculating Fiber Loss and Distance.” .

[4] Cho, H, “Performance Comparison between Copper, Carbon Nanotube, and Optics for Off-chip and On-Chip Interconnects,” Ph.D., Stanford University, Stanford, CA, 2007.

[5] D. M. Kuchta, A. V. Rylyakov, C. L. Schow, J. E. Proesel, C. Baks, P. Westbergh, J. S. Gustavsson, and A. Larsson, “64Gb/s transmission over 57m MMF using an NRZ modulated 850nm VCSEL,” in *Optical Fiber Communications Conference and Exhibition (OFC), 2014*, 2014, pp. 1–3.

[6] Y. Lu and E. Alon, “A 66Gb/s 46mW 3-tap decision-feedback equalizer in 65nm CMOS,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, 2013, pp. 30–31.

[7] P. Westbergh, E. P. Haglund, E. Haglund, R. Safaisini, J. S. Gustavsson, and A. Larsson, “High-speed 850 nm VCSELs operating error free up to 57 Gbit/s,” *Electron. Lett.*, vol. 49, no. 16, pp. 1021–1023, Aug. 2013.

[8] D. M. Kuchta, C. L. Schow, A. V. Rylyakov, J. E. Proesel, F. E. Doany, C. Baks, B. H. Hamel-Bissell, C. Kocot, L. Graham, R. Johnson, G. Landry, E. Shaw, A. MacInnes, and J. Tatum, “A 56.1Gb/s NRZ modulated 850nm VCSEL-based optical link,” in *Optical Fiber Communication Conference and Exposition and the National Fiber Optic Engineers Conference (OFC/NFOEC), 2013*, 2013, pp. 1–3.

[9] Top 500 the List, “Top #1 Systems Sequoia.”

[10] IBM Microelectronics, “CPW model in IBM BiCMOS 8HP process.” .

[11] S. McNab, N. Moll, and Y. Vlasov, “Ultra-low loss photonic integrated circuit with membrane-type photonic crystal waveguides,” *Opt. Express*, vol. 11, no. 22, p. 2927, Nov. 2003.

[12] I. A. Young, E. Mohammed, J. T. S. Liao, A. M. Kern, S. Palermo, B. A. Block, M. R. Reshotko, and P. L. D. Chang, “Optical I/O Technology for Tera-Scale Computing,” *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 235–248, Jan. 2010.

[13] M. Haurylau, G. Chen, H. Chen, J. Zhang, N. A. Nelson, D. H. Albonesi, E. G. Friedman, and P. M. Fauchet, “On-Chip Optical Interconnect Roadmap: Challenges and Critical Directions,” *IEEE J. Sel. Top. Quantum Electron.*, vol. 12, no. 6, pp. 1699–1705, Nov. 2006.

[14] G. Chen, H. Chen, M. Haurylau, N. Nelson, D. Albonesi, P. M. Fauchet, and E. G. Friedman, “Electrical and optical on-chip interconnects in scaled microprocessors,” in *IEEE International Symposium on Circuits and Systems, 2005. ISCAS 2005*, 2005, pp. 2514–2517 Vol. 3.

[15] M. Stucchi, S. Cosemans, J. Van Campenhout, Z. Tőkei, and G. Beyer, “On-chip optical interconnects versus electrical interconnects for high-performance applications,” *Microelectron. Eng.*, vol. 112, pp. 84–91, Dec. 2013.

[16] S. Reynolds, “Samsung and GlobalFoundries sign multi-year 14 nm FinFET fab deal.” .

[17] Yokogawa, “Optical communications & Networks.” .

[18] Intel, “Intel Silicon Photonics Research.” .

[19] Frederic Gardes, Goran Mashanovich, and Graham Reed, “Evolution of optical modulation in silicon-on-insulator devices,” *SPIE Newsroom*.

[20] F. Y. Liu, D. Patil, J. Lexau, P. Amberg, M. Dayringer, J. Gainsley, H. F. Moghadam, X. Zheng, J. E. Cunningham, A. V. Krishnamoorthy, E. Alon, and R. Ho, “10-Gbps, 5.3-mW Optical Transmitter and Receiver Circuits in 40-nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2049–2067, Sep. 2012.

[21] J. F. Buckwalter, X. Zheng, G. Li, K. Raj, and A. V. Krishnamoorthy, “A

Monolithic 25-Gb/s Transceiver With Photonic Ring Modulators and Ge Detectors in a 130-nm CMOS SOI Process," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1309–1322, Jun. 2012.

[22] M. Rakowski, M. Pantouvaki, P. De Heyn, P. Verheyen, M. Ingels, H. Chen, J. De Coster, G. Lepage, B. Snyder, K. De Meyer, M. Steyaert, N. Pavarelli, J. S. Lee, P. O'Brien, P. Absil, and J. Van Campenhout, "22.5 A 4 #x00D7;20Gb/s WDM ring-based hybrid CMOS silicon photonics transceiver," in *Solid- State Circuits Conference - (ISSCC), 2015 IEEE International*, 2015, pp. 1–3.

[23] P. Dumon, W. Bogaerts, V. Wiaux, J. Wouters, S. Beckx, J. Van Campenhout, D. Taillaert, B. Luyssaert, P. Bienstman, D. Van Thourhout, and R. Baets, "Low-loss SOI photonic wires and ring resonators fabricated with deep UV lithography," *IEEE Photonics Technol. Lett.*, vol. 16, no. 5, pp. 1328–1330, May 2004.

[24] M. Gnan, S. Thoms, D. S. Macintyre, R. M. De La Rue, and M. Sorel, "Fabrication of low-loss photonic wires in silicon-on-insulator using hydrogen silsesquioxane electron-beam resist," *Electron. Lett.*, vol. 44, no. 2, pp. 115–116, Jan. 2008.

[25] MOSIS, "imec-ePIXfab Fabrication." .

[26] VPI photonics, "VPIcomponentMaker Photonic Circuits." .

[27] H. Rong, R. Jones, A. Liu, O. Cohen, D. Hak, A. Fang, and M. Paniccia, "A continuous-wave Raman silicon laser," *Nature*, vol. 433, no. 7027, pp. 725–728, Feb. 2005.

[28] G. Kurczveil, M. J. R. Heck, J. D. Peters, J. M. Garcia, D. Spencer, and J. E. Bowers, "An Integrated Hybrid Silicon Multiwavelength AWG Laser," *IEEE J. Sel. Top. Quantum Electron.*, vol. 17, no. 6, pp. 1521–1527, Nov. 2011.

[29] M. N. Sysak, D. Liang, R. Jones, G. Kurczveil, M. Piels, M. Fiorentino, R. G. Beausoleil, and J. E. Bowers, "Hybrid Silicon Laser Technology: A Thermal Perspective," *IEEE J. Sel. Top. Quantum Electron.*, vol. 17, no. 6, pp. 1490–1498, Nov. 2011.

[30] W. M. Green, M. J. Rooks, L. Sekaric, and Y. A. Vlasov, “Ultra-compact, low RF power, 10 Gb/s siliconMach-Zehnder modulator,” *Opt. Express*, vol. 15, no. 25, pp. 17106–17113, Dec. 2007.

[31] I. Goykhman, B. Desiatov, J. Khurgin, J. Shappir, and U. Levy, “Waveguide based compact silicon Schottky photodetector with enhanced responsivity in the telecom spectral band,” *Opt. Express*, vol. 20, no. 27, pp. 28594–28602, Dec. 2012.

[32] M. Casalino, G. Coppola, M. Iodice, I. Rendina, and L. Sirleto, “Near-Infrared All-Silicon Photodetectors,” *Int. J. Photoenergy*, vol. 2012, p. e139278, Dec. 2011.

[33] Y. Chen, M. Kibune, A. Toda, A. Hayakawa, T. Akiyama, S. Sekiguchi, H. Ebe, N. Imaizumi, T. Akahoshi, S. Akiyama, S. Tanaka, T. Simoyama, K. Morito, T. Yamamoto, T. Mori, Y. Koyanagi, and H. Tamura, “22.2 A 25Gb/s hybrid integrated silicon photonic transceiver in 28nm CMOS and SOI,” in *Solid- State Circuits Conference - (ISSCC), 2015 IEEE International*, 2015, pp. 1–3.

[34] C. Li, R. Bai, A. Shafik, E. Z. Tabasy, B. Wang, G. Tang, C. Ma, C.-H. Chen, Z. Peng, M. Fiorentino, R. G. Beausoleil, P. Chiang, and S. Palermo, “Silicon Photonic Transceiver Circuits With Microring Resonator Bias-Based Wavelength Stabilization in 65 nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1419–1436, Jun. 2014.

[35] J. D. Cressler and G. Niu, *Silicon-germanium Heterojunction Bipolar Transistors*. Artech House, 2002.

[36] G. L. Patton, J. H. Comfort, B. S. Meyerson, E. F. Crabbe, G. J. Scilla, E. de Fresart, J. M. C. Stork, J. Y.-C. Sun, D. L. Harame, and J. Burghartz, “63-75 GHz fT SiGe-base heterojunction bipolar technology,” in *1990 Symposium on VLSI Technology, 1990. Digest of Technical Papers*, 1990, pp. 49–50.

[37] G. L. Patton, J. H. Comfort, B. S. Meyerson, E. F. Crabbe, G. J. Scilla, E. de Fresart, J. M. C. Stork, J. Y. C. Sun, D. L. Harame, and J. N. Burghartz, “75-GHz f/sub T/ SiGe-base heterojunction bipolar transistors,” *IEEE Electron Device Lett.*, vol. 11, no. 4, pp. 171–173, Apr. 1990.

[38] N. Zerounian, F. Aniel, B. Barbalat, P. Chevalier, and A. Chantre, “500 GHz cutoff frequency SiGe HBTs,” *Electron. Lett.*, vol. 43, no. 14, p. -, Jul. 2007.

[39] “IBM Preps New Wireless Chip Technology,” 04-Jun-2013. [Online]. Available: http://www-03.ibm.com/press/us/en/pressrelease/41224.wss.

[40] Lars Zimmermann, “Silicon Photonics in Optical Communications.” SEMICON, 2013.

[41] D. Knoll, H. H. Richter, B. Heinemann, S. Lischke, Y. Yamamoto, L. Zimmermann, and B. Tillack, “Substrate Design and Thermal Budget Tuning for Integration of Photonic Components in a High-Performance SiGe:C BiCMOS Process,” *ECS Trans.*, vol. 50, no. 9, pp. 297–303, Mar. 2013.

[42] Mitsubishi electric, “Optical communication system.” .

[43] Justin Rattner and Mario Paniccia, “The 50Gbps Si Photonics Link--A research milestone from Intel Labs.” .

[44] Agilent, “Eye Diagram Measurements in Advanced Design System.” .

[45] Behzad Razavi, *Design of Integrated Circuits for Optical Communications*. McGraw-Hill, 2002.

[46] R. A. Soref and B. R. Bennett, “Electrooptical effects in silicon,” *IEEE J. Quantum Electron.*, vol. 23, no. 1, pp. 123–129, Jan. 1987.

[47] R. A. Soref and B. R. Bennett, “Kramers-Kronig Analysis Of Electro-Optical Switching In Silicon,” *Proc. SPIE, Integrated Optical Circuit Engineering IV, 1986*, vol. 0704, pp. 32–37.

[48] G. T. Reed, G. Mashanovich, F. Y. Gardes, and D. J. Thomson, “Silicon optical modulators,” *Nat. Photonics*, vol. 4, no. 8, pp. 518–526, Aug. 2010.

[49] Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, “Micrometre-scale silicon electro-optic modulator,” *Nature*, vol. 435, no. 7040, pp. 325–327, May 2005.

[50] Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya, and M. Lipson, “125 Gbit/s carrier-injection-based silicon micro-ring silicon modulators,” *Opt. Express*, vol. 15, no. 2, p. 430, Jan. 2007.

[51] S. Deng, Z. R. Huang, and J. F. McDonald, “Design of High Efficiency Multi-GHz SiGe HBT Electro-Optic Modulator,” *Opt. Express*, vol. 17, no. 16,

pp. 13425–13428, Aug. 2009.

[52] S. Deng, T. G. Neogi, J. Novak, J. McDonald, and R. Huang, “Design of a short electro-optic modulator based on SiGe HBT structure,” *Opt. Express*, vol. 18, no. 3, pp. 1994–2001, Feb. 2010.

[53] T. Neogi, S. Deng, J. Novak, J. Guo, R. Clarke, M. R. LeRoy, J. F. McDonald, and Z. Rena Huang, “Modeling and Analysis of an 80-Gbit/s SiGe HBT Electrooptic Modulator,” *IEEE Photon J*, vol. 3, no. 1, pp. 42–56, Feb. 2011.

[54] T. Guha Neogi, G. Niu, D. Connelly, J. D. Cressler, Z. R. Huang, and J. F. McDonald, “Design of a 250-Gbit/s SiGe HBT Electrooptic Modulator,” *IEEE Photonics J.*, vol. 3, no. 5, pp. 897–914, Oct. 2011.

[55] P. Wu, R. E. Clarke, J. Novak, S. Deng, J. F. McDonald, and Z. R. Huang, “Ultrashort SiGe Heterojunction Bipolar Transistor-Based High-Speed Optical Modulator,” *IEEE J. Sel. Top. Quantum Electron.*, vol. 19, no. 2, pp. 7900109–7900109, Mar. 2013.

[56] E. Fu, V. J. Koomson, P. Wu, S. Deng, and Z. R. Huang, “Design of an integrated high-speed HBT-based electroabsorption modulator and driver in SiGe BiCMOS technology,” in *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2012, pp. 37–40.

[57] M.-S. Kao, F.-T. Chen, Y.-H. Hsu, and J.-M. Wu, “20-Gb/s CMOS EA/MZ Modulator Driver With Intrinsic Parasitic Feedback Network,” *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 22, no. 3, pp. 475–483, Mar. 2014.

[58] Y. Zhao, L. Vera, and J. R. Long, “A 10 Gb/s, 6 V p-p , Digitally Controlled, Differential Distributed Amplifier MZM Driver,” *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 2030–2043, Sep. 2014.

[59] B. Goll and H. Zimmermann, “10 Gbit/s SiGe modulator driver with 37 dB gain and 680 mW power consumption,” *Electron. Lett.*, vol. 48, no. 15, pp. 938–940, Jul. 2012.

[60] H. Koizumi, M. Togashi, M. Nogawa, and Y. Ohtomo, “A 10Gb/s burst-mode laser diode driver for burst-by-burst power saving,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE*

International, 2012, pp. 414–416.

[61] J. Verbrugghe, R. Vaernewyck, B. Moeneclaey, X. Yin, G. Maxwell, R. Cronin, G. Torfs, X.-Z. Qiu, C. P. Lai, P. Townsend, and J. Bauwelinck, "Multichannel 25 Gb/s Low-Power Driver and Transimpedance Amplifier Integrated Circuits for 100 Gb/s Optical Links," *J. Light. Technol.*, vol. 32, no. 16, pp. 2877–2885, Aug. 2014.

[62] T. Takemoto, Y. Matsuoka, Y. Sugiyama, H. Yonezawa, H. Yamashita, K. Adachi, T. Nakamura, E. Nomoto, K. Nakahara, H. Arimoto, K. Osada, and T. Ido, "A 50-Gb/s NRZ-modulated optical transmitter based on a DFB-LD and a 0.18- #x00B5;m SiGe BiCMOS LD driver," in *Optical Fiber Communications Conference and Exhibition (OFC), 2015*, 2015, pp. 1–3.

[63] M. Nagatani, Y. Bouvier, H. Nosaka, and K. Murata, "A 3-Vppd 730-mW Linear Driver IC Using InP HBTs for Advanced Optical Modulations," in *2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2013, pp. 1–4.

[64] N. Kono, H. Yagi, N. Itabashi, and H. Shoji, "Miniaturized Optical DP-QPSK Modulator Module with 3.2-W Power Dissipation Using InP-Based Modulator and Driver ICs," in *2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2013, pp. 1–4.

[65] J. Zucker and R. B. Lauer, "Optimization and Characterization of High-Radiance (Al,Ga)As Double-Heterostructure LED's for Optical Communication Systems," *IEEE J. Solid-State Circuits*, vol. 13, no. 1, pp. 119–124, Feb. 1978.

[66] R. A. Aroca, P. Schvan, and S. P. Voinigescu, "A 2.4- 60-Gb/s CMOS Driver With Digitally Variable Amplitude and Pre-Emphasis Control at Multiple Peaking Frequencies," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2226–2239, Oct. 2011.

[67] R. A. Aroca and S. P. Voinigescu, "A Large Swing, 40-Gb/s SiGe BiCMOS Driver With Adjustable Pre-Emphasis for Data Transmission Over 75 Coaxial Cable," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2177–2186, Oct. 2008.

[68] L. Zhang, J. M. Wilson, R. Bashirullah, L. Luo, J. Xu, and P. D. Franzon, “A 32-Gb/s On-Chip Bus With Driver Pre-Emphasis Signaling,” *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 17, no. 9, pp. 1267–1274, Sep. 2009.

[69] E.-J. Choi, S. Kim, Y.-K. Jeong, K. Kwon, and J.-H. Chun, “A low-swing AC- and DC- coupled voltage-mode driver with pre-emphasis,” in *2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2011, pp. 1–4.

[70] R. Sredojevic and V. Stojanovic, “Digital link pre-emphasis with dynamic driver impedance modulation,” in *2010 IEEE Custom Integrated Circuits Conference (CICC)*, 2010, pp. 1–4.

[71] Y.-S. Son, H.-H. Son, Y.-S. Kim, H.-S. Oh, and G.-H. Cho, “A Gray-Level Dependent Pre-Emphasis Column Driver With Fast Settling for Active-Matrix LCD Applications,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 54, no. 12, pp. 1057–1061, Dec. 2007.

[72] Y. Hayashi, M. Sonehara, S. Ueno, Y. Ito, A. Koyama, and H. Yamashita, “A 1.2Gb/s write driver with pre-emphasis overshoot control optimized for high density HDD applications,” in *Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005*, 2005, pp. 519–522.

[73] N. Fujimoto and H. Mochizuki, “477 Mbit/s visible light transmission based on OOK-NRZ modulation using a single commercially available visible LED and a practical LED driver with a pre-emphasis circuit,” in *Optical Fiber Communication Conference and Exposition and the National Fiber Optic Engineers Conference (OFC/NFOEC), 2013*, 2013, pp. 1–3.

[74] H. Li, X. Chen, J. Guo, Z. Gao, and H. Chen, “An analog modulator for 460 MB/S visible light data transmission based on OOK-NRS modulation,” *IEEE Wirel. Commun.*, vol. 22, no. 2, pp. 68–73, Apr. 2015.

[75] M. Zhang, “An experiment demonstration of a LED driver based on a 2nd order pre-emphasis circuit for visible light communications,” in *Wireless and Optical Communication Conference (WOCC), 2014 23rd*, 2014, pp. 1–3.

[76] Y. Tsunoda, M. Sugawara, H. Oku, S. Ide, and K. Tanaka, “8.9 A 40Gb/s VCSEL over-driving IC with group-delay-tunable pre-emphasis for optical

interconnection," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*, 2014, pp. 154–155.

[77] J. Wang, L. Sun, Z. Wang, N. Qi, P. Y. Chiang, and Z. Hong, "25 Gb/s VCSEL driver with pulse equalization technique," in *2014 IEEE Optical Interconnects Conference*, 2014, pp. 55–56.

[78] B. Sedighi and J. Christoph Scheytt, "40 Gb/s VCSEL driver IC with a new output current and pre-emphasis adjustment method," in *Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International*, 2012, pp. 1–3.

[79] D. Kucharski, Y. Kwark, D. Kuchta, D. Guckenberger, K. Kornegay, M. Tan, C.-K. Lin, and A. Tandon, "A 20 Gb/s VCSEL driver with pre-emphasis and regulated output impedance in 0.13 mu;m CMOS," in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, 2005, pp. 222–594 Vol. 1.

[80] I. S. Stievano, I. A. Maio, F. G. Canavero, and C. Siviero, "Behavioral macromodels of differential drivers with pre-emphasis," in *9th IEEE Workshop on Signal Propagation on Interconnects, 2005. Proceedings*, 2005, pp. 129–132.

[81] B. Mutnury, M. Swaminathan, M. Cases, N. Pham, D. De Araujo, and E. Matoglu, "Macro-modeling of non-linear pre-emphasis differential driver circuits," in *Microwave Symposium Digest, 2005 IEEE MTT-S International*, 2005.

[82] M. Honarvar Nazari, "Electrical and Optical Interconnects for High-Performance Computing," PhD thesis, California Institute of Technology, United States -- California, 2013.

[83] J. H. R. Schrader, "Wireline equalization using pulse-width modulation.," University Microfilms International, P.O. Box 1764, Ann Arbor, MI, 48106, USA, 2007.

[84] E. Laskin and S. P. Voinigescu, "A 60 mW per Lane, 4 23-Gb/s 2 1 PRBS Generator," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2198–2208, Oct. 2006.

[85] T. O. Dickson, E. Laskin, I. Khalid, R. Beerkens, J. Xie, B. Karajica, and

S. P. Voinigescu, “An 80-Gb/s 231-1 pseudorandom binary sequence generator in SiGe BiCMOS technology,” *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2735–2745, Dec. 2005.

[86] E. Fu and V. J. Koomson, “Monolithic ultra-low-power 6 Gbit/s inductorless PRBS generator for silicon HBT-based carrier-injection electro-absorption modulator,” *Electron. Lett.*, vol. 51, no. 12, pp. 921–923, 2015.

[87] V. Kozlov, P. Park, and S. P. Voinigescu, “4 #x00D7; 24 Gb/s 27 #x2014; 1 PRBS generator using 1.8 V MOS-HBT quasi-CML logic,” in *2012 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2012, pp. 1–4.

[88] K.-J. Sham, S. Bommalingaiahnapallya, M. R. Ahmadi, and R. Harjani, “A 3 5-Gb/s Multilane Low-Power 0.18- CMOS Pseudorandom Bit Sequence Generator,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 55, no. 5, pp. 432–436, May 2008.

[89] Fu, E, Wu, P, Huang, Z. Rena, and Koomson, V. J., “Monolithic Low Power 6-Gbps Opitcal Transmitter for a Silicon HBT-based Carrier Injection Electroabsorption Modulator,” *IEEE Trans. Circuits Syst. II Express Briefs* (under review).

[90] B. R. Moss, C. Sun, M. Georgas, J. Shainline, J. S. Orcutt, J. C. Leu, M. Wade, Y.-H. Chen, K. Nammari, X. Wang, H. Li, R. Ram, M. A. Popovic, and V. Stojanovic, “A 1.23pJ/b 2.5Gb/s monolithically integrated optical carrier-injection ring modulator and all-digital driver circuit in commercial 45nm SOI,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, 2013, pp. 126–127.

[91] X. Wu, B. Dama, P. Gothoskar, P. Metz, K. Shastri, S. Sunder, J. Van der Spiegel, Y. Wang, M. Webster, and W. Wilson, “A 20Gb/s NRZ/PAM-4 1V transmitter in 40nm CMOS driving a Si-photonic modulator in 0.13 #x00B5;m CMOS,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, 2013, pp. 128–129.

[92] A. E. Kelly, J. J. D. McKendry, S. Zhang, D. Massoubre, B. R. Rae, R. P. Green, R. K. Henderson, and M. D. Dawson, “High-speed GaN micro-LED arrays for data communications,” in *2012 14th International Conference on*

Transparent Optical Networks (ICTON), 2012, pp. 1–5.

[93] C. Xi, A. Mirvakili, and V. J. Koomson, "A Visible Light Communication System Demonstration Based on 16-Level Pulse Amplitude Modulation of an LED Array," in *2012 Symposium on Photonics and Optoelectronics (SOPO)*, 2012, pp. 1–4.

[94] N. B. Datiri, A. Mirvakili, C. Sthalekar, E. Fu, C. Xi, S. Nercessian, T. Shah, B. Noorani, and V. J. Koomson, "The Smart Room: a 100 Mb/s integrated optical access point transceiver for indoor visible light communication," *Proc. SPIE 8282, Broadband Access Communication Technologies VI, 8282K, 2012*, vol. 8282, p. 82820K–82820K–13.

[95] H. Li, X. Chen, B. Huang, D. Tang, and H. Chen, "High Bandwidth Visible Light Communications Based on a Post-Equalization Circuit," *IEEE Photonics Technol. Lett.*, vol. 26, no. 2, pp. 119–122, Jan. 2014.

[96] M. Noshad and M. Brandt-Pearce, "Application of Expurgated PPM to Indoor Visible Light Communications #x2014; Part I: Single-User Systems," *J. Light. Technol.*, vol. 32, no. 5, pp. 875–882, Mar. 2014.

[97] C.-L. Liao, C.-L. Ho, Y.-F. Chang, C.-H. Wu, and M.-C. Wu, "High-Speed Light-Emitting Diodes Emitting at 500 nm With 463-MHz Modulation Bandwidth," *IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 563–565, May 2014.

[98] I-fiberoptics, "IF-E99 datasheet." .

[99] Avago, "AV02-1802EN data sheet." .

[100] ATCeramics, "550L datasheet." .

[101] Fu, E., Mirvakili, A., and Koomson, V. J., "BiCMOS LED Pre-emphasis Transmitter IC Enabling Visible Light Communication up to 300Mb/s," *IEEE J. Light. Technology*, (preparing).

[102] J. Gerdes, K. H. Helf, and R. Pregla, "Full-wave analysis of traveling-wave electrodes with finite thickness for electro-optic modulators by the method of lines," *J. Light. Technol.*, vol. 9, no. 4, pp. 461–467, Apr. 1991.

[103] K. Wu, C.-Y. E. Tong, and R. Vahldieck, "Microwave characteristics of high-speed traveling-wave electrooptic modulators on III-V semiconductors,"

J. Light. Technol., vol. 9, no. 10, pp. 1295–1304, Oct. 1991.

[104] J. C. Yi, S. H. Kim, and S. S. Choi, "Finite-element method for the impedance analysis of traveling-wave modulators," *J. Light. Technol.*, vol. 8, no. 6, pp. 817–822, Jun. 1990.

[105] Koshiba, M., Tsuji, Y., and Nishio, M., "Finite-element modeling of broadband traveling-wave optical modulators," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 9, pp. 1627–1633, Sep. 1999.

[106] H. Chung, W. S. C. Chang, and E. L. Adler, "Modeling and optimization of traveling-wave LiNbO3 interferometric modulators," *IEEE J. Quantum Electron.*, vol. 27, no. 3, pp. 608–617, Mar. 1991.

[107] S. Hopfer, Y. Shani, and D. Nir, "A novel, wideband, lithium niobate electrooptic modulator," *J. Light. Technol.*, vol. 16, no. 1, pp. 73–77, Jan. 1998.

[108] G. L. Li, C. K. Sun, S. A. Pappert, W. X. Chen, and P. K. L. Yu, "Ultrahigh-speed traveling-wave electroabsorption modulator-design and analysis," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 7, pp. 1177–1183, Jul. 1999.

[109] J. Witzens, T. Baehr-Jones, and M. Hochberg, "Design of transmission line driven slot waveguide Mach-Zehnder interferometers and application to analog optical links," *Opt. Express*, vol. 18, no. 16, p. 16902, Aug. 2010.

[110] H. Yu and W. Bogaerts, "An Equivalent Circuit Model of the Traveling Wave Electrode for Carrier-Depletion-Based Silicon Optical Modulators," *J. Light. Technol.*, vol. 30, no. 11, pp. 1602–1609, Jun. 2012.

[111] D. Petousi, L. Zimmermann, A. Gajda, M. Kroh, K. Voigt, G. Winzer, B. Tillack, and K. Petermann, "Analysis of Optical and Electrical Tradeoffs of Traveling-Wave Depletion-Type Si Mach #x2013;Zehnder Modulators for High-Speed Operation," *IEEE J. Sel. Top. Quantum Electron.*, vol. 21, no. 4, pp. 1–8, Jul. 2015.

[112] Y. Zhou, L. Zhou, X. Sun, and J. Chen, "Design of traveling wave electrode for high-speed silicon modulators," in *Communications and Photonics Conference (ACP), 2012 Asia*, 2012, pp. 1–3.

[113] H. Ishihara, K. Oda, T. Ori, K. Goi, K. Ogawa, T.-Y. Liow, X. Tu, G.-Q. Lo, and D.-L. Kwong, “High-ON/OFF-contrast 10-Gb/s silicon Mach-zehnder modulator in high-speed low-loss package,” in *2014 International Conference on Electronics Packaging (ICEP)*, 2014, pp. 680–683.

[114] D. Marris-Morini, L. Vivien, J. M. Fédéli, E. Cassan, P. Lyan, and S. Laval, “Low loss and high speed silicon optical modulator based on a lateral carrier depletion structure,” *Opt. Express*, vol. 16, no. 1, p. 334, 2008.

[115] J. Wang, C. Qiu, H. Li, W. Ling, L. Li, A. Pang, Z. Sheng, A. Wu, X. Wang, S. Zou, and F. Gan, “Optimization and Demonstration of a Large-bandwidth Carrier-depletion Silicon Optical Modulator,” *J. Light. Technol.*, vol. 31, no. 24, pp. 4119–4125, Dec. 2013.

[116] T. Latchu, M. Pochet, N. G. Usechak, C. DeRose, A. Lentine, D. C. Trotter, and W. Zortman, “Power-penalty comparison of push-pull and traveling-wave electrode Silicon Mach-Zehnder modulators,” in *2014 IEEE Optical Interconnects Conference*, 2014, pp. 25–26.

[117] S. Dogru, J. H. Shin, and N. Dagli, “Traveling Wave Electrodes for Substrate Removed Electro-Optic Modulators With Buried Doped Semiconductor Electrodes,” *IEEE J. Quantum Electron.*, vol. 49, no. 7, pp. 599–606, Jul. 2013.

[118] A. Samani, M. Chagnon, D. Patel, V. Veerasubramanian, S. Ghosh, M. Osman, Q. Zhong, and D. V. Plant, “A Low-Voltage 35-GHz Silicon Photonic Modulator-Enabled 112-Gb/s Transmission System,” *IEEE Photonics J.*, vol. 7, no. 3, pp. 1–13, Jun. 2015.

[119] X. Zhang, B. Lee, C. Lin, A. X. Wang, A. Hosseini, and R. T. Chen, “Highly Linear Broadband Optical Modulator Based on Electro-Optic Polymer,” *IEEE Photonics J.*, vol. 4, no. 6, pp. 2214–2228, Dec. 2012.

[120] Y. Tang, H.-W. Chen, S. Jain, J. D. Peters, U. Westergren, and J. E. Bowers, “50 Gb/s hybrid silicon traveling-wave electroabsorption modulator,” *Opt. Express*, vol. 19, no. 7, p. 5811, Mar. 2011.

[121] J. Lim, Y.-S. Kang, K.-S. Choi, J.-H. Lee, S.-B. Kim, and J. Kim, “Analysis and characterization of traveling-wave electrode in

electroabsorption modulator for radio-on-fiber application," *J. Light. Technol.*, vol. 21, no. 12, pp. 3004–3010, Dec. 2003.

[122] K. Kawano, M. Kohtoku, M. Ueki, T. Ito, S. Kondoh, Y. Noguchi, and Y. Hasumi, "Polarisation-insensitive travelling-wave electrode electroabsorption (TW-EA) modulator with bandwidth over 50 GHz and driving voltage less than 2 V," *Electron. Lett.*, vol. 33, no. 18, pp. 1580–1581, Aug. 1997.

[123] X. Luo, J. Song, Q. Fang, X. Tu, L. Jia, T.-Y. Liow, M. Yu, and G.-Q. Lo, "First demonstration of silicon-based parallel-fed travelling-wave photodetector array (TWPDA)," in *Optical Fiber Communications Conference and Exhibition (OFC), 2014*, 2014, pp. 1–3.

[124] T. Kato, M. Sato, T. Yamase, K. Sato, and H. Noguchi, "10-Gb/s - 80-km operation of full C-band InP MZ modulator with linear-accelerator-type tiny in-line centipede electrode structure directly driven by logic IC of 90-nm CMOS process," in *Optical Fiber Communication Conference and Exposition (OFC/NFOEC), 2011 and the National Fiber Optic Engineers Conference*, 2011, pp. 1–3.

[125] T. Yamase, M. Sato, H. Uchida, H. Noguchi, K. Sato, and T. Kato, "10-Gb/s in-line centipede electrode InP MZM and low-power CMOS driver with quasi-traveling wave generation," in *Opto-Electronics and Communications Conference (OECC), 2011 16th*, 2011, pp. 61–62.

[126] McAndrew, Colin, "VBIC Fundamentals." .

[127] E. Fu, V. Joyner Koomson, P. Wu, and Z. R. Huang, "Traveling wave electrode design for ultra compact carrier-injection HBT-based electroabsorption modulator in a 130nm BiCMOS process," in *Proc. SPIE 8989, Smart Photonic and Optoelectronic Integrated Circuits XVI, SPIE Photonics West*, 2014, vol. 8989, p. 89890H–89890H–11.