Low Profile Packaging for MEMS Aero-acoustic Sensors

Submitted By

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Abstract

This thesis explores both a semi-automated conductive ink process and modifications to Draper Laboratory's i-UHD (Integrated – Ultra High Density) process for packaging MEMS devices. These methods are applied to packaging MEMS acoustic sensors for wind tunnel testing. The primary advantage of these methods is a reduction in surface topology between the package and the integrated MEMS sensors. In these particular applications, the sensor records surface pressure and shear stress under the turbulent boundary layer. In order to avoid self-noise effects or other modifications to the boundary layer structure associated with surface roughness, the interface between the MEMS sensor and its package must be as close to planar as possible.

The thickness of the viscous sub layer below the turbulent boundary layer is the upper bound on allowable surface topology. For wind tunnel flows at free stream velocities between 20 and 200 m/s and plate lengths on the order of half a meter, the Reynolds number is between 10^5 and 10^7. This suggests that the viscous wall unit will be on the order of 1 to 35 µm. The viscous sub layer is approximately 5 wall units thick, so surface topologies of between 5 and 175 µm are desired [1]. A previous packaging approach using gold wire bonds with Computer Numerical Controlled (CNC) machined epoxy fill resulted in a minimum surface topology of greater than 100 µm. In addition, for large arrays of MEMS microphones, yield issues were dominated by wire bond integrity problems. These two issues were the primary motivation for using Draper's i-UHD process and developing the low profile conductive ink process. However, the process is generally useful and can be applied to the packaging of various types of sensor systems that require low profile interconnects.

Acknowledgments

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Chapter 1

1. Introduction, Contributions, and Background

1.1 Introduction

The objective of this thesis is to package MEMS aero-acoustic sensors into low profile packages for wind tunnel testing. Two packaging methods will be explored, one being a precise placement of silver conductive ink on a PCB package and the other being three embedded sensors in a ceramic wafer using a variant of Draper Laboratory's integrated ultra high density (i-UHD) packaging approach. In order to avoid self-noise effects or other modifications to the boundary layer structure associated with surface roughness, the interface between the MEMS sensor and its package must be as close to planar as possible. The goal of this project is to successfully package MEMS acoustic sensors into these two respective packages with a surface topology that is within the viscous sub layer of flow.

In order for the package to accommodate a MEMS acoustic sensor using the i-UHD platform, research began looking at different materials that would be able to withstand an aggressive release etch (4:1 HF:HCl) [1]. Since these sensors would be released after they were embedded, materials such as chromium, gold, ceramic, epoxy, and Draper's commercially-available negative-toned photosensitive epoxy were the basis of the design. After materials that were already well characterized in the i-UHD platform were chosen, tests were designed in order to check their compatibility with the release etchant. Finally, the design for the sensor integration went through multiple iterations to critique ideas and finalize a plan. L-edit is design software for physical layout with hierarchical, foundry-compatible, design rule checking

verification. Soda lime masks were created for the six layer process using L-edit, and a process traveler was produced outlining and detailing each of the process steps that would be performed.

For the conductive ink process, the shear sensors were released before they were embedded into the printed circuit board package, and therefore materials could not be placed over the active surface of the MEMS sensor. For this reason, the packaging approach was designed around the careful consideration for the active layers in the MEMS device. The conductive ink process consists of a low profile, low volumetric resistivity silver conductive ink which is pneumatically dispensed from a syringe between the pads of the printed circuit board package and its integrated sensor. The package and sensor are mounted to an aluminum fixture on top of computer controlled micro-positioning stages for accurate and precise placement of the silver traces. To create a more repeatable process by eliminating variables, an in depth characterization of the different process parameters was performed. The resistance and trace geometry were compared to the process parameters of feed rate, syringe tip diameter, dispense pressure, and dispense duty cycle. The impedance and surface topology of the conductive ink packaging scheme were also compared to previous wire bonded hybrid packaging schemes.

1.2 Contributions

Most MEMS microphone systems on the market are packaged by conventional chip bonding and wire bonding on a single chip with high surface topologies [2]. It is believed that the i-UHD technology could advance the field of packaging for MEMS sensors, offering the ability for large arrays of sensors (thousands of microphone elements) on a ceramic wafer, low surface topology packages (less than 10 μm), and a potential for thinned flexible 100 – 125 μm thick substrates.

Once the thicker MEMS die (580 μm) and thinner Through Silicon Vias (150 μm) are embedded into the ceramic handle wafer through a unique encapsulation process, metal interconnects are micro-fabricated on the surface of the wafer using standard photolithographic processes. This allows large numbers of interconnects to be patterned simultaneously without the need for wire bonding, resulting in high yield and rapid manufacturing, even for very large arrays of chips. The metal traces connect to Through Silicon Vias (TSVs) which reroute the connection to the backside of the wafer. These TSVs are manufactured by deep reactive ion etching large cavities in silicon populated with hundreds of silicon "posts". Next, the posts are sputtered with titanium and copper to coat them completely. The final steps are to pot the cavities with epoxy and thin down the backside until the cavities expose the back of the TSV connection. Once they are fabricated, they get diced out in a four by ten array. Lastly, a polish-back step thins the entire wafer to 125 μm increasing flexibility because the neutral axis is closer to the surface of the wafer and also exposing the TSV connections in order to surface mount the module to its electronics.

This research will produce the largest spatial resolution and the largest array aperture of pressure and shear below the Turbulent Boundary Layer (TBL) ever taken. This research advances the i-UHD process by enabling it to be compatible with vibrating MEMS structures for the first time. In addition, this project will also provide a flexible array of sensors that can now be placed on curved surfaces such as an engine nacelle, airfoil or fuselage section in order to improve their designs. Finally, the TBL characterization with this design would improve acoustic properties such as reduced cabin and community noise and fuel efficiency by reducing weight and drag.

1.3 Background

1.3.1 History of MEMS Sensor Packaging

The earliest paper found on Micro Electro Mechanical Systems dated back to the mid 1950's by Smith, who was then at Bell Telephone Laboratories [3]. This was when the first stress-sensitive effects found in silicon and germanium was discovered. Researchers were starting to wonder if the same technology that was used to yield the transistor, which revolutionized the electronics industry, could be applied to sensors. During the early 1960's, a group of papers from the Honeywell Research Centre and the Bell Labs described the first silicon diaphragm pressure sensors and strain gauges [3]. The curiosity with sensor technology grew largely in the late 1960's and many other businesses in the U.S. started to commercialize silicon pressure sensors. These first few sensors were rudimentary by today's standards, but with advancements in silicon micromachining in the early 1970's, pressure sensors with non-planar geometries were developed and were arguably the first "true" MEMS sensors [3].

There has also been much progress and success in the last half century with manufacturing MEMS sensors, after Smith's breakthrough papers. MEMS technology has been very successful in the physical sensing context, yielding many small and robust devices such as microphones, strain gauges, accelerometers, and gyroscopes. The impact of pressure sensing, which has been used in a wide range of applications, has made the largest impact on the aerospace, medical, automotive, and process control industries. The sophistication of pressure sensors in the past 40 years has increased dramatically. The sensors manufactured today are exceedingly small and are able to use both capacitive and piezo-resistive sensing methods. Since the mid 1980's many have featured on chip signal processing and the ability to generate digital outputs [3].

A comparison of multiple microphones including a MEMS microphone similar to the ones that will be embedded into the i-UHD process will help illustrate some of the most common commercial MEMS acoustic sensors available. Firstly, the B&K 4134 shown below in Figure 1 is well known for its high quality, industry standard, and pulse system software, but has a relatively high voltage required compared to the other two commercial microphones [4]. Depending on the type, the insulator is made either of silicone-treated quartz, synthetic sapphire or synthetic ruby to give dimensional stability. The diaphragm consists mainly of nickel and the back plate and housing are made of high nickel alloys. This minimizes variations in sensitivity with temperature.

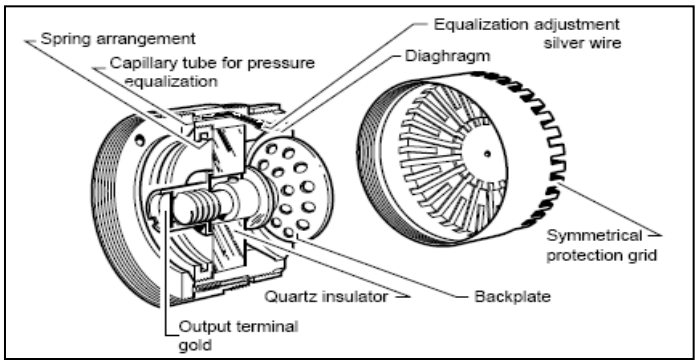


Figure 1: B&K 4134 microphone packaging diagram (Figure taken from Walter C. Babel III, Q.A.S., and James F. Bockman [4])

The Electret microphone is much smaller and cheaper than the B&K, but is also cheaply made in comparison to the B&K [4]. The Electret condenser microphone consists of a very light diaphragm and back plate which has a permanent charge implanted in an electret material to provide polarizing voltage. The principle of operation is that sound waves affecting the diaphragm cause the capacitance between it and the back plate to change at the same time, which in turn creates an AC voltage on the back plate. A picture is shown below in Figure 2.

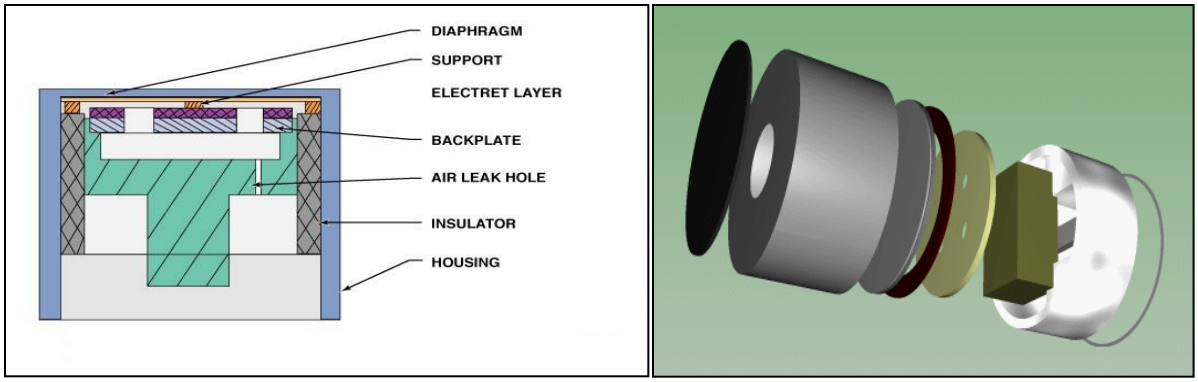


Figure 2: Electret microphone cross section and assembly view (Figure taken from Walter C. Babel III, Q.A.S., and James F. Bockman [4])

Finally, the MEMS microphone is multi-directional, draws very low current (<0.75 mA), and can operate at higher temperature [4]. The pressure-sensitive diaphragm is etched directly into a silicon chip by MEMS techniques, and is usually accompanied with integrated preamplifier. Most MEMS microphones are variants of the condenser microphone design. Often MEMS microphones have built in analog-to-digital converter circuits on the same Complementary Metal Oxide Semiconductor (CMOS) chip making the chip a digital microphone. A picture of a MEMS microphone is shown below in Figure 3.

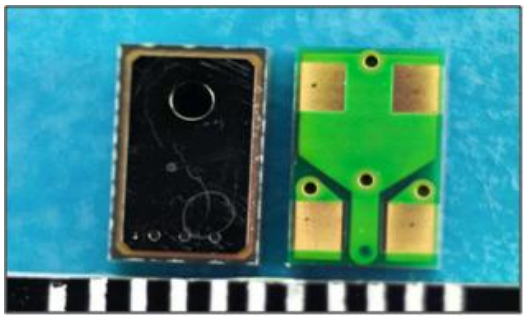
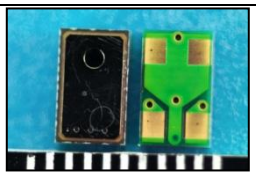


Figure 3: MEMS microphone top-view and bottom-view (Figure taken from Walter C. Babel III, Q.A.S., and James F. Bockman [4])

Since many of these microphones and their packaging methods have different tradeoffs, Table 1 below shows the comparison in performance and packaging attributes.

Table 1: General comparison of different microphones and their performance/packaging attributes

			
Name	B&K 4134	Electret	MEMS
Volume	>150 mm^3	100 mm^3	25mm^3
Support Electronics	High	Medium	Low
Power	Low	Low	Low
Voltage	200V	3V	1-3V
Mass	High	Low	Low
Cost	Very High	Low	Low
Sensitivity	High	Medium	Medium
Range	<100 KHz	<20 KHz	<50 KHz
Temperature	Low	Low	Medium

1.3.2 Alternative Packaging Methods Similar to the i-UHD Process

MEMS packaging is application specific and the package provides the physical interface of the MEMS device to the environment. Harsh environments may create different challenges for the packaging of MEMS. In addition to challenges related to the MEMS chip environment

and interfacing with that environment, challenges also exist inside the MEMS package, such as die handling, die attach, material compatibility, miniaturization and die release [5].

In order to incorporate MEMS devices into a commercial package for increased miniaturization, flip-chip packaging is widely used. Flip-chip packaging is one way to resolve some of the issues mentioned above, especially for large footprints and tall packages. Instead of connecting the MEMS device to its package through conventional wire bonding, which takes up a larger area, the device can be surface mounted to its package through flip-chip packaging as shown below in Figure 4. There are tradeoffs, as in any design, because flip-chip packaging poses challenges when active layers need to be exposed to the environment. In the case of flip-chip packaging, cutouts or gaps must be left in the package in order for the device to interact with its surroundings.

Another solution to improve miniaturization is 3-D stacking. Both of these methods of chip scale MEMS packaging (CSMP) are shown in Figure 4 and Figure 5 [2].

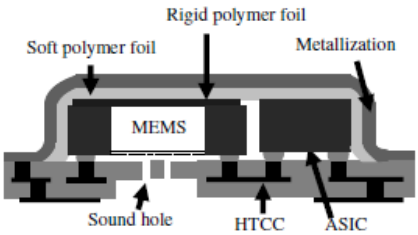


Figure 4: Schematic cross section of MEMS microphone packaged with CSMP (Figure taken from Winter, et al [2].)

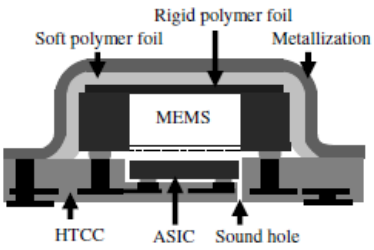


Figure 5: Schematic cross section of MEMS microphone using new 3-D stacking method (Figure taken from Winter, et al [2].)

For both package types the same chip set is used, but in the 3-D package, the Application Specific-Integrated Circuit (ASIC) is polished back to a height of only 120 μm before assembly. The process flow is also slightly different. Instead of first bonding the MEMS chip, now the ASIC chip is flip chip bonded into the cavity. After soldering the ASIC chip to the substrate, the MEMS chip is bonded by a thermosonic process. Another change in the package is the reduction of the number of holes in the substrate for the sound inlet. Since the available space of the ceramic surface is significantly reduced in the 3-D design, only two instead of the original four sound holes are used. Because the sound holes have a strong resistive behavior on the acoustic wave, the diameter of both sound holes has slightly been increased from 100 μm to 125 μm.

Another way to increase the density of a multi-chip module or in order to stack chips in 3-D is to incorporate Through-Silicon Vias (TSVs). A through-silicon via provides a means of implementing complex, multichip systems entirely in silicon, with a physical packing density many times better than today's advanced Multi-Chip Modules (MCMs) [6]. These TSVs are different than the TSVs used in the i-UHD design because instead of forming posts, cylindrical trenches are etched and filled with metal. To begin the process, an oxide layer is deposited using plasma enhanced chemical vapor deposition (PECVD). This oxide layer will serve as an isolation layer for topside processing. Titanium and copper are then deposited using physical vapor

deposition (sputtering). The thin layer of titanium is used as an adhesion layer between the oxide and copper. Next, photolithography is used to create the circular holes. A wet etch process is then used to open the holes through the copper and titanium layers. A wet or dry etch method can be used to open the holes through the oxide layer. Finally using Deep Reactive Ion Etching (DRIE), the vias are created as shown in Figure 6.

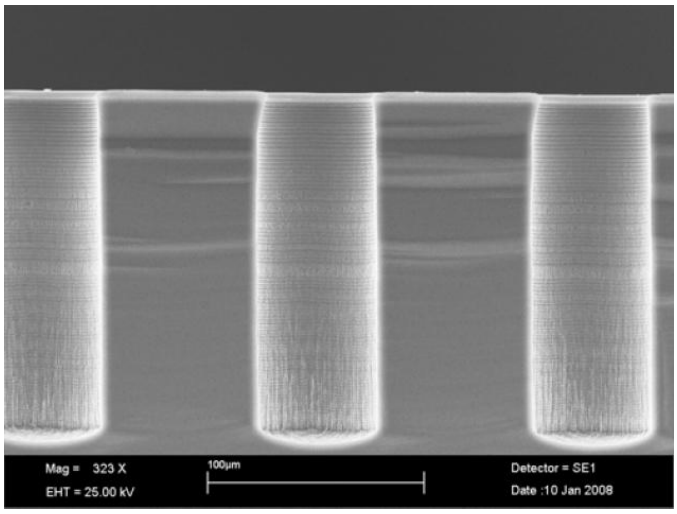


Figure 6: DRIE of the vias for the TSV (Figure taken from Spiesshoefer, S. and L. Schaper [17].)

A chemical vapor deposition (CVD) process is used to deposit SiO_2 in order to insulate the subsequent via metal from the surrounding silicon. Ideally, coverage over the entire via structure should he uniform, just like insulation on a wire. This is helped by the gentle slope of the via sidewall as previously discussed. Sidewall insulation of 0.5 µm thick has been produced, with excellent uniformity. A metal layer consisting of a barrier/adhesion layer and a copper seed layer is then deposited. The via must next be plated with copper until solid, with no voids that would trap the plating solution. After forming the solid vias with the copper plating solution, the wafer needs to be polished-back in order to expose the backside connections of the vias. Copper

pattern plating over a seed and barrier layer is then used to create the bottom connecting pads resulting in the finalized design for the TSV chip as shown below in the Figure 7.

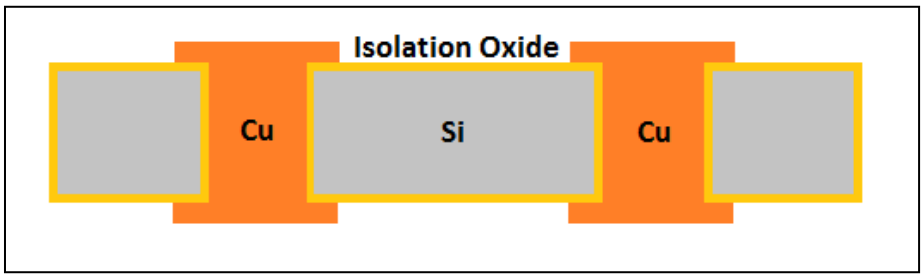


Figure 7: Overview of the TSV chip with oxide as the isolation layer, copper as the connection and silicon as the substrate

For some applications it is important to obtain 2-D measurements such as force, temperature, stress, and pressure on a 3-D object. If the surface is flat, then a single MEMS sensor can be used in order to characterize these parameters. As soon as the surface is non-planar, as in the case of a popular research object like the airfoil for aerodynamic applications, it becomes more challenging. This is where the motivation for flexible packages with integrated MEMS sensor arrays that could be taped or glue to a cylindrical surface come from.

A new micro-fabrication technology that enables the integration of MEMS devices on a flexible polyimide skin has been developed [7]. The flexible structure is manufactured with a thicker polyimide layer connecting multiple silicon islands in which the shear sensors are processed on as shown below in Figure 8.

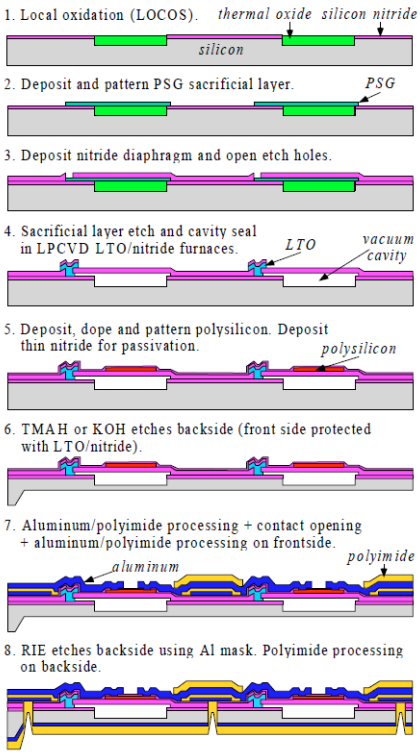


Figure 8: Simplified process flow for the flexible skin technology (Figure taken from Fukang, J., et al. [5].)

The process starts with selective TMAH or KOH etching on the backside of a silicon wafer using silicon nitride as an etch mask to form silicon membranes of desired thicknesses. Aluminum is evaporated on the front side and patterned to cover the area between future silicon islands. Polyimide is spun-on, cured and patterned to cover the protective aluminum completely. Sputtered aluminum metallization then follows to provide electrical leads. Another polyimide layer is spun-on and patterned to expose the bonding pads. Reactive Ion Etching (RIE) etching on the backside using aluminum as masking material removes the silicon on the areas between the silicon islands. Here, the first layer of aluminum serves as the etch stop in the SF_6 based RIE etching. Finally, a thick polyimide layer is spun-on and cured on the backside to

pack in the silicon islands. The finished packages are then cut off from the silicon wafer frame with a razor blade as shown in Figure 9 below.

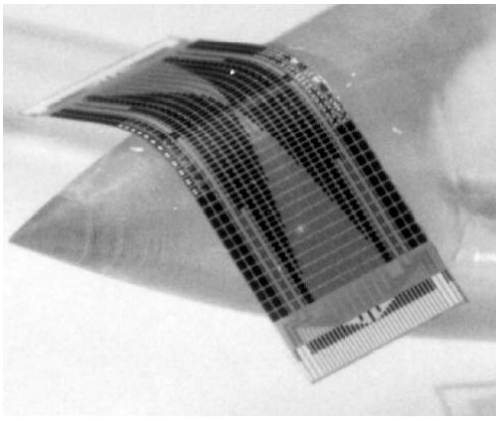


Figure 9: A flexible shear stress sensor sits on a conical object. Bending is due to gravitation. (Figure taken from Fukang, J., et al. [5].)

1.3.3 Alternate Packaging Methods Similar to the Conductive Ink Process

Inkjet printing provides an interesting approach to electronic packaging where small volumes of conductive ink are deposited on the surface of a substrate in order to form an electrical circuit. For this specific application, the conductive ink is dispensed interconnecting a System-In-Package (SiP), which contains Integrated Circuits (ICs) and discrete passive components that are encapsulated with a resin mold [8-10]. The encapsulation material acts as a substrate for interconnections, which are directly deposited on top of the mold. All connections between the components and connections to the input/output pins are formed by ink-jetting silver nano-particle and dielectric inks [11]. Silver nano-particles are sintered in an oven at 220°C and resistivity values lower than 5 μΩcm are reported. Pre-curing of a substrate in a higher temperature than the sintering temperature of silver nano-particles decreases the resistivity of the

lines. As a conclusion, the sintering profile needs to be optimized in order to achieve resistance requirements set by the design. The manufacturing process of a module using this process is outlined in Figure 10 below.

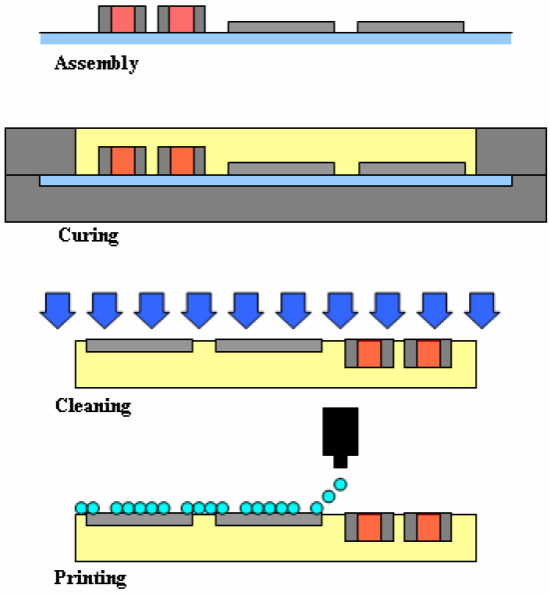


Figure 10: Process steps for ink-jet printed system in package manufacturing process (Figure taken from Matti Mäntysalo and Pauliina Mansikkamäki,[9].)

At the beginning, components are assembled on an adhesive carrier. High accuracy is essential due to small pitch values within the ICs. Alignment is more important than in the conventional surface mount devices because of the lack of self-alignment capability. Contact areas of the components must be placed towards the carrier. After the component assembly, the carrier is placed in the molding cast and the epoxy resin is poured inside the case. Narrow gaps between the components need to be filled, which sets strict requirements for the viscosity of the molding material. The denser the layout is, the lower the viscosity must be. Also, the surface of the adhesive carrier needs to be suitable for mold material. Furthermore, thermo-mechanical properties must be considered during the material selection. In general, materials with low

modules and coefficient of thermal expansion (CTE) are needed in order to minimize thermo-mechanical stresses and bowing in the package. The CTE value can be decreased with silica particles in order to match it better with the components. However, the particle size must be small enough to allow proper filling of the gaps. After the molding process, the module is ready for the printing. The components are placed in the contact side of the mold and the encapsulation material acts as a substrate for interconnections. The surface of the substrate needs a proper treatment. It is recommended to do both a physical and a chemical treatment. The physical treatment cleans with plasma. This reduces the amount of impurities on surface. After the surface treatment, the "wettability" of the surface is very high due to the increased surface energy and the droplet will spread. Therefore, a chemical surface treatment must be dispensed on the top of the surface in order to decrease its solid-vapor surface energy. A proper concentration of the surface treatment material can be estimated with contact angle measurements. Possible dispensing methods for surface treatment material are dipping, wiping, spraying, and ink-jetting. Proper deposition method depends on the application. The effect of the surface treatment can be seen in Figure 11 and Figure 12 below, which uses 3M EGC-1720 diluted with 3M HFE-7100 for the chemical treatment [8].

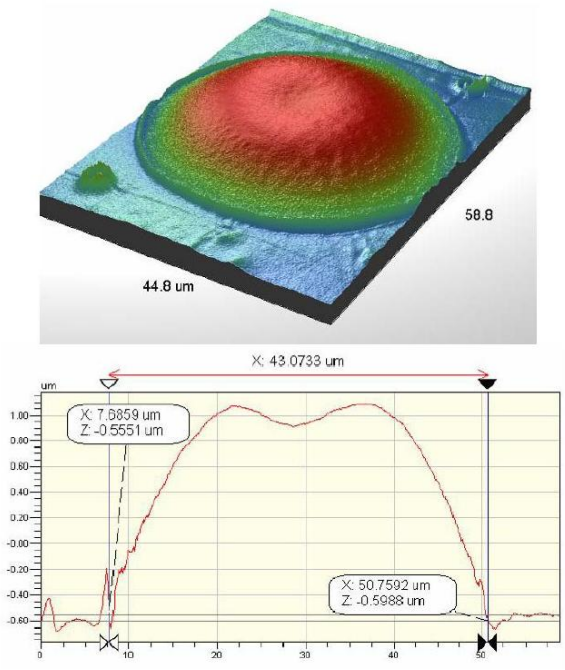


Figure 11: 0.5% concentration of pretreatment chemical (Figure taken from Matti Mäntysalo and Pauliina Mansikkamäki,[9].)

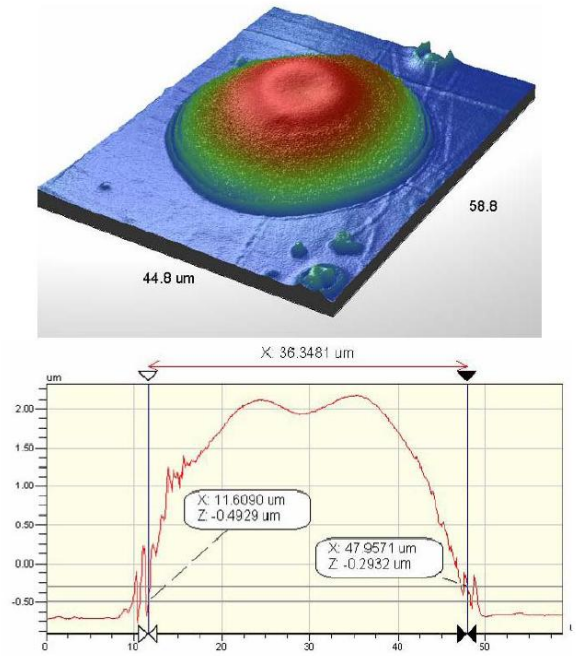


Figure 12: 10% concentration of pretreatment chemical (Figure taken from Matti Mäntysalo and Pauliina Mansikkamäki,[9].)

The forming of the electrical circuit with ink-jet technology is based on low temperature sintering of nano-sized metal particles and dielectric fluids. The melting point of the nano-sized particles is significantly lower than the melting point of the bulk material due to increased number of surface atoms compared to inner atoms, and therefore interactions between the atoms diminish [12]. As previously stated, the silver nano-paste used in this study requires sintering temperature of 220-230°C for a period of one hour [13], which will introduce a strong thermal stress for the components. In order to reduce heat stresses different sintering methods, such as laser or microwave sintering can be used [14-16]. Figure 13 shows an example of an encapsulated component with its first level interconnections below.

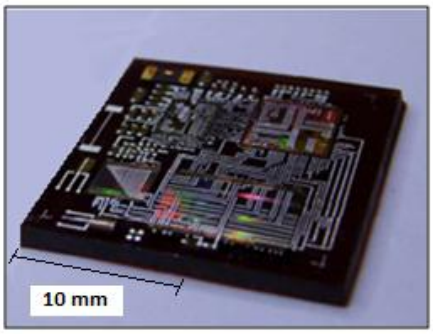


Figure 13: First level of inter-connections using inkjet printing (Figure taken from Matti Mäntysalo and Pauliina Mansikkamäki,[9].)

In addition to printing nano-inks for SiP's, application of functionalized structures printed with aerosol beams have been characterized and used for electrical connection of MEMS devices[17]. The IMSAS (Institute for Microsensors, Actuators and Systems) at University of Bremen, Germany developed an aerosol beam printed silver packaging approach for connecting a MEMS thermal flow sensor to its printed circuit board package as shown below in Figure 14.

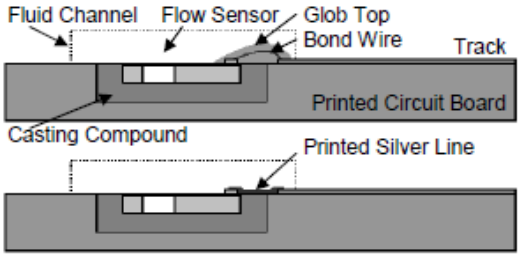


Figure 14: Wire bonding (top) and printed silver line (bottom) (Figure taken from Sturm, H., et al. [15].)

The figure above shows how the flow sensor was previously packaged with wire bonds however the glob top that encases the wire bonds created additional topographies. Therefore a printed silver line with aerosol nano-ink with particle sizes on the order of 50 nm down to 5 nm was used instead to package the sensor. The ink were developed based on different materials (e.g. silver), by using physical sputtering processes (VERL, Vacuum Evaporation on Running Liquids [18])

With this aerosol technology, it is possible to realize functional structures like electrical connections down to 10 μm trace widths and 1 μm trace thicknesses. The aerosol beam technology used, also known as Maskless Mesoscale Material Deposition (M3D) or Aerosol Jet was developed by Optomec and is based on a well defined aerosol jet of small droplets. In comparison to inkjet, the aerosol printing technology has a higher resolution and wider process latitude regarding resolution and stability of the inks shown below in Table 2.

Table 2: Processing results based on syringe, inkjet, and aerosol printing methods

Process results	Syringe Printing	Ink-Jet Printing	Aerosol Printing
Trace Width [μm]	125-200	20-100	10-20
Trace Height [μm]	20-30	3-10	1-5
Drop size [μm]	100-200	20-100	1-5
Standoff Height[mm]	0.25-1.0	1.0-2.0	Up to 5.0
Complexity	Low	Medium	Medium/High
Cost	Low ~5k	Medium ~50k-100k	High ~100k-400k

Furthermore, step heights of up to millimeters can be printed allowing three-dimensional aerosol printing technology. Due to different thermal expansion coefficients between the silicon sensor, printed circuit board and casting compound, cracks are likely to occur during sintering process and may cause defects in the printed silver line. The problem has been solved by using temperature stable printed circuit boards and casting compounds with adapted thermal expansion coefficients in combination with nano-scaled inks with sintering temperatures of 150°C. Below, in Figure 15, is a picture of the final package connecting the MEMS sensor to the printed circuit board package.

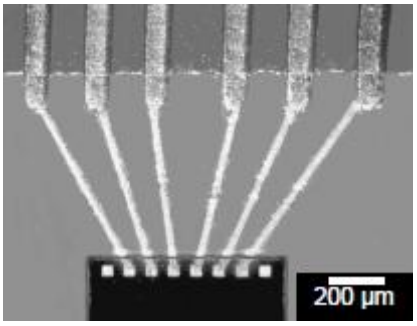


Figure 15: Packaged MEMS sensor in its respective package using aerosol deposition (Figure taken from Sturm, H., et al. [15].

1.3.4 Review

In this section, a few different packaging methods were introduced as well as the motivation for a flexible design. The novelty of the work, being the large array of sensors, low surface topology and semi-flexible configuration was outlined. The history of acoustic sensor packaging was described from its earliest roots in the mid 1950's and other packaging approaches were highlighted and represented throughout the background section. Next, the conductive ink packaging method that was used to package a MEMS shear sensor will be explained.

Chapter 2

2. Low Profile Packaging Method 1: Conductive Ink Packaging Setup and Approach

In this chapter, a semi-automated conductive ink process used for packaging MEMS devices is described. The method is applied to packaging MEMS sensors for wind tunnel testing. The primary advantage of this method is a reduction in surface topology between the package and the integrated MEMS sensors. In this chapter, the relationship between trace dimensions, resistivity, and deposition parameters such as pressure, tip diameter, stage velocity, and the distance the syringe tip is to its substrate is explored. Using this procedure it is possible to generate interconnect between the PCB and the MEMS sensor with a topology of less than 25 µm and widths of less than 150 µm.

2.1 The Dispensing System and Conductive Ink Motivation

The previous packaging approach, which is similar to other methods commonly used for packaging MEMS sensor chips, uses gold wire bonds with potting epoxy fill. For this application, a minimum surface topology of approximately 100 µm was achieved. For large arrays of MEMS microphones, yield issues were dominated by wire bond integrity problems. These two issues were the primary motivation for developing the low profile conductive ink process. The ability to produce low-profile connections easily and consistently is a critical component of the integration of MEMS devices into low topology packages. By optimizing the flow characteristics of the conductive ink through the syringe, the velocity of the micro-

positioning stages, the pressure of the syringe pump, and the distance the syringe tip is from the package, the height of the silver traces can be reduced to fewer than 25 µm in order to achieve low profile, low resistance, and versatile connections for a wide variety of applications. The conductive ink process is low cost, uses inexpensive equipment, and compatible with circuit integration because of the low temperature processing.

Some applications include the production of active and passive components such as transistors, resistors, capacitors, diodes, and even complete circuits such as RFID tags, keypads, sensors, and electrodes, as well as backplanes of organic light-emitting diodes (OLEDs) and other electroluminescent displays [19].

For a high level overview, a block diagram is shown below in Figure 16 highlighting the different parts of the system and how they are integrated within one another to form the conductive ink printing system.

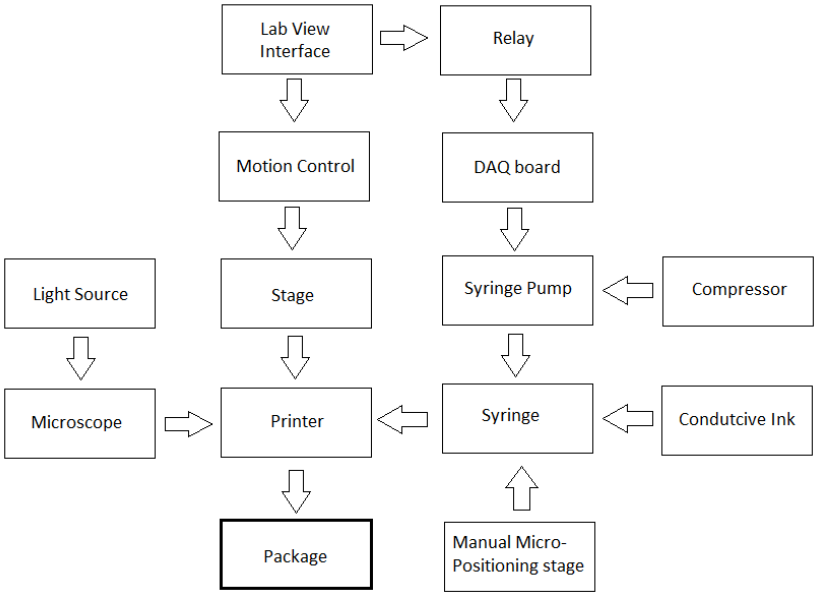


Figure 16: Block diagram of the conductive ink printing system

2.2 The Dispensing System and Conductive Ink Setup

The conductive ink process consists of a low profile, low volumetric resistivity silver conductive ink [125-13], Creative Materials, Ayer, MA which is pneumatically dispensed from a syringe between the pads of the printed circuit board package and its integrated sensor. The ink was chosen for its small particle size and relatively low viscosity properties which allow for high resolution lines. This ink is typically used for high resolution screen printing. The package and sensor are placed on a rubber O-ring, clamped down by four spring clips, and mounted to an aluminum fixture on top of computer controlled micro-positioning stages for accurate and precise placement of the silver traces as shown in Figure 17 and Figure 18 below.

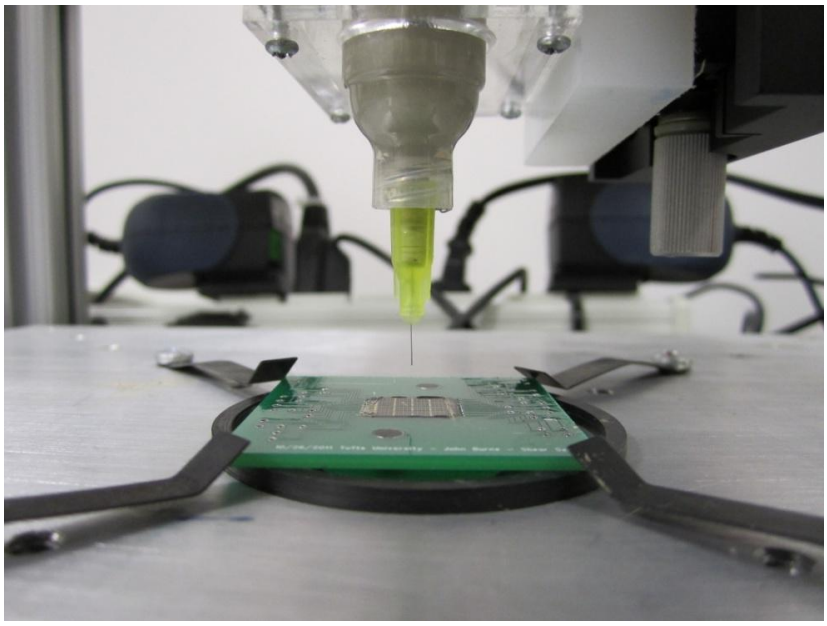


Figure 17: Conductive ink dispensing setup with syringe and package on top of aluminum plate

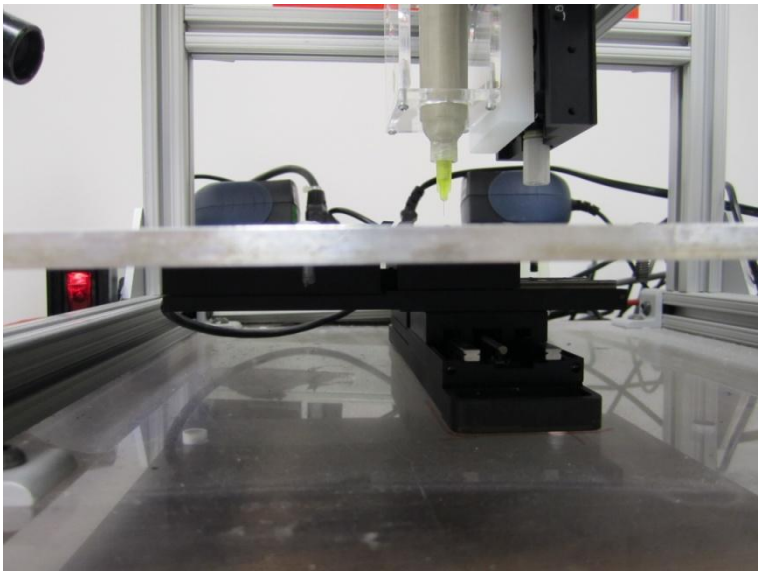


Figure 18: Micropositioning stages in the X,Y directions below the conductive ink and aluminum stage

The syringe press fits into an acrylic fixture hanging above the aluminum stage which can be adjusted up and down with the manual micropositioning stage located to the right of it. The syringe is attached to a pneumatic dispensing system which is controlled by a National Instruments data acquisition board and relay with logic from Lab View code written on the computer. The pressure of the automatic syringe pump is controlled with a portable pressure pumping system. This portable pressure pump is attached to the syringe pump through a quarter inch tube in order to manually control the syringe pump pressure up to 860 kPa.

The control end of the relay is attached to the Data-Acquisition (DAQ) board which supplies 5V to turn on and off the syringe pump which is attached to the switch end of the relay. This setup allows for the syringe pump to be controlled by a 5V digital output from the National Instrument device interfaced with the lab view software on the computer. The Lab View code interfaces with the DAQ board with a switch. When the switch is turned “On” in the graphic

user interface on the computer, it tells the DAQ to turn pin 6 on, which outputs 5V. The 5V is connected to the coil of the relay, which activates the switch that is connected to the syringe pump. This powers the pump and dispenses the silver ink. This setup is shown below in Figure 19.

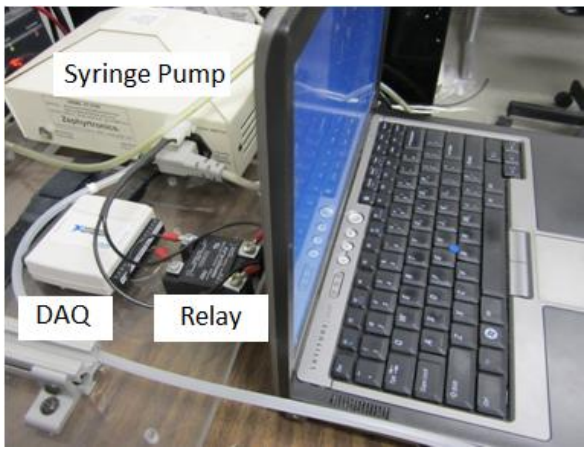


Figure 19: Syringe pump integration with Lab View

Finally, a microscope is hovering over the conductive ink tip which is mounted to an adjustable stand with a light as shown below in Figure 20. This is necessary when drawing fine lines on such small pads. The goal is to manually drive the stages so that the syringe tip is hovering over the pad on the sensor. This value is recorded on the Lab View display for the micro positioning stage controller. The tip is manually driven to the next pad while still looking under the microscope for accuracy. Once this final measurement is recorded, the total distance the stages are to travel is set in order to dispense from one pad to the next.

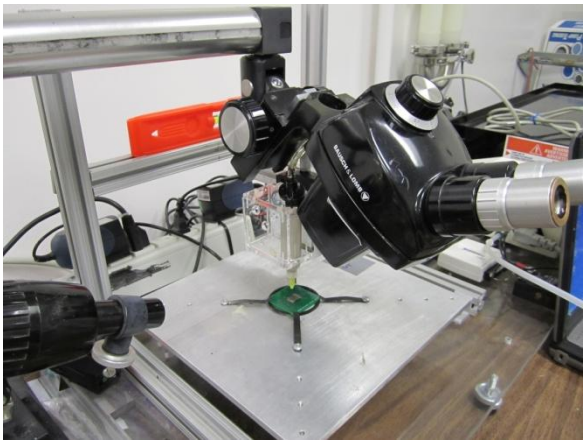


Figure 20: Microscope setup with light source

2.3 Process Flow Steps for Packaging Acoustic Sensors with Conductive Ink

The detailed steps to packaging a MEMS acoustic sensor with conductive ink and its PCB package are shown below in Table 3. There are some challenges with the process; however successful embedding of the sensor using epoxy without any damaged sensor membranes and low profile connections have been exemplified. Some of the main challenges are consistently getting planar surfaces between the MEMS die and its package with the epoxy. A stencil has been developed in order to help with the consistency of the adhesive film cutout before the epoxy is poured from the backside. If there is any large surface topology (>15 µm) between the package and the sensor, the tip from the syringe will have trouble dispensing a continuous line of ink. Therefore the surface must be close to planar as possible. A graphical representation can also be seen below is Figure 21.

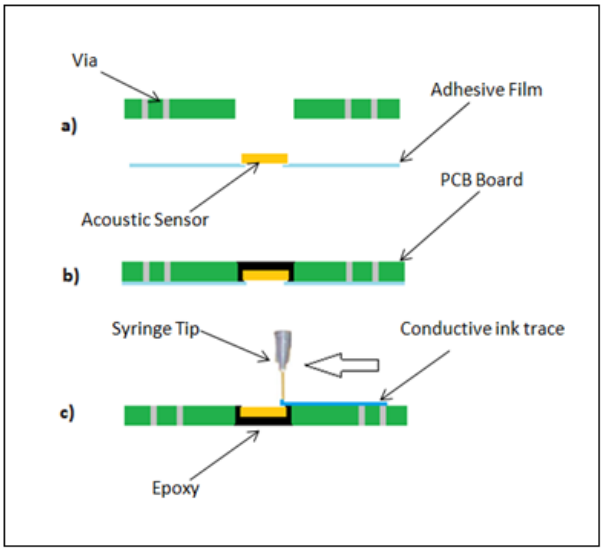


Figure 21: Overview of the conductive ink packaging approach

Table 3: Process flow for applying silver conductive ink interconnects

Step Name:	**Parameters:**	**Measurements/Comments:**
1. Cut the PCB package for MEMS microphone array and MEMS shear sensor		Draw a straight line across the package with a marker, and run it through the band saw to split it in half in order to have one of each package type.
2. Film Preparation	**ProFilm:DX266C** Cut out 75 mm by 75 mm of the ProFilm dicing tape	Peel off release sheet of the dicing tape and place on the front-side of the PCB package.
3. Double sided tape placement	**Intertape:** Cut off small pieces of the double sided tape	Peel off the release film (so that both sides are adhesive) and place small strips on all sides of the square cutout stencil so that the PCB can adhere to it.

4. PCB Board placement		Place PCB (face down) with the adhesive film onto the double sided tape on the stencil, so that the ProFilm tape is adhered to the double sided tape.
5. Cut a hole in the ProFilm dicing tape	**ProFilm:DX266C**	Cut out a hole in the tape on the PCB board with a razor from the stencil side using the edges of the stencil as a guide.
6. Released Acoustic MEMS sensor Placement	Note: Released membranes	Place MEMS sensor (face down) in the center of the milled out section on the PCB board so just the edges are touching the tape. Make sure the tape is fully wetted to the surface of the edges of the tape.
7. Use two part epoxy to encapsulate	**LOCTITE Fixmaster Fast Cure Poxy Pak** Epoxy is a 2-component, room temperature curing epoxy adhesive	Pour epoxy on the backside of the sensor die until the cavity is fully filled. It will cure at room temperature after 45-60 minutes.
8. Loctite epoxy cure	**LOCTITE Fixmaster Fast Cure Poxy Pak**	Wait 45-60 Minutes for the epoxy to fully cure.
9. Peel off ProFilm adhesive	**ProFilm:DX266C**	Remove the adhesive film from the PCB board carefully making sure not to disturb the active layer on the MEMS device.
10. Thaw Conductive Ink	Conductive ink for fine line screen printing. (**Creative Materials 125-13**)	Leave at room temperature for 120 minutes or until silver is re-suspended.
11. Attach the pump		Attach the syringe pump to the conductive ink.
12. Attach the tip	50µm inner diameter tip.	Place the yellow tip into the luer lock on the syringe.
13. Place the ink into the dispensing system	(**Creative Materials 125-13**)	Plug the tube of ink into the acrylic holder above the aluminum stage.

14. Place the package below the ink		Place your package on top of the rubber O-ring and secure the PCB with the metal spring clips.
15. Lower the syringe tip	~0.25mm from the surface of the package	Using the manual micro positioning stage attached to the syringe holder, adjust the height of the tip to .25mm from the package
16. Turn on the power strip		Turns on micro-poisitioning stages, pressure pump, syringe pump, microscope light, and DAQ board.
17. Draw your interconnects	Load "**Conductive Ink Code**" on the desktop of the computer	Use the Graphic User Interface in Lab View to draw the lines of conductive ink. You may also use the foot pedal for manual dispensing when needed.
16. Cure the conductive ink		Slowly bring heat up to 100 degrees C for 5 minutes on the hot plate, and then slowly bring heat up to 150 degrees C for another 5-10 minutes. For the best properties, bring up to 170 degrees C to 180 degrees C for several minutes.

A full analysis of the packaging has been explored, along with proven results for packaging a sensor; however there is room for improvement. Recent efforts have been made to make this process more repeatable by eliminating as many variables as possible to ensure consistent results. Further development could be done to optimize the velocity of the stages as a function of ink dispensing and to integrate camera vision software in order to visually click on the connections to further provide a user-friendly system. Also improving the workflow and usability of the system to ensure reliable results from user to user are currently being looked into.

Chapter 3

3. Low Profile Packaging Method 1: Conductive Ink Packaging Characterization and Results

Multiple parameters were explored in order to optimize a process by which the conductive ink is deposited to package a MEMS acoustic sensor. A test matrix was produced, starting from reasonable baseline parameters, in order to characterize the parameters by which the conductive ink was deposited. These baseline parameters were varied both above and below the baseline in order to test a range of values for characterization. With each parameter varying one at a time, it allowed the system to be analyzed on a parameter by parameter basis.

3.1 Test Board Matrix Characterization

A test board was designed with varying lengths in between pads as shown in Figure 22 below.

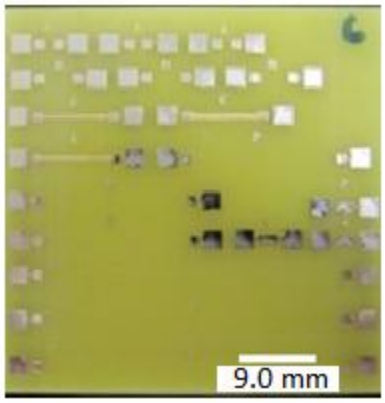


Figure 22: One of six test boards used for varying different parameters.

The test matrix consisted of thirteen tests varying the stage velocity, syringe tip diameter, syringe pressure, tip distance from the package, and interconnect length from the baseline case shown in

Table 4. Each parameter was varied individually above and below the baseline parameters with a total of two lines drawn for each test scenario. After all the tests were complete, the conductive ink was partially cured at 150°C on a hotplate in air for five minutes and then raised to 180°C for one minute to complete the cure. Next, the resistance was measured on each of the traces using a digital multi-meter and hand probes. Since the pads on the test board themselves have added resistance, a connection on the board was made with both pads fused together in order to subtract their resistance from the resistance of the silver ink when measured. The surface profile of the ink was measured using a stylus profilometer. Three measurements were taken along the conductive ink trace in order to check for variation in trace height and width.

Table 4: Baseline parameters for test matrix.

Baseline Parameters	**Measurements**
Stage Velocity	0.75 mm/sec
Syringe Tip Inner Diameter	0.125 mm
Syringe Pressure	415 kPa
Tip Distance from Package	0.5 mm
Trace Length	9.0 mm

3.2 Results

Each of the test parameters were plotted versus resistance, trace height, and trace width to determine which the best set of parameters was in order to achieve the lowest profile and lowest resistive traces. The resistance measurement plot as a function of line length as shown in Figure 23 shows the resistance measurements with a best fit linear trend. Therefore, the length of each trace from the pad of the sensor to the electronics was minimized as much as possible.

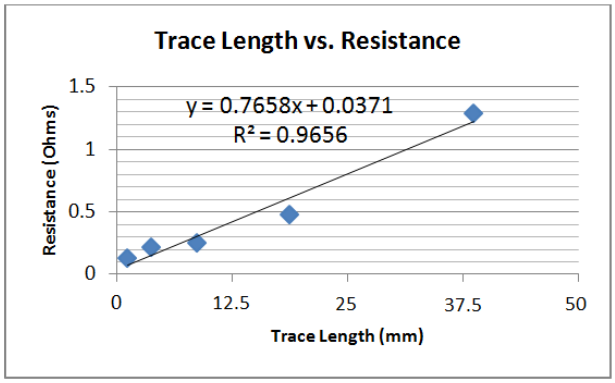


Figure 23: Trace length versus resistance plot

The plot of tip diameter versus resistance shown in Figure 24 was particularly interesting because it showed how the cure temperature is very sensitive to the size of the cross sectional area of the trace. Since the trace width and height for the smallest tip diameter was so small, the amount of time needed to cure the ink was less than the largest tip diameter. With that said, the traces with a larger cross sectional areas need to be cured for a longer period of time to completely drive off all of its solvents.

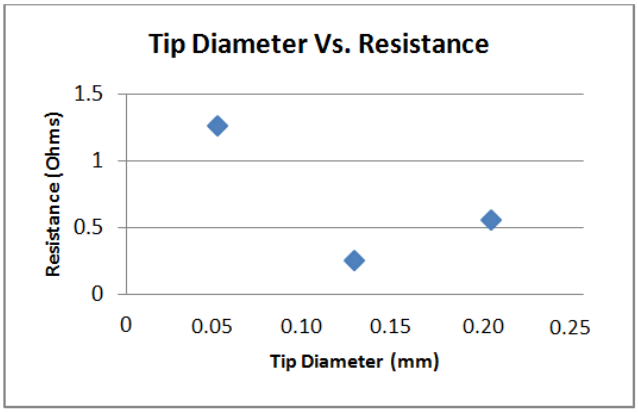


Figure 24: Tip diameter versus resistance plot

The distance the syringe tip was from the package had a large effect on how wide, how tall, and even if the tip would deposit at all, shown in Figure 25. For the baseline case at distances of 0.25 mm and 0.5 mm away from the package, the trace height was roughly the same, but when the tip was moved to 0.75 mm away from the package, the trace nearly doubled in height. However, if the tip was away from the package by more than 0.75 mm with the smallest syringe tip, then the ink would not even deposit on the package at all. A manually adjustable micro positioning stage needed to be added to the design in order to accurately adjust this critical setting.

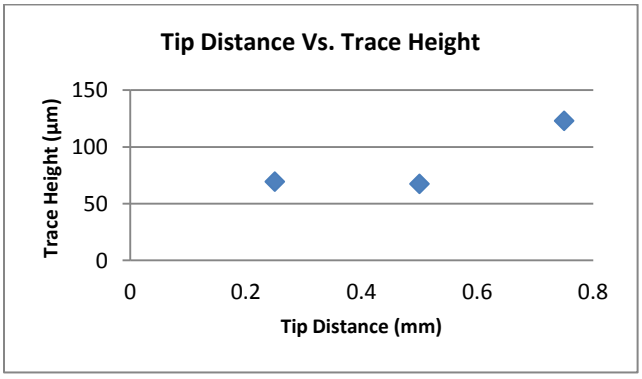


Figure 25: Tip distance versus trace height plot

As expected, the height of the traces decreased as the velocity increased as shown in Figure 26 and the change in height of the traces was much greater from 0.25 mm/s to 0.75 mm/s than from 0.75 mm/s to 1.25 mm/s. Depending on the size of the trace being drawn, the velocity needed to be calibrated accordingly; otherwise if the tip size is too small and the velocity of the stage is traveling too fast, then the traces will not be completely continuous. This is the reason for choosing smaller values for the velocity of the stages for smaller syringe tips.

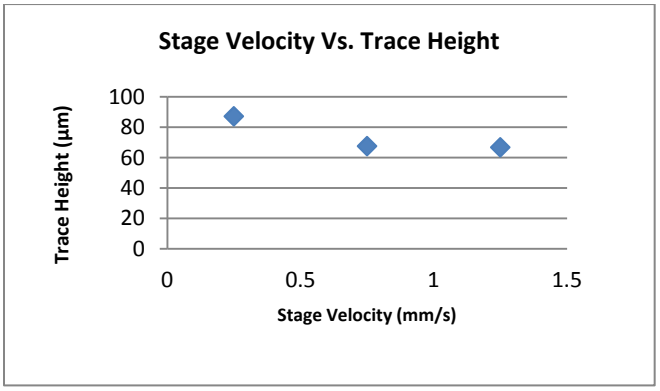


Figure 26: Stage velocity versus trace height plot

The graphs shown in Figure 27 and Figure 28 show the direct relationships between increasing the tip diameter and increasing the syringe pressure as a function of trace height. These were the two largest driving factors for increasing or decreasing the cross sectional area of the traces. Since the sensor would read more accurately with low profile traces, these parameters were minimized as much as possible. For the smallest syringe tip, pressures below 240 kPa would not dispense any conductive ink, so 240 kPa was the ideal operating pressure for drawing the lowest profile traces.

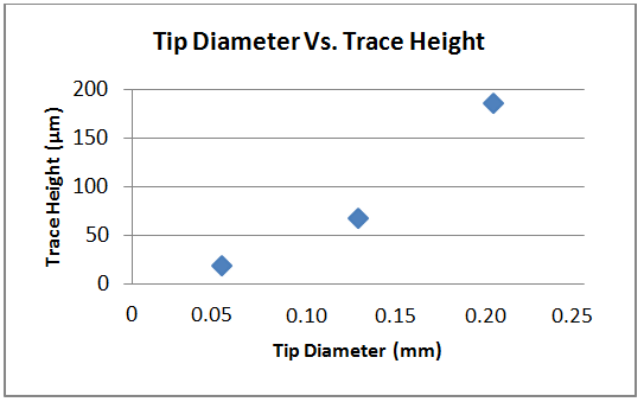


Figure 27: Tip diameter versus trace height plot

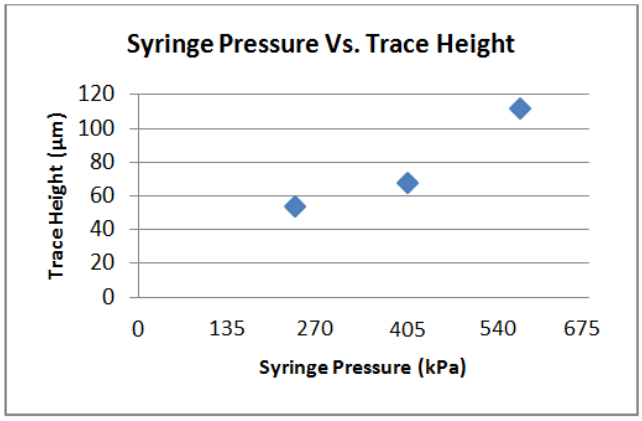


Figure 28: Syringe pressure versus trace height plot

The profilometer measurements of the individual traces showed a greater percent thickness variation the smaller the traces drawn. As shown in Figure 29, which was drawn with an inner tip diameter of 125 µm , the thickness only varied from 550 µm to 521 µm. For the trace width with inner tip diameter of 50 µm, it varied from 212 µm to 151 µm. This is attributed to the particle size of the silver ink. The smaller the trace that is drawn, the greater the impact of particle size. Since the particle size of the ink is only slightly smaller than the diameter of the syringe tip, a greater pressure must be used in order to dispense the ink at the same feed rate thus making it harder to control uniformity.

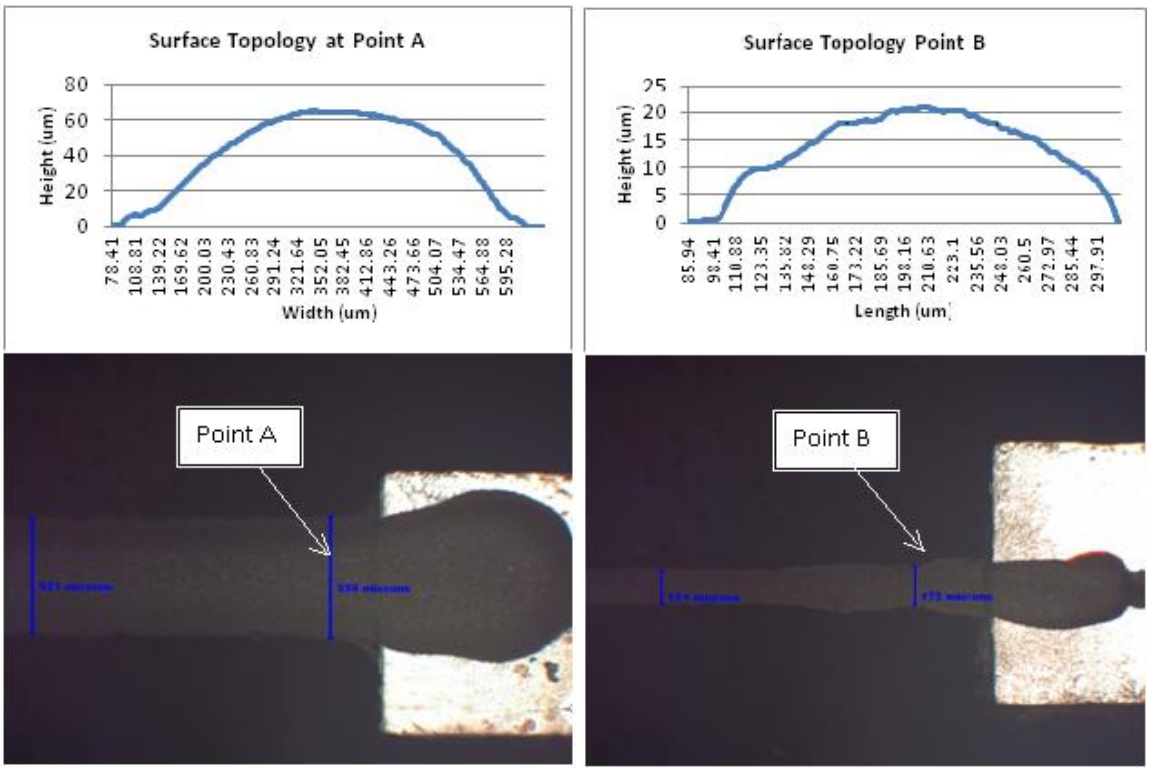


Figure 29: Surface topology measurements for different syringe tip sizes

After the resistance and surface topology of the conductive ink were fully characterized, they were then compared to the wire bonded hybrid packaging schemes that had previously been used. The height of the wire bond is roughly 100 µm tall as shown in Figure 30. The largest motivation towards developing a new package was to reduce this surface topology in order to keep all connections within the viscous sublayer of flow. After characterizing the conductive ink process, the average height of the traces drawn with the smallest tip was 18.86 µm, which ultimately reduces this critical dimension by a factor of 10.

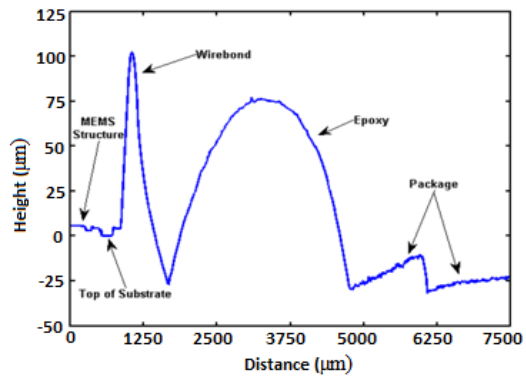


Figure 30: The profilometer measurement of the wire-bond packaging scheme

Figure 30 shows the entire package that connects to the MEMS structure. There are numerous other surface protrusions in addition to the wire bond, which can be minimized. One of the other packaging techniques incorporated with the conductive ink process is minimizing the topology associated with the epoxy. A square piece of dicing tape with a cutout in the middle to avoid sticking to the released MEMS structure is placed over the PCB package so that just the edges of the MEMS sensor stick to it. This allows for the epoxy to fill the backside of the package without seeping over the released membranes. A stencil was laser cut in order to get a consistent cutout for the dicing tape that fits onto the edges of the sensor every time.

Finally, the resistivity of the conductive ink was calculated using equation 1 to be $8.5 \cdot 10^{-5}$ $\Omega \cdot$ cm where ρ is resistivity, R is resistance of the trace, A is the cross sectional area, and l is the length.

$$\rho = \frac{RA}{l} \tag{1}$$

The cross sectional area of the conductive ink was calculated by taking the integral under the surface profile in Matlab. The resistivity of the material at the specific cure time used was roughly double that of what was reported in the data sheet, which was $4 \cdot 10^{-5}$ $\Omega \cdot$ cm. This

difference in resistivity is attributed to the cure time. In comparison, the measured resistance of a gold wire bond was 9 Ω for a 1.5 mm long, and 25 µm diameter wire, including contact resistance.

After characterizing the conductive ink process, an acoustic sensor was packaged into a printed circuit board in order to reduce all surface topology to below 25 µm and demonstrate the conductive ink system. The optimal parameters to package an acoustic sensor, with our design, is with a tip diameter of 0.05 mm, 0.25 mm from the package, at 240 kPa, with a 0.5 mm/s stage velocity, and at the smallest length possible in order to reduce resistance. After packaging an acoustic sensor using the conductive ink process, the traces were all able to be precisely placed on each of the pads as shown in Figure 31, 32, and 33.

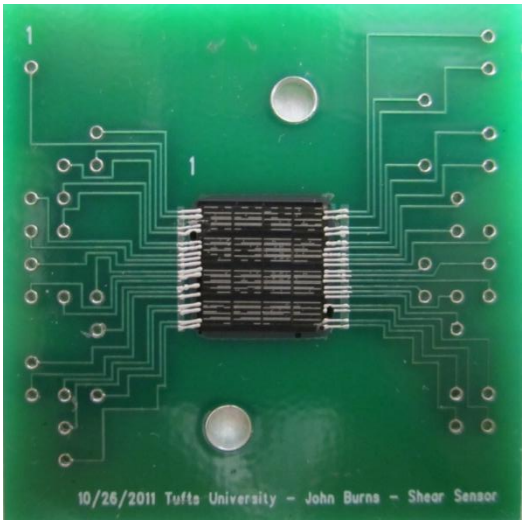


Figure 31: Packaged dummy shear sensor

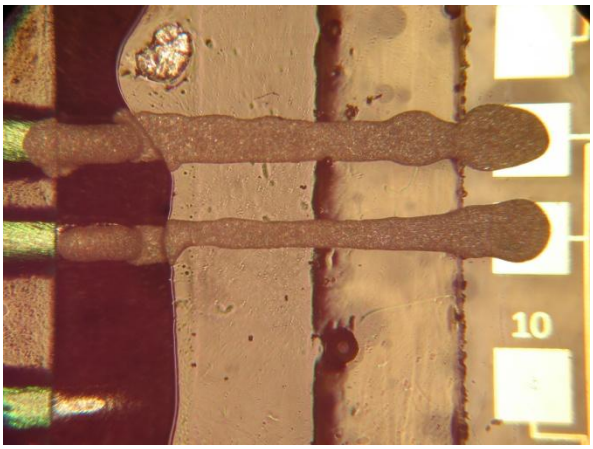


Figure 32: Individual connections successfully deposited from pad to vi

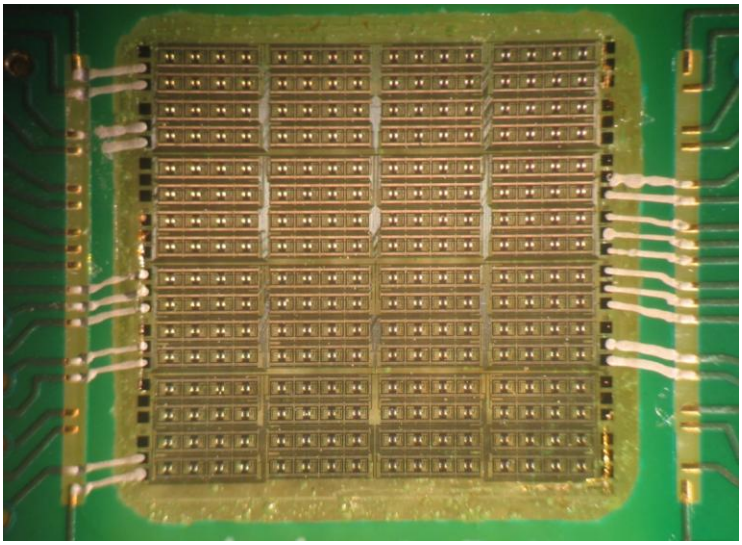


Figure 33: Packaged live MEMS shear sensor with conductive ink approach

3.3 Conductive Ink Packaging Review

These conductive ink methods for packaging acoustic sensors prove to be very useful, especially from a yield, low resistance, low cost, and surface planarity standpoint. There are many different applications where controlled placement of conductive ink proves to be useful as

previously described, and only one specific application was explored in this paper. The limiting factors for producing even smaller traces using conductive ink is the diameter of the tip that is used to dispense the ink, particle size of the silver ink itself, and critiquing automation for repeatability in order to further optimize the process controls. For interconnects with an order of magnitude less than 10 µm of topology, other packaging methods should be explored. For example, MEMS processes for photo-defining the traces, which will be further explored in chapter 4.

Chapter 4

4. Low Profile Packaging Method 2: Integrated-Ultra High Density Packaging Setup and Approach

In order to achieve an order of magnitude less in surface topology than the conductive ink approach, an integrated-Ultra High Density packaging design from Draper Laboratory was pursued. An integral part of the i-UHD design includes thin dielectric/metal deposition and photo-defined layers for high resolution to achieve low profile connections between the pads on the sensor and the through silicon vias.

4.1 Integrated-Ultra High Density Motivation

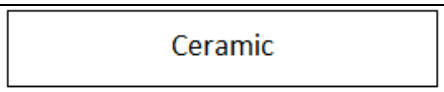
The i-UHD process offers many capabilities that both the conductive ink process and the wire bonding process for packaging acoustic sensors do not provide. For this thesis project, one of the main goals was to be able to accommodate a vibrating MEMS structure inside of the current packaging scheme while also being able to achieve the theoretical maximum packing density for a heterogeneous process. Some of the other benefits of the i-UHD process are as follows. Firstly, with a laser cut ceramic wafer, unique encapsulation process for embedding the MEMS sensor, and sputtered metal layers used as interconnect, the i-UHD package has less than 5 µm of surface topology. Secondly, when grinding the backside of the wafer to expose the TSV connections, the total thickness of the package is 125 µm, which offers flexibility for mounting to non-planar surfaces. Thirdly, the package offers the ability to embed large arrays of sensors with hundreds and even thousands of microphone elements for a larger spatial resolution and larger array aperture for characterization. Finally, the i-UHD process could incorporate all the

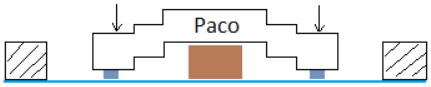
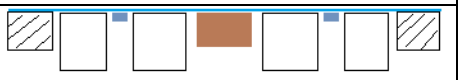
electronics, in bare die form, into the same cavity as the sensors themselves reducing electrical noise effects and bulky electronic modules.

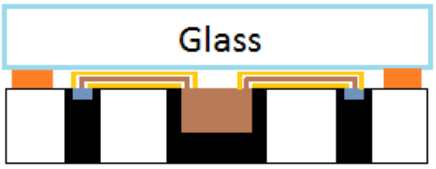
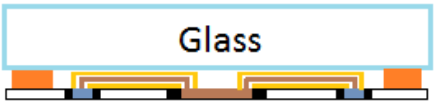
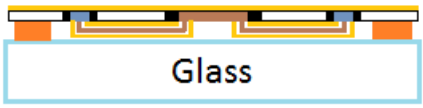
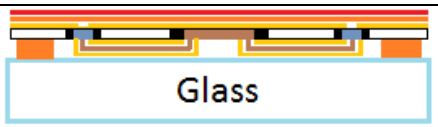
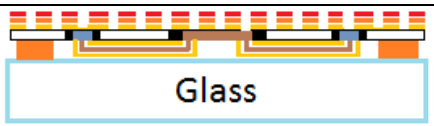
4.2 Integrated-Ultra High Density Process Steps

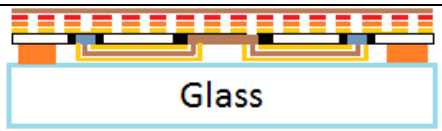
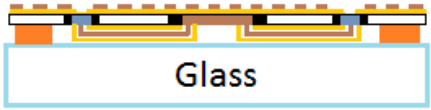
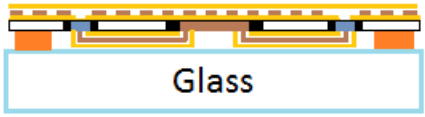
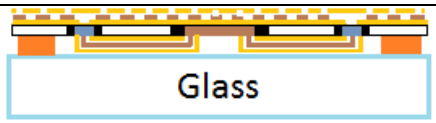
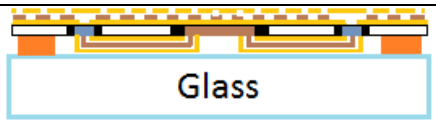
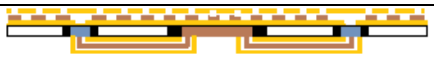
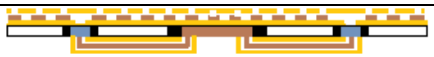
When designing the package for integrating a MEMS sensor into the i-UHD platform, a few decisions had to be made. Firstly, the MEMS sensor either had to be released before the process steps or after its integration. The decision was quickly made to release the sensor after each of the processing steps, otherwise peeling off films, dicing out the final module, and processing dielectric layers on top of the microphones would have contaminated, disturbed, or even broken the membranes. Secondly, if the sensor was to be released after integration, the entire package had to be compatible with the aggressive 30 minute 4:1, HF:HCl release etch. Therefore materials such as ceramic, chromium, gold, and the Draper's proprietary spin on dielectric photo-sensitive dielectric were the basis of the design. Lastly, in order to process a signal out of the sensor, the electrical effects of the mechanical design such as noise, stray capacitance, and resistance had to be reduced. Table 5 below outlines a high-level graphical process flow highlighting any major steps.

Table 5: High level process flow highlighting the major steps

Step Name:	Measurements/Comments:	Graphic Representation
1. Starting Substrate (Ceramic)	100mm 99.6% Alumina, 1000µm thick wafers. (Major and minor flat included)	
2. Laser cut the ceramic wafers	Create a Solidworks model to send out of house for laser cutting.	

3. MRSI Pick and place tool	Place the 3 Acoustic sensors (gold square ~580 µm thick) and the 12 TSVs (blue square ~150 µm thick) Reference fiducials on the mask to the center location on the die.	
4. Die Seating, using conformal "Paco" pad alignment	Heat chuck on the encapsulation tool to 90C. Wait until the die are fully "wet" to the acrylic adhesive; applies uniform axial pressure across the die.	
5. Cavity wafer placement	Align cavity wafer with the die, and combine both together.	
6. Encapsulation	Using new encapsulation tool, apply epoxy over backside of cavity.	
7. Encapsulant Removal	Clean off MRSI chuck with acetone, peel off Teflon film.	
8. Pre-Cure	80C for 120 mins then let cool to < 45C before final cure.	
9. Final Cure	165C for 120 mins then let cool to <50C.	
10. Spin 8µm dielectric layer		
11. Expose photo dielectric	Expose, develop, post-develop exposure, post develop bake, oven bake.	
12. For liftoff process, spin on liftoff resist and photoresist		
13. Expose and develop	1-Dehydrate 2-Spin Resist, 3-Expose 4-Develop 5-Postbake.	

14. Sputter Cr/Au	1000Å Cr, 5000Å of Au	
15. Liftoff	PG Remover, 10 mins Spin Rinse Dry	
16. Spin 8µm dielectric layer. (Mask layer for HF release etch)	Spin on dielectric, expose, develop, post-develop exposure, post develop bake, oven bake.	
17. Expose photo dielectric	Expose, develop, post-develop exposure, post develop bake, oven bake.	
18. Mount to a handle wafer	Bond glass handle wafer with polyimide spacers.	
19. Thin Backside of substrate	Thin down using thinning process traveler. (Lapping tools, varying diamond slurries).	
20. Spin 8µm dielectric layer (Backside)		
21. Expose photo dielectric	Expose, develop, post-develop exposure, post develop bake, oven bake.	
22. For liftoff process, spin on LOR and photo-resist		
23. Expose and develop	1-Dehydrate 2-Spin Resist, 3-Expose 4-Develop 5-Postbake.	

24. Sputter Cr/Au	1000A Cr, 5000A of Au.	
25. Liftoff	Leaving pads and interconnect.	
26. Spin on 8µm dielectric layer		
27. Expose photo dielectric	1-Dehydrate 2-Spin Resist, 3-Expose 4-Develop 5-Postbake soldermask layer to hold conductive epoxy for electronics integration	
28. Singulate	Dice out individual module.	
29. Remove Glass Handle Wafer	PG Remover (10 mins) Spin Rinse Dry Hot Plate	
30. Release membranes	4:1 HF:HCL for 45 minutes.	
31. Coat with Parylene-C	Room temperature.	
32. Solder paste/Conductive Ink the backside	Place solder spheres on backside in order to reflow onto PCB board.	
33. Mount to electronics	Prepare for wind tunnel testing.	

4.2.1 Laser Cut Ceramic Wafer

The starting substrate is a ceramic wafer with laser cut cavities for both the MEMS microphone array chips and the TSVs. There are a total of 76 connections on the sensor itself which need to be rerouted to the backside of the wafer in order to mount onto the electronics. These TSVs provide the connection by which the metal trace gets transferred to the backside of the wafer. Each TSV contains 40 connections, so with 12 TSVs, we are able to add redundancy to each connection for all three sensors that get embedded. Redundancy is incorporated into the design by patterning the metal over two connections on the TSV as a factor of safety in case one of the connections of the TSV is damaged. The two small narrow cavities are for the 12 TSVs and the larger center cavity is for the 3 by 1 sensor array with 200 µm of separation between the dies to allow for the epoxy to hold it in place. Figure 34 below shows a Solidworks model of the cavities in the ceramic wafer, which was sent out to be laser cut by a high precision contracting company. The two main reasons for choosing ceramic over silicon was that its fracture toughness was four times that of silicon and its dielectric properties reduced any stray capacitance between materials. The reason the ceramic's fracture toughness is four times that silicon is because of its heterogeneous amorphous makeup as compared to a single crystal silicon wafer which fractures along crystallographic planes.

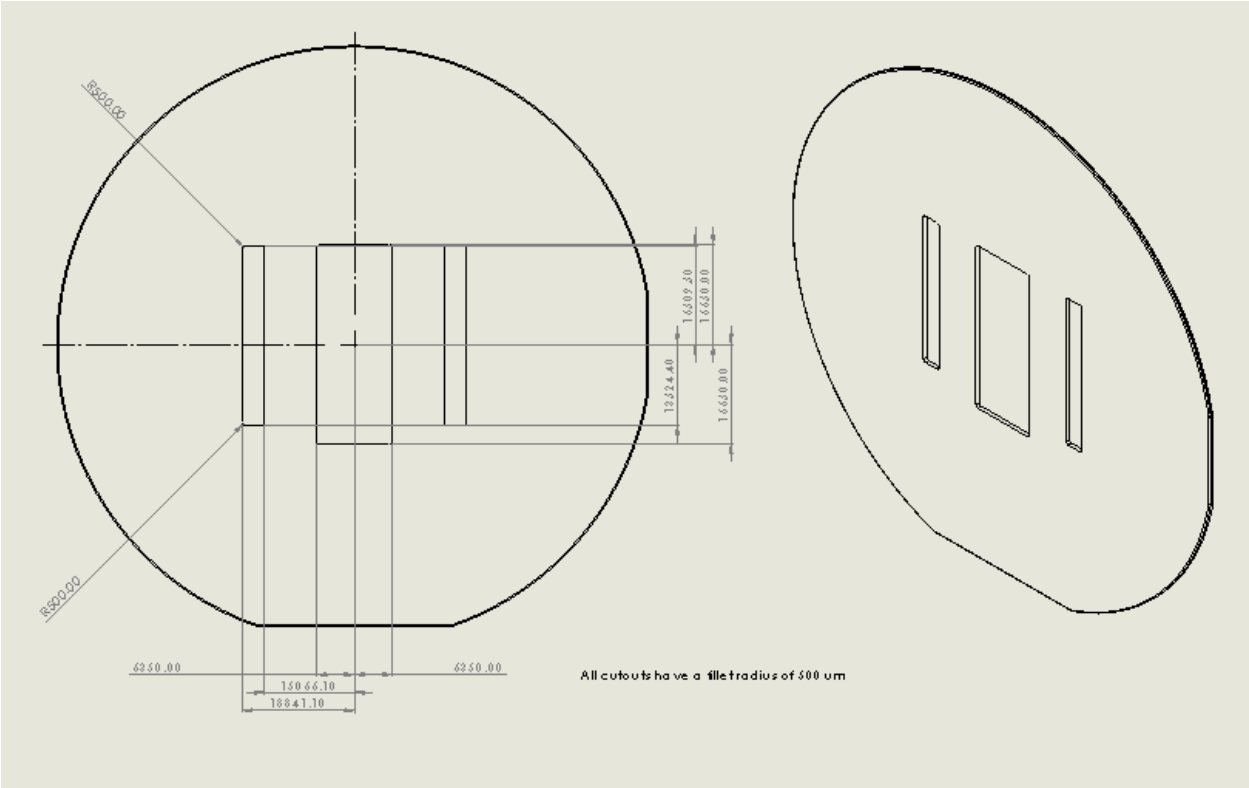


Figure 34: Solidworks model of the laser cut ceramic wafer with dimensions in µm

Initially, silicon wafers with laser cut through-holes were used, but they broke after curing the epoxy at high temperatures. Since the epoxy thermally expanded and contracted, this stress would propagate any cracks that initially formed from the laser cut silicon. Since the laser cut silicon created a large void in the wafer, there was nothing to support these areas or prevent cracks from propagating. A modification to this packaging approach etches a cavity with posts on the front-side and a fill port on the backside leaving a “web-like” structure to prevent the silicon from cracking. For this design, where a through-hole was desired, a wafer with increased fracture toughness (ceramic wafer) played an integral role when choosing the respective substrate for co-packaging.

4.2.2 Die Placement/Die Seating

After the substrate was laser cut and cleaned, an acrylic adhesive film was prepared in order to place the TSVs and MEMS sensors in their respective locations. A pick and place tool accurately places these die on the adhesive film face down so when the film is peeled off after encapsulation, the surfaces of the die are exposed to the environment. A placement file was created in Excel in order to reference locations on the dies with respect to fiducials on the die placement mask. This allowed the placement tool to be able to pick up the die at its center and precisely place it at its intended location on the adhesive film. After all the dies were placed in their respective locations, they were "seated" in order to wet the entire surface of the devices with the film so that when they were encapsulated, the epoxy would not seep over the pads of the sensor and contaminate the connection points. A picture of the sensor after seating is shown in Figure 35.

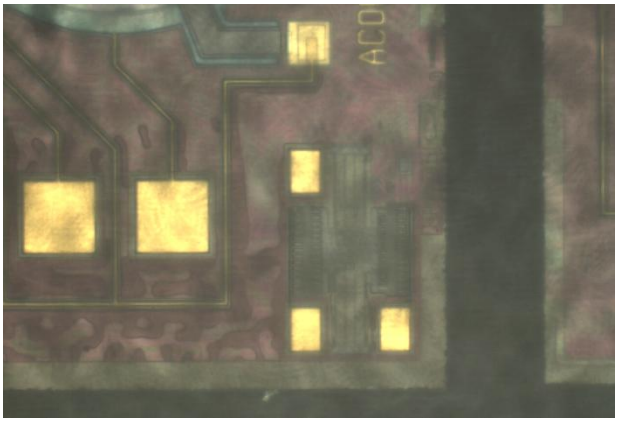


Figure 35: Picture of the wetted corner of the sensor after seating

Since the sensors were 575 µm thick, and the TSVs were only 150 µm thick, a thicker conformal pad was used made by Pacothane technologies in order to apply equi-axial pressure to the backside of the chips to ensure equivalent wetting across the dies. This "Pacopad" eliminates

air voids, inner-layer slippage and white corners or edges. Pacopads also reduce dielectric thickness variations, image and glass cloth transfer, and obviate the potential of low-pressure prepreg blisters. They are cellulosic-based product manufactured on a highly specialized paper machine, using virgin fibers, that guarantees a low density profile consistent across the entire area of the sheet. Once the uniform pressure is applied, the film is heated up to remove any thermal intrinsic stresses in order to relax the film for better adhesion. Finally, the film with the die are placed inside of the ceramic wafer with a aluminum fixture that can control the x,y and theta directions of the film for precise placement into the wafer as shown below in Figure 36. At this point, the wafer is ready to be potted with epoxy from the backside to mold everything into place.

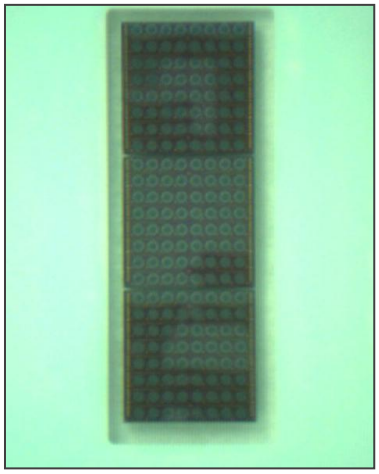


Figure 36: The 3x1 sensor array after placement into the cavity of the ceramic wafer

4.2.3 Encapsulation

Once the film is precisely placed over the ceramic wafer, it is loaded into a custom encapsulation tool in order to uniformly fill the backside of the wafer with epoxy and eliminate any surface topology on the frontside of the wafer after the film is removed. This step is critical in order to planarize the surface of the wafer so that the first layer has minimal surface topology. Since the sensor and TSVs vary in thickness, the shift of the die needs to be minimized in order for each lithography mask to align to its features. Also, the sensors and TSVs must adhere well to the film during encapsulation so that none of the epoxy penetrates the film thus contaminating the electrical pads. Figure 37 shows the pilot wafer after encapsulation with very little surface topology or die shift. The pilot wafer (containing one live acoustic sensor) was designed to go through each of the process steps before the live wafer (containing three live acoustic sensors) in order to resolve any issues before the live wafer was processed.

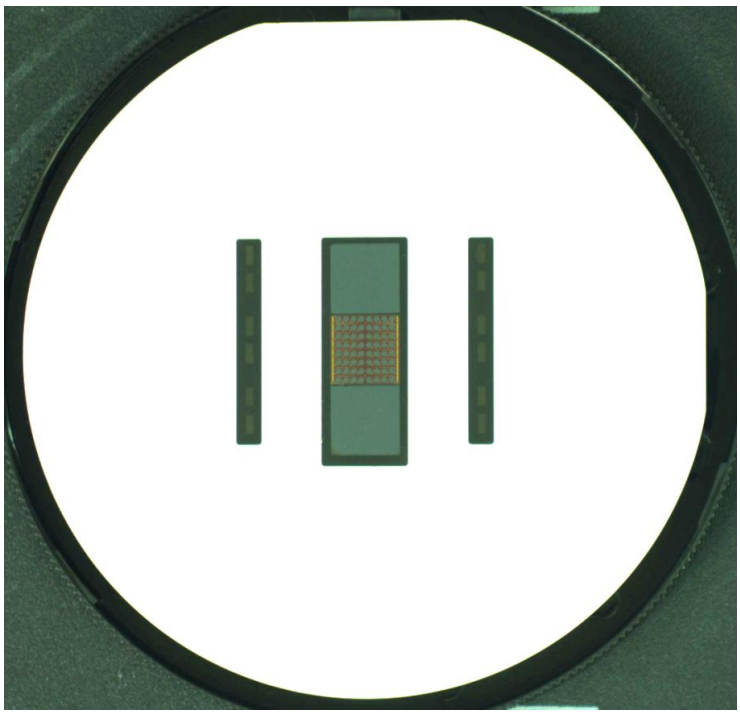


Figure 37: Full wafer after the pilot wafer was encapsulated

Wafer bow was another concern during processing that is measured with an interferometry tool. Depositing each layer bows the wafer due to its tensile stress pulling on the substrate. Especially when the wafer gets thinned to 150 µm with large cavities filled with epoxy, the wafer is easily bowed by adding layers of dielectrics/metals. The wafer bow increases as the ratio of epoxy to ceramic increases. For this design, wafer bow is not as much of an issue since the large pocket for the sensors in mostly filled up with thick silicon die, so the amount of epoxy is minimized. There is also the same number of layers on each side of the wafer, balancing the wafer out in terms of the amount of tensile stress pulling the wafer in one direction or the other.

Finally once the bow is measured and the epoxy is partially cured, a polish-back step is performed in order to remove the excess epoxy from the backside of the wafer. The wafer is mounted to a vacuum fixture to planarize the surface. Once this excess epoxy is removed, a final hardbake is performed in order to prevent the epoxy from expanding and contracting during subsequent processing steps.

4.2.4 Frontside Layer 1

The first layer on the surface on the ceramic substrate is a spin on dielectric photosensitive polymer which planarizes the surface and opens vias for metallization as shown below in Figure 38 and Figure 39. The thickness of this dielectric is roughly 8 µm, so if the surface has 2-3 µm on roughness, this dielectric layer is specifically formulated in order to help level it out.

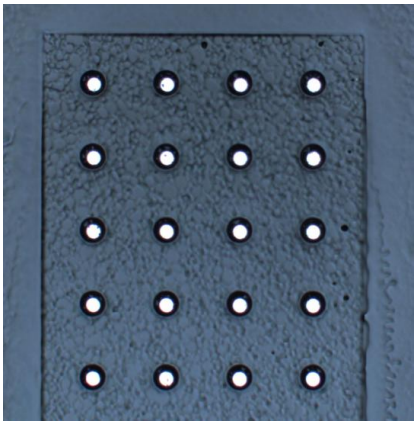


Figure 38: 1st layer patterned over the TSV

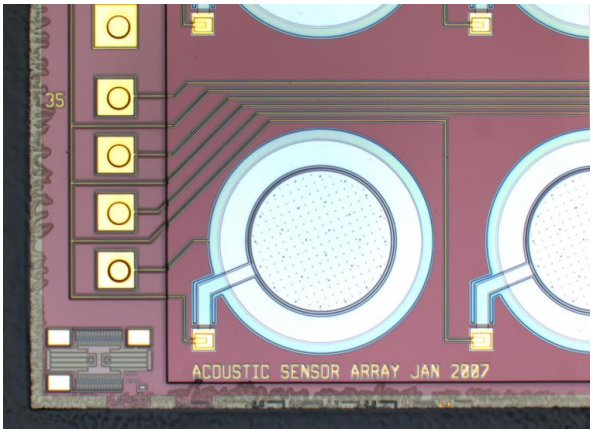


Figure 39: 1st layer patterned over the sensor

The mask was designed so that it would clear out any of the dielectric that deposited over the microphones in addition to clearing out any of the dielectric around the 40 mm by 40 mm module in order to reduce its effect on wafer bow. This was because the microphones needed to be released in 4:1 HF:HCl solution when the entire packaging process was completed. Tests were performed in order to ensure the photo-sensitive dielectric would not delaminate from the ceramic substrate by attacking the native oxide on top of the substrate. The undercutting of the HF:HCl solution on the photo-sensitive dielectric was measured to be 10-15 µm. With that said,

the design of the dielectric layers incorporated enough distance away from anything that would be affected by the aggressive release, such as the SiO_2 beads in the epoxy.

4.2.5 Frontside Metal Layer 1

After the first layer was spun onto the wafer and patterned, the first layer of chromium/gold was deposited. Chromium was deposited as an adhesion layer underneath the gold since gold is an inert metal which doesn't adhere well to most materials. A liftoff process was used when depositing the metal otherwise all of the gold connections on the sensor itself would have been etched away. The metal was sputtered in order to completely coat the 8 µm convex "step profile" that the first dielectric layer created on top of each of the TSVs and sensor pads. Since the metal was sputtered instead of evaporated, a lift off resist (LOR) was deposited underneath the photo resist in order to create a re-entrant profile for the deposited metal. Lift-off resists are based on polydimethylglutarimide. Their unique properties enable LOR products to perform exceptionally well when used either as a sacrificial layer, or as an undercut layer in bi-layer lift-off processing. Lift-off resists are designed for applications requiring high resolution imaging, easy process tuning, high yields and superior deposition line width control. The LOR is undercut after the photo resist is developed in order to create a profile from which the metal would lift off easily. The total thickness of the LOR and photoresist is the upper bound for allowable metal thickness. Since the total thickness of these two layers was 2 µm, the total thickness of both the chromium and gold was 0.6 µm. The metal lifted easily in solvents with ultra-sonics; however certain solvents were avoided due to swelling of layer 1. Small defects did appear on the metal layer 1, which were attributed to contamination on the mask either through particles or wafer handling, but could be reworked in order to separate two conjoining traces. A picture of the metal traces is shown below in Figure 40. It may appear as though the traces are

discontinuous over the edges of the cavity, but the metal is so thin it appears transparent. Continuity tests were performed by probing the pad of the sensor and the pad of the TSV in order to confirm the connection.

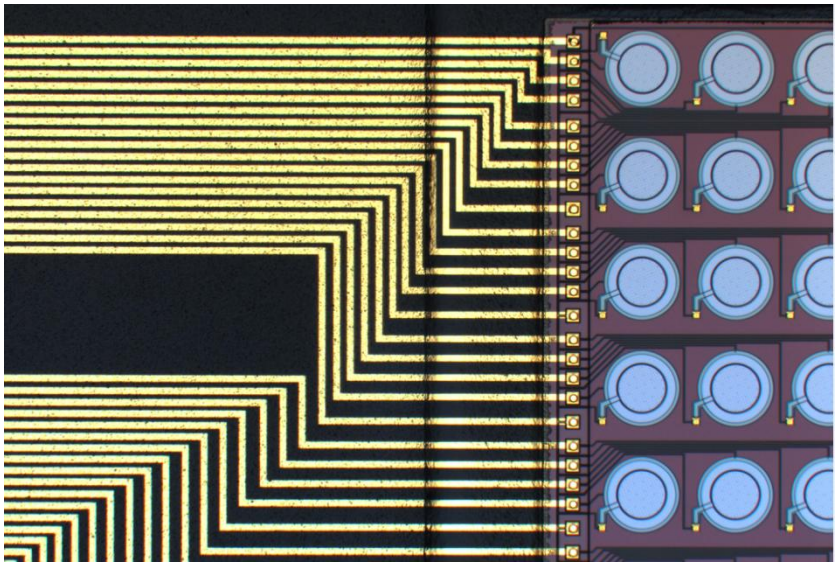


Figure 40: Chromium / gold traces running from the sensor to the TSV

Finally, metal lines for dicing were included into the mask in order to cut out the module when the processing is finished. A full wafer view of the sensors with dielectric layer and metal layer fully processed is shown below in Figure 41.

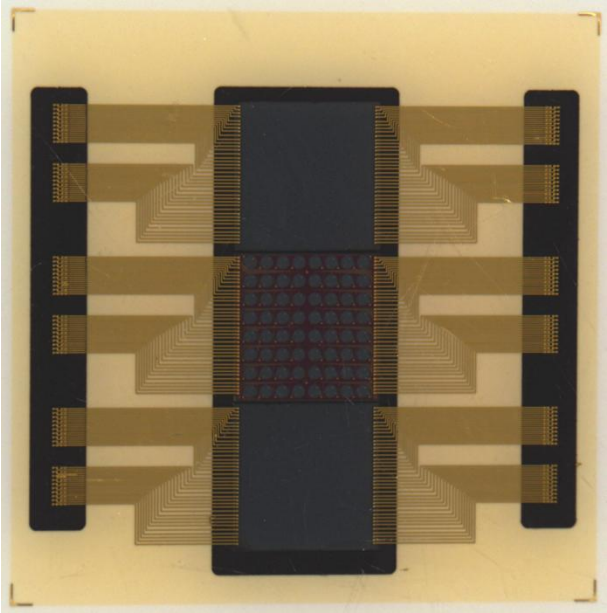


Figure 41: Full wafer view of the module after layer 1 and layer 2

4.2.6 Frontside Layer 3

After the metal layer was deposited on the front-side, it was still exposed to the environment, and therefore layer 2 served the purpose of sealing off the entire module and overlapping layer 1 in order to protect everything from the 4:1 HF:HCl release etchant. A picture of layer 2 overlapping layer 1 is shown in Figure 42. Layer 2 was designed to overlap layer 1 by 20 µm which is twice the distance that the HF solution was tested to penetrate its interface. Similar to layer 1, it was developed away from the sensor in order for the etchant to release the microphone membranes.

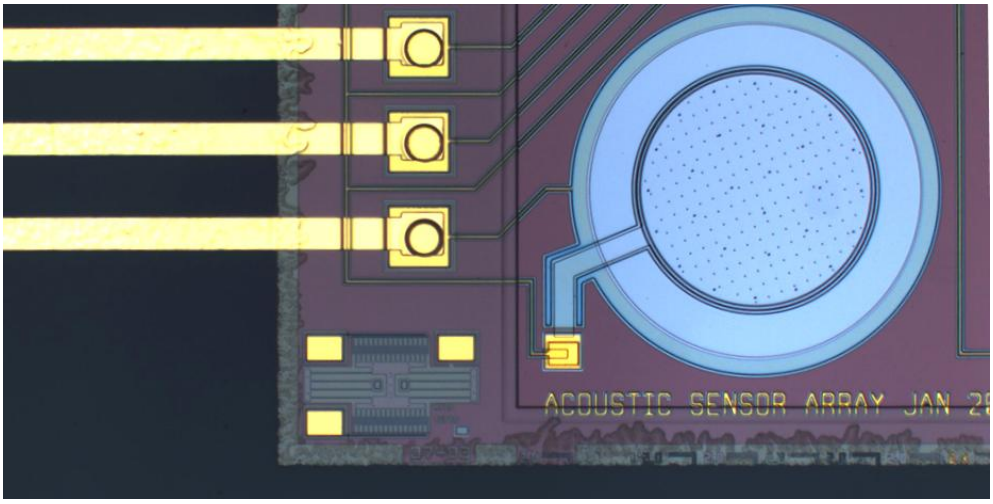


Figure 42: Layer 2 overlapping layer 1 in order to seal off the module

4.2.7 Backside Grinding

Before the backside grinding step, the wafer must be mounted to a glass handle wafer in order to protect and planarize the surface. A temporary removable thermoplastic material from Brewer Science was deposited on the surface of the wafer to bond the two together along with spacers in order to keep the wafer from bowing. This wafer bond material also is chosen for when the wafer is demounted from the substrate. An epoxy cannot be chosen to mount a handle wafer otherwise it would not be able to be removed easily when it's released from the ceramic. Therefore, the Brewer Science material was chosen for its material properties that allow it to soften at high temperatures in order to slide the handle from the substrate. A picture of the wafer after is it mounted to the handle wafer is shown is Figure 43.

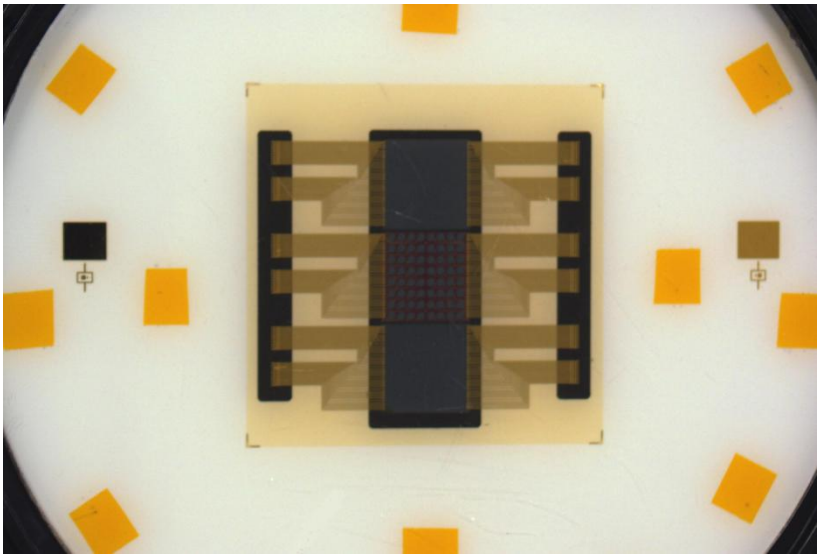


Figure 43: Handle wafer attached with wafer bond material from Brewer Science and polyimide spacers

Next, the wafer is placed onto a Logitech serrated cast iron grinding wheel with 5.67 kg. of pressure applied uniformly across the wafer. 30 µm diamond grit slurry is sprayed for 5 seconds for every 20 seconds of elapsed time to remove the bulk amount of material in order to ultimately expose the TSVs from the backside. The total thickness of the ceramic wafer was 1 mm, the TSVs were 150 µm thick, and the sensor was 575 µm thick. Therefore in order to expose the TSVs, a total of 850 µm of ceramic, epoxy, and silicon had to be removed from the wafer. The standard process for removing bulk material from silicon uses alumina slurry, however since these wafers were made primarily of alumina, a diamond abrasive coupled with a serrated cast iron plate was used. Even with the 30 µm grit slurry, small removal rates were recorded, and the total thickness variation (TTV) across the wafer approached 100 µm. With that said, the wafer was removed from the cast iron serrated plate, and mounted to a vacuum grinding fixture in order to reduce the TTV and level the surface with finer grit. A copper serrated plate with 9 µm grit diamond slurry was used in conjunction with the vacuum fixture.

At this point the ceramic wafer was at a total thickness of 300 µm. It was planned to remove the wafer from the cast iron plate with 30 µm slurry as soon as 50 µm plus the TTV plus the 150 µm of TSV thickness was reached (300 µm). This would allow the vacuum fixture to planarize the surface with 50 µm of tolerance. Ultimately, the 9 µm slurry had even slower removal rates than the 30 µm slurry, but planarized the surface back to a 35 µm TTV. After the wafer was removed from the 9 µm slurry and vacuum fixture, the thickness of the wafer was 150 µm with 35 µm TTV. Since the TSVs were not entirely exposed yet, and the vacuum fixture with 9 µm slurry slowed its removal rate down to nearly 0.1 µm/min, it was decided to place the wafer back onto the cast iron plate with 30 µm diamond slurry to expose all the TSVs as shown in Figure 44. Finally to bring the roughness of the surface down to about 100 nm, 9 µm slurry was used for 30 minutes, followed by 0.5 µm slurry for 30 minutes. Unfortunately, after grinding, small cracks in the die were observed. These were attributed to the aggressive 30 µm slurry on the serrated cast iron plate when the thickness of the substrate was about 150 µm. For the live wafer, more tests are being conducted in order to develop a grinding process for thinning ceramic with silicon parts down to 125-150 µm without cracks, a small TTV, and larger removal rates. The parameters that can be adjusted in order to compensate for these issues are different pressures, lapping wheels, slurries, times, and the order of the grinding processes.

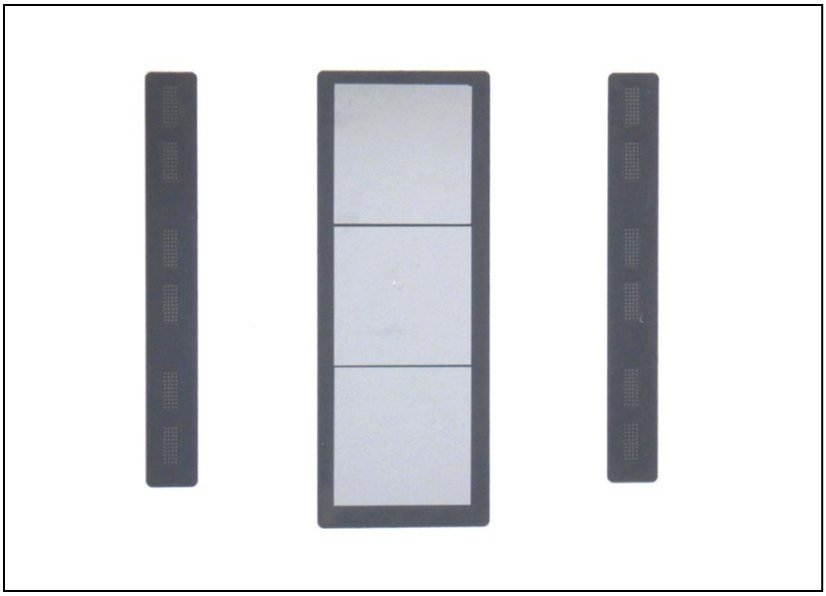


Figure 44: The backside of the ceramic wafer after grinding

4.2.8 Backside Layer 4

On the backside of the wafer, after a planar surface was produced with all of the TSV connections exposed, a layer of Draper's proprietary dielectric was deposited in order to further planarize the surface and act as the adhesion layer for the following metal pads. The surface roughness of the ceramic after grinding was roughly 100 nm. The adhesion of the dielectric and ceramic was already characterized at 250 nm roughness and 10nm roughness; therefore the roughness of 100 nm for this particular case also worked. Holes in the dielectric were patterned in order to open the connection points to the TSVs.

4.2.9 Backside Metal Layer 2

An array of all 228 pads for each individual connection was fanned out into an equidistant pattern for mounting onto the electronics board. This layer of metal was also both chromium and gold for compatibility with the HF release etch shown below in Figure 45.

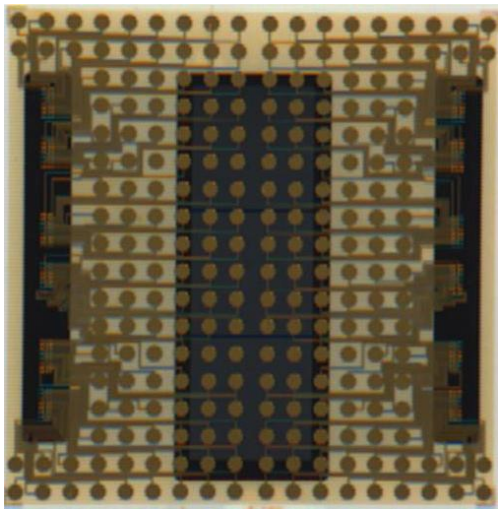


Figure 45: Fanned out array of gold pads for electronics integration

The metal deposition was similar to that of the front side deposition because it was a liftoff process with LOR and photoresist sputtered on to coat the convex holes created by the first backside layer dielectric which is shown in Figure 46. The metal pads were 1250 µm in diameter in order to create the largest pads possible for easy alignment to the interposer board between the module and the electronics. The pads were designed to be circular in order to reduce any stresses from corners during liftoff or while patterning. The top six rows of pads are connected to the top sensor, the middle six rows of pads are connected to the center sensor, and the bottom six rows of pads are connected to the bottom sensor. The 18 by 18 array of 1250 µm pads was the optimal number of pads to maximize space for the 75 µm wide traces. If the pads

were any larger, the traces would intersect and if the pads were smaller, the metal lines connecting the pads would have large separations.

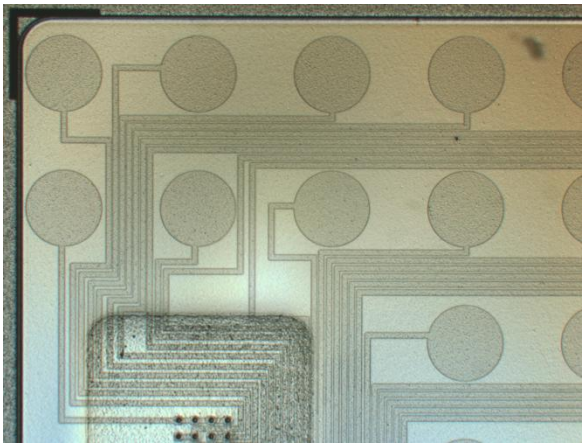


Figure 46: LOR and photo-resist deposited on the backside dielectric

4.2.10 Backside Layer 5

The final layer of the design coats over the metal pads to create a solder mask. The solder mask is used to mask off the entire surface and only leave the metal pads exposed to the environment. This layer also helps keep the solder spheres or conductive epoxy in place. Without this layer, the conductive epoxy or solder spheres would run down the traces that attach to the pads potentially contaminating other connections.

This layer is composed of the dielectric polymer which is designed to overlap the metal pads by 250 µm and encompass the solder spheres in order to surface mount onto the electronics. This is shown in Figure 47. This layer had some dielectric residue which had formed, which could be due to the wafer bow of the substrate. If the wafer is not completely flat when loaded into the MA-6 mask aligner for exposure, then some areas could receive more energy than others, thus not completely developing all of the dielectric away.

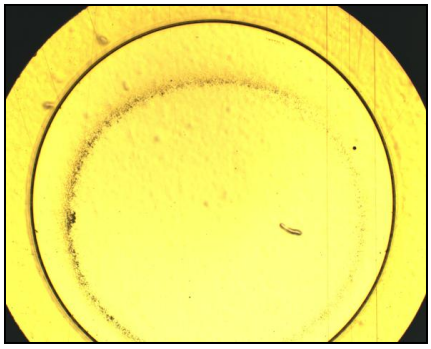


Figure 47: Solder mask on top of the gold pads with residue

4.2.11 Dice and Remove from Glass Handle

After the final layer of dielectric layer was deposited, exposed, and developed, the wafer was ready to be diced. Since all the dielectric and metal layers were kept within the dicing marks on the wafer, the diamond blade for dicing was cutting solely on ceramic. The cut was 100 µm from the dicing marks in both the x and y directions. The entire module was separated from the rest of the wafer, leaving only the module attached to its glass handle wafer. The next step after dicing was to remove the ceramic module from the glass handle wafer. Even when two smooth surfaces come into contact with one another, it is challenging to mechanically separate one from another. The process that was used in order to separate these two surfaces bonded together by a wax-like material, was to soak in wafer bond remover and then place on a hotplate and slide the two surfaces apart. A picture of the ceramic module separated from the glass handle wafer is shown in Figure 48.

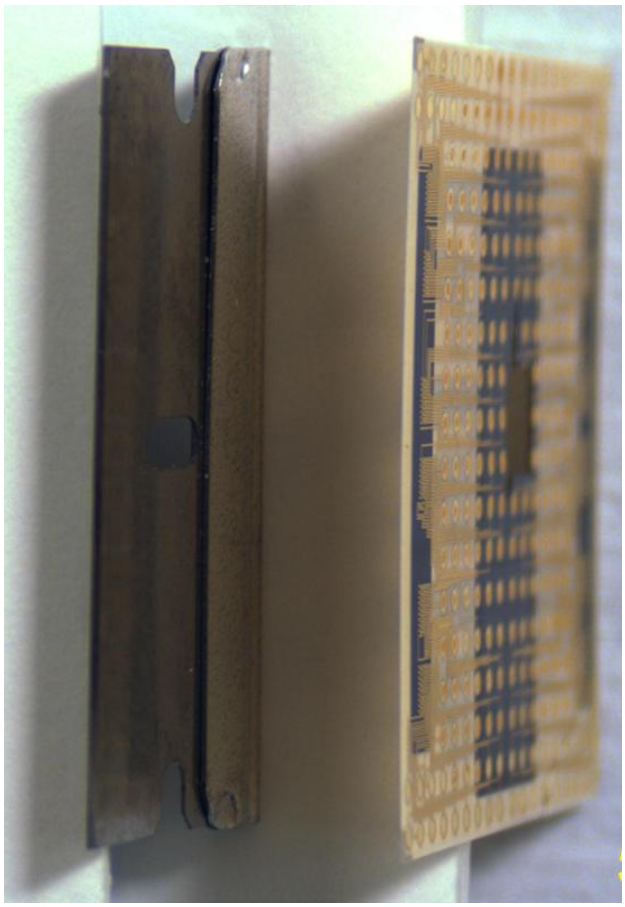


Figure 48: Diced out module compared to standard razor blade

4.2.12 MEMS Acoustic Sensor Release Etch

An aggressive release etch is used to clear out the SiO_2 from between the polysilicon membranes, using a mixture of 4 parts 49% Hydrofluoric acid (HF) to 1 part 37% Hydrochloric acid (HCl) for 30 minutes. The use of a mixture of HCl and HF rather than straight HF is important. Straight HF attacks the polysilicon grain boundaries, greatly increasing the resistivity of the polysilicon layers. By including HCl in the mixture, this effect can be greatly reduced [20]. After the release etch, the chip is rinsed in water, isopropanol, and methanol, and allowed to air dry in a dry box that has been flooded with clean, dry air with a low relative humidity. By

drying in the low humidity environment, stiction problems are reduced [1]. Two interfaces were closely examined both before and after exposure to the HF:HCl solution. Pictures of these interfaces are shown below in Figure 49 and Figure 50. Small bubbles were observed underneath the dielectric layers as if the HF:HCl solution pin-holed its way through. These bubbles were sparsely populated, but were observed across the wafer. The two pictures that were taken before and after the etchant look to be nearly identical. Minimal delamination was observed, which means the native oxide was thin enough to avoid getting consumed by the etchant. For our design, this was tolerable since from a material compatibility standpoint, everything was resistant. With that said, any delamination is undesirable however we contained it within a region where it would not affect the package itself. The package was designed with a factor of safety, so that even penetration greater than the observed 15-20 µm could be tolerated.

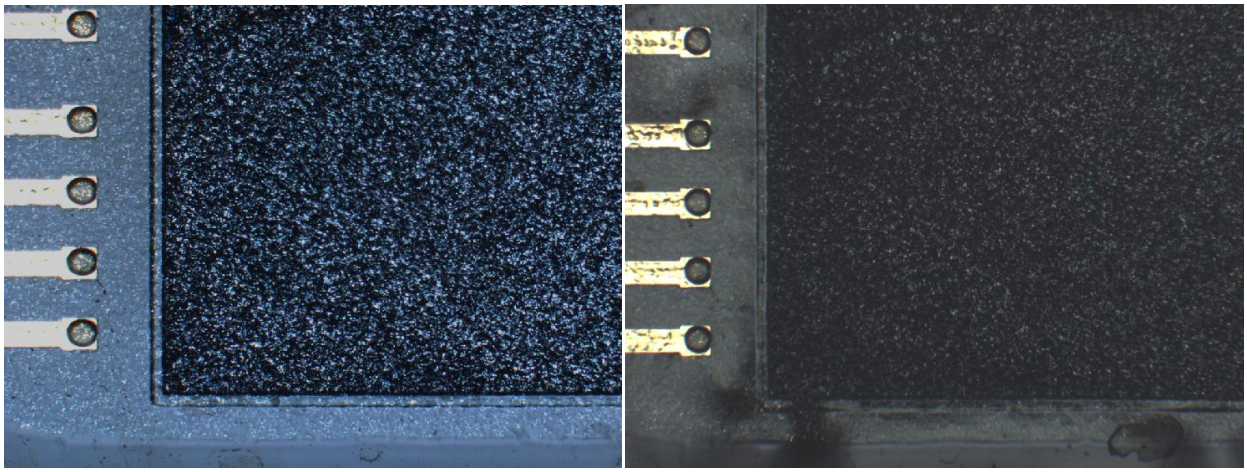


Figure 49: Corner of silicon die before and after release etch

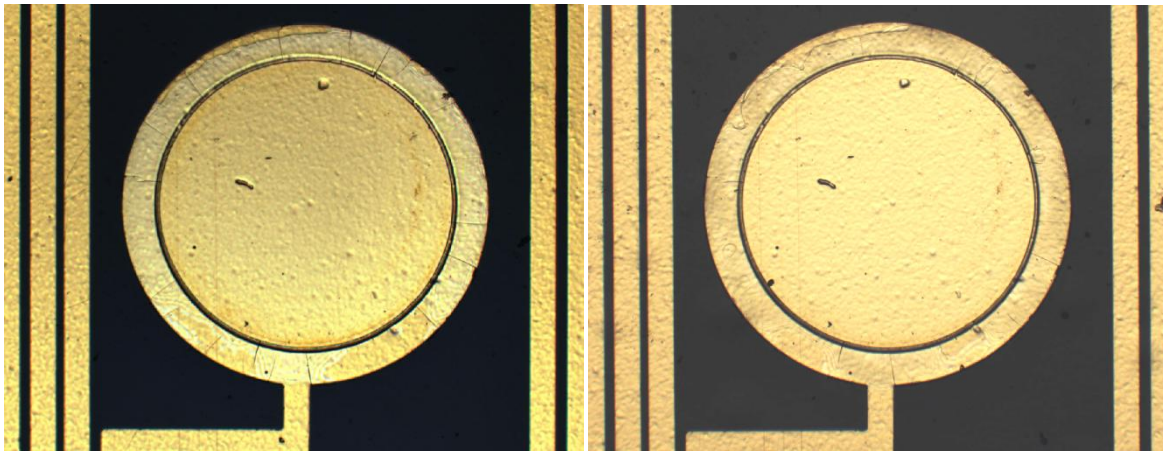


Figure 50: Backside solder mask before and after release etch

Chapter 5

5. Low Profile Packaging Method 2: Integrated-Ultra High Density Packaging Test Results

Numerous tests were run before the live wafer or even the pilot wafer were sent through the process traveler, focused on the critical steps in the i-UHD process. The three main tests performed before any process steps were started were release etchant compatibility evaluations with the different materials, encapsulation tests for surface planarity and voids within the epoxy, and a verification of adhesion and electrical connectivity after Cr/Au liftoff.

5.2 Critical Processing Steps in the i-UHD Process

5.1.1 Release Etchant Test

Two wafers were prepared for the HF release etch test. The first wafer was coated with 1 µm of oxide, and then the photo sensitive dielectric which is the standard process for typical i-UHD builds. The next wafer was just coated with the dielectric on the native oxide. This test was designed to see how far the HF etchant penetrated the interface between the dielectric and the substrate. The results of the test are shown in Figure 51. The oxide on the first wafer was completely consumed and the dielectric on top crinkled up almost immediately. The native oxide wafer showed signs of dissolution, but at a much slower rate. The maximum penetration from the patterns was 15-20 µm.

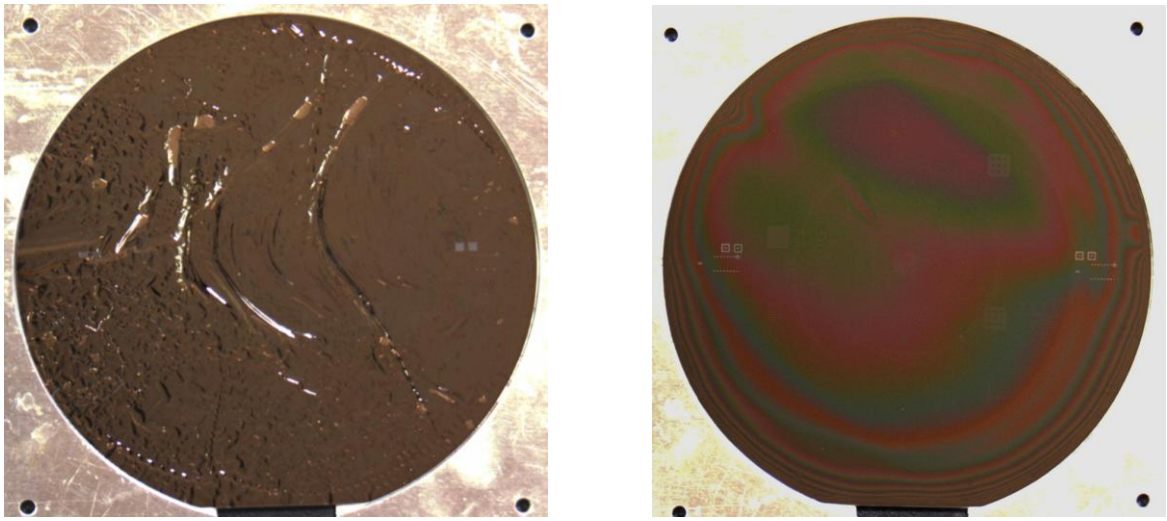


Figure 51: HF release etch test results (Left: 1 µm of oxide delaminated by HF:HCl) (Right: Native oxide after HF:HCl)

5.1.2 Encapsulation Test

One of the most important steps in the process is encapsulating the die with minimal surface topology. The purpose of the test was to measure the surface topology on the devices after capsulation, check to see whether the pads on the sensor were contaminated, and make sure none of the die shifted more than 25 µm. The test encapsulation is shown in Figure 52. The first problem that arose was that when seating the thinner TSVs with the thicker MEMS sensor, the TSVs did not leave an imprint in the conformal pad. Therefore they did not adhere well to the surface of the film. Secondly, the 5 µm pad on top of the TSVs created large topologies on the surface of the epoxy as shown in Figure 53. The TSVs were mounted with the flat side facing into the film from this point on in order to avoid epoxy voids. Lastly, the entire process was tested using a laser cut silicon wafer that was 800 µm thick. After the hard bake at 200 degree Celsius for one hour, the silicon wafer split in half as shown in Figure 54. This was attributed to the fact that the epoxy expanded and contracted at high temperatures, propagating the crack that

initially formed from laser cutting the wafer. This was the reason for choosing a ceramic substrate for the final design.

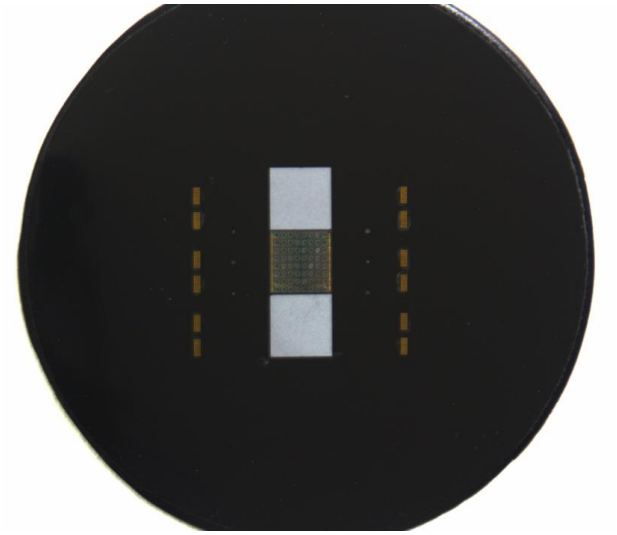


Figure 52: Test encapsulation to ensure process specifications

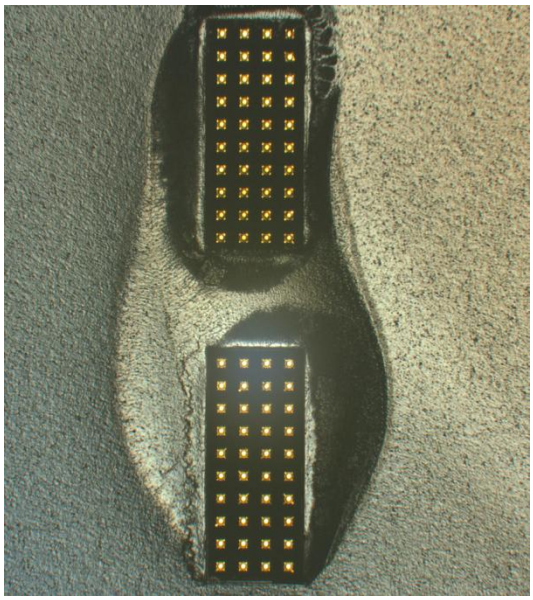


Figure 53: Surface topology around the TSVs with the 5 µm pads

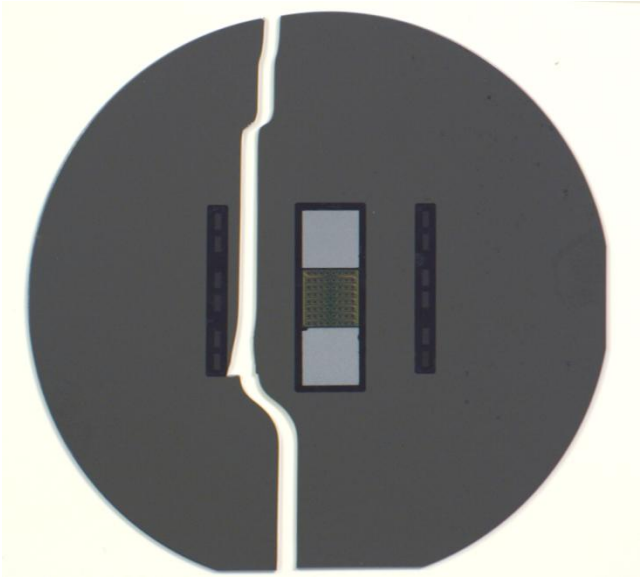


Figure 54: Cracked silicon substrate with embedded die after 200 degree Celsius hard bake

5.1.3 Chromium/Gold Sputter Deposition with LOR and Photoresist Test

Since there were two layers of Cr/Au for metallization, a test wafer was prepared to characterize its adhesion to the Draper proprietary dielectric, and to formalize a process for its deposition. Initially the results of the liftoff process yielded residue as shown in Figure 55. The LOR and photoresist did not get exposed with enough energy in order to be developed away completely. Therefore the exposure time was doubled in order to remove this residue for the pilot wafer and live wafer. Once the exposure time was doubled, there was no residue from the LOR resist, and the metal lines were tested as continuous.

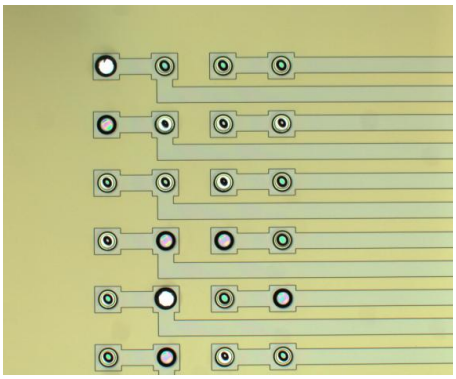


Figure 55: Residue on the surface of the wafer after developing the dielectric away

Chapter 6

6. Conclusions and Future Work

6.1 Conclusions

In this thesis, two packaging methods were explored for integrating MEMS acoustic sensors into low profile packages. For the conductive ink method of packaging an acoustic sensor, line widths of 150 µm were drawn and line heights of 20 µm were achieved in order to successfully stay within the viscous sub layer of flow and connect the pads on the sensor to the trace on the PCB. An entire packaging approach to integrate a live acoustic sensor into the custom PCB package was developed, and both the hardware and software implemented allowed for the traces to be modified. This enables applications to numerous packaging designs. This process is low cost and easy to implement with low cost equipment, and has been applied successfully to package a live sensor.

Another packaging approach was also explored in collaboration with Draper Laboratory. For the i-UHD platform for packaging MEMS microphone arrays, an entire project was outlined, designed, tested, developed and fabricated from start to finish with over 400 process steps. Six masks were designed in L-edit, all of which were successfully used, in order to transfer geometrical patterns onto the substrate with high enough resolution to reroute over 200 connections to the backside of the wafer. Issues were identified and fixed with numerous pilot wafers, focused on the critical steps for the live embedded MEMS microphone array wafers.

6.2 Remaining Issues and Future Work

While the primary goals of this research were achieved, there are still some issues that need to be addressed. First and foremost, the least characterized process in the traveler was the ceramic wafer backside-polish step. This step used an aggressive serrated cast iron grinding wheel with 30 µm diamond slurry in order to remove the bulk ceramic. Since it was the first time that this process has been used, there were still details that needed to be characterized. The standard process to thin silicon substrates used alumina slurry for bulk silicon removal. Since the ceramic wafers were made up of almost entirely alumina, a 30 µm diamond abrasive was chosen in order to get higher removal rates. A grinding plate that is designed to uniformly grind down ceramics was ordered and is currently being used to run some tests for thickness variation across the wafer, removal rates, surface roughness, and to check whether surface cracks form at small thicknesses.

While the research here provides two new packaging approaches, there is still much room for improvement. One of the limiting factors in the acoustic array design was the thickness of the Through Silicon Vias. Since their thickness was on the order of 150 µm, it forced the design to be thinned to at least 150 µm to expose all connections. If the TSVs were twice as thick, the polish back step would not be as critical to the success of the design. Fortunately, the state of the art of the TSV has advanced, and now such things can readily be purchased from other manufacturers.

Another interesting solution is to stack multiple TSVs on top of one another as shown in Figure 56, however this would take some time to develop.

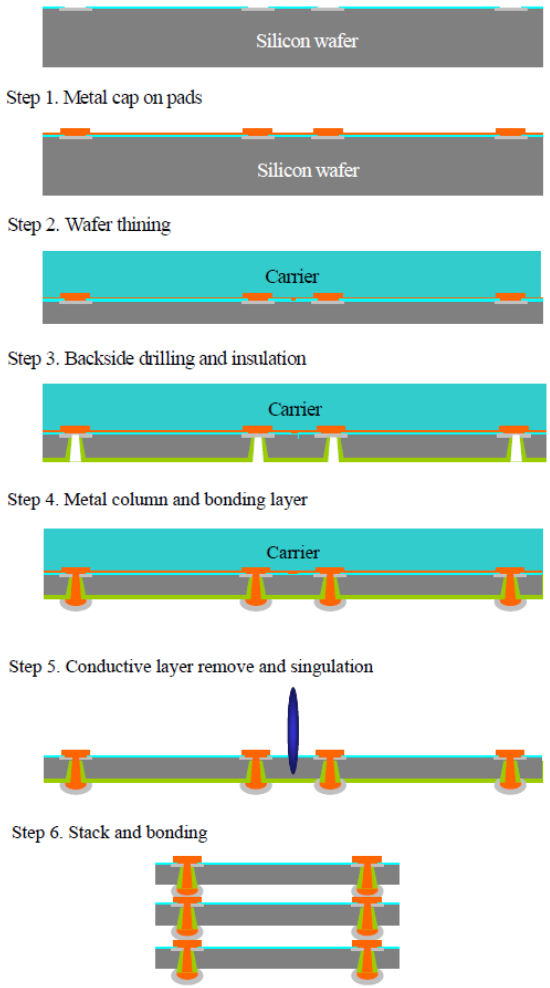


Figure 56: 3-D stack of through silicon vias in order to increase thickness (Figure taken from Li-Cheng, S. et. al [21]).

Optimizing a uniform etch with the deep reactive ion etch (DRIE) tool in order to create taller posts to increase the thicknesses of the vias would also prove useful for this design. With taller TSV chips, the risk in the polish-back step would be greatly reduced.

Finally, for future work in the field of packaging, including the electronics on board with MEMS sensors, in bare die form, would eliminate an intermediary board for connection. This

would also significantly reduce signal noise, miniaturize the system, and advance this field by combining MEMS sensors with bare die silicon electronics to create a hybrid packaging scheme. As far as the future for conductive ink packaging, aerosol nano-ink deposition is the gateway to high resolution printed lines. An aerosol jet printer is very expensive compared to syringe printing, however companies similar to Optomec can process individual orders, thus reducing the price dense connections. Aerosol jet printing provides a packaging approach for low profile surface connections that are dispensed with high resolution and 3-D versatility.

In conclusion, these two packaging methods span the range between a cost-premium advanced packaging approach and a low-cost versatile method of dispensing low profile connections directly onto a printed circuit board. With these two packaging approaches, vibrating MEMS acoustic sensors were able to be successfully embedded into their respective packages with reduced surface topologies, increased spatial resolution, and added flexibility, thus advancing the field of MEMS packaging.

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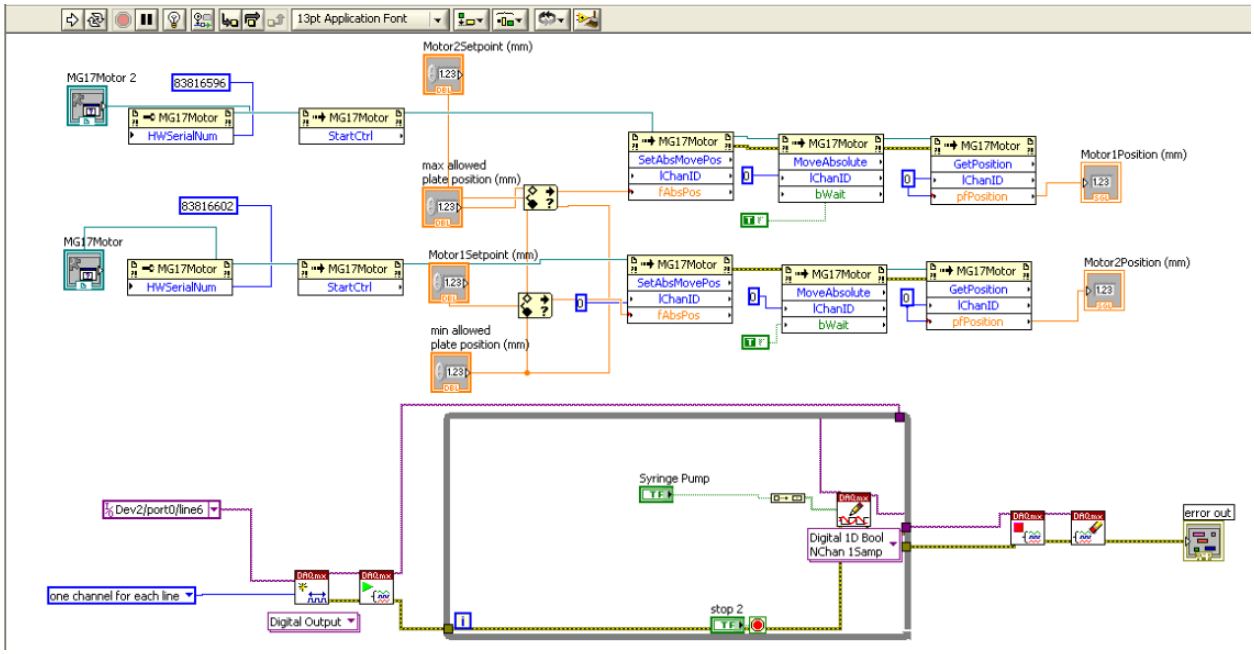
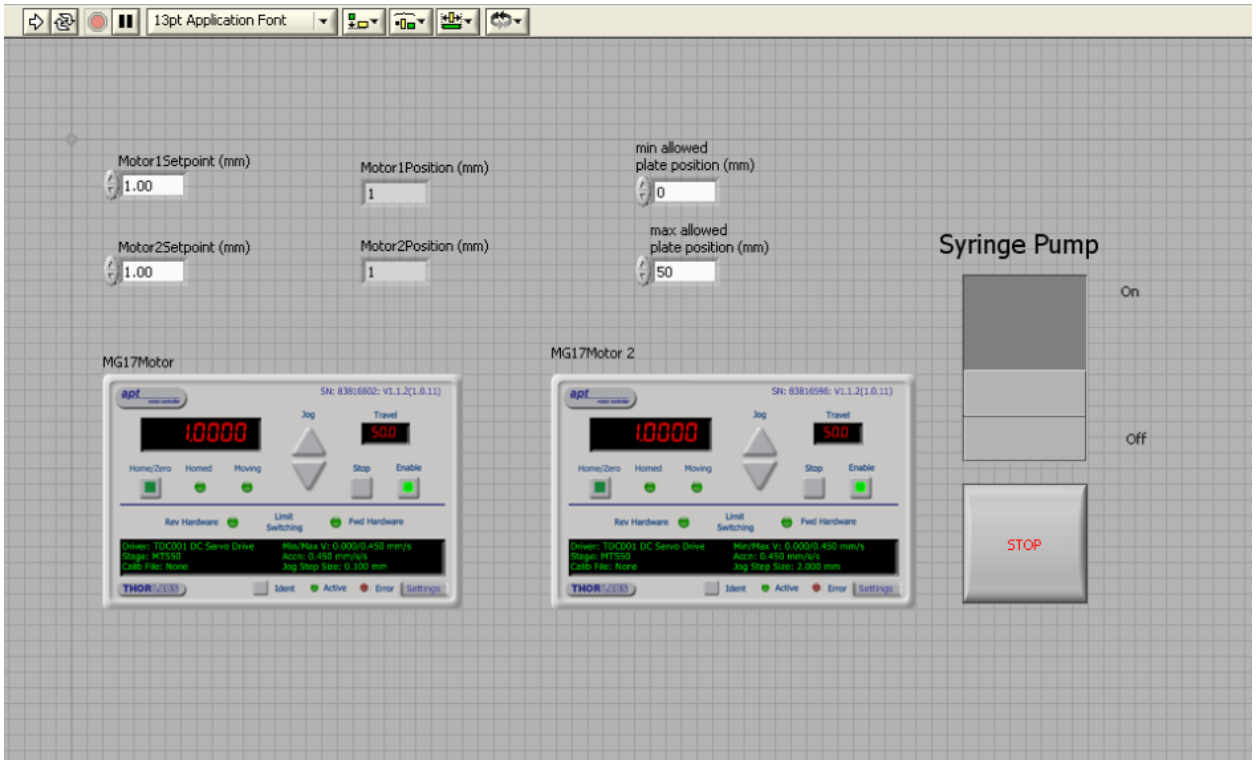
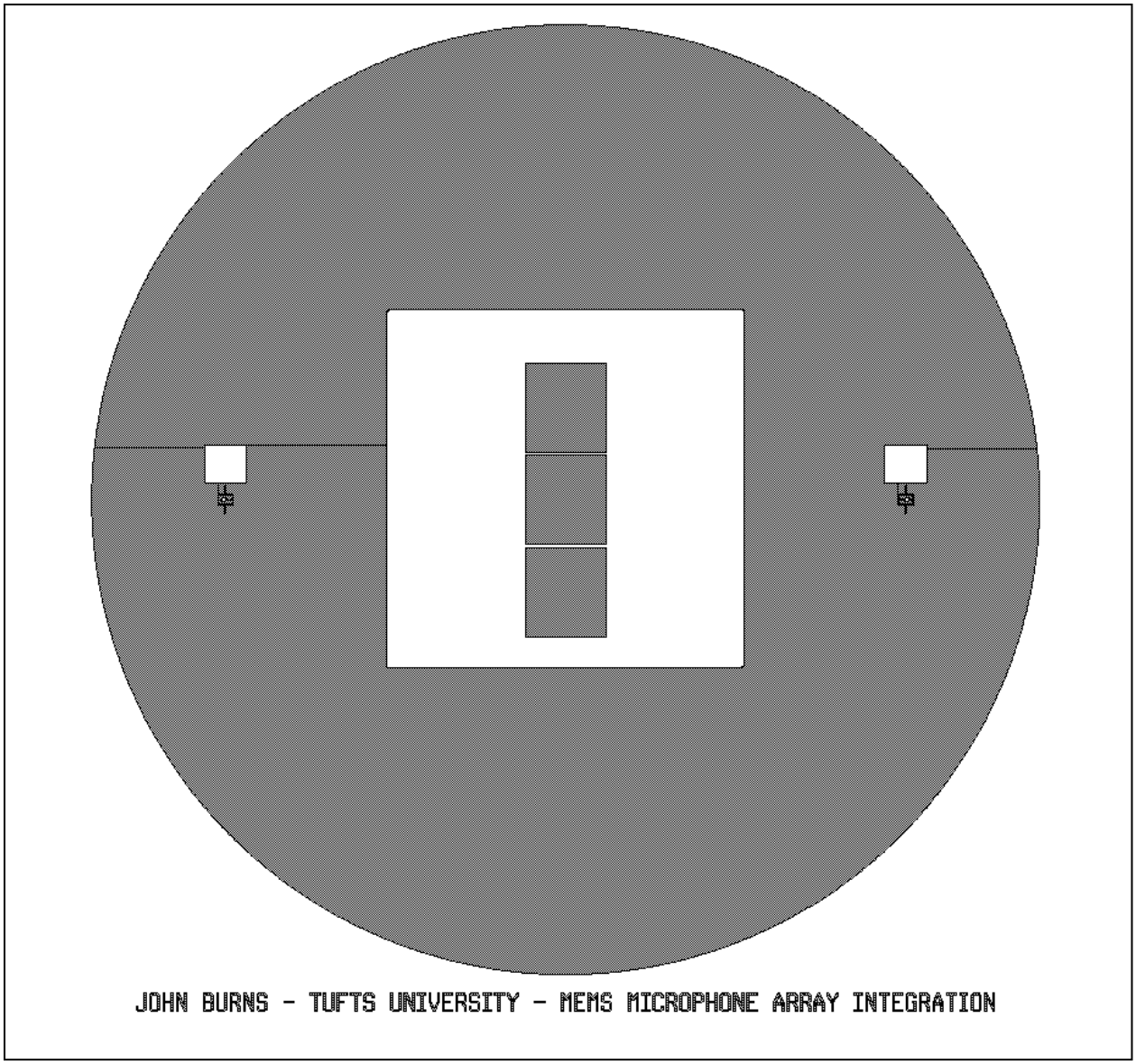
Appendix

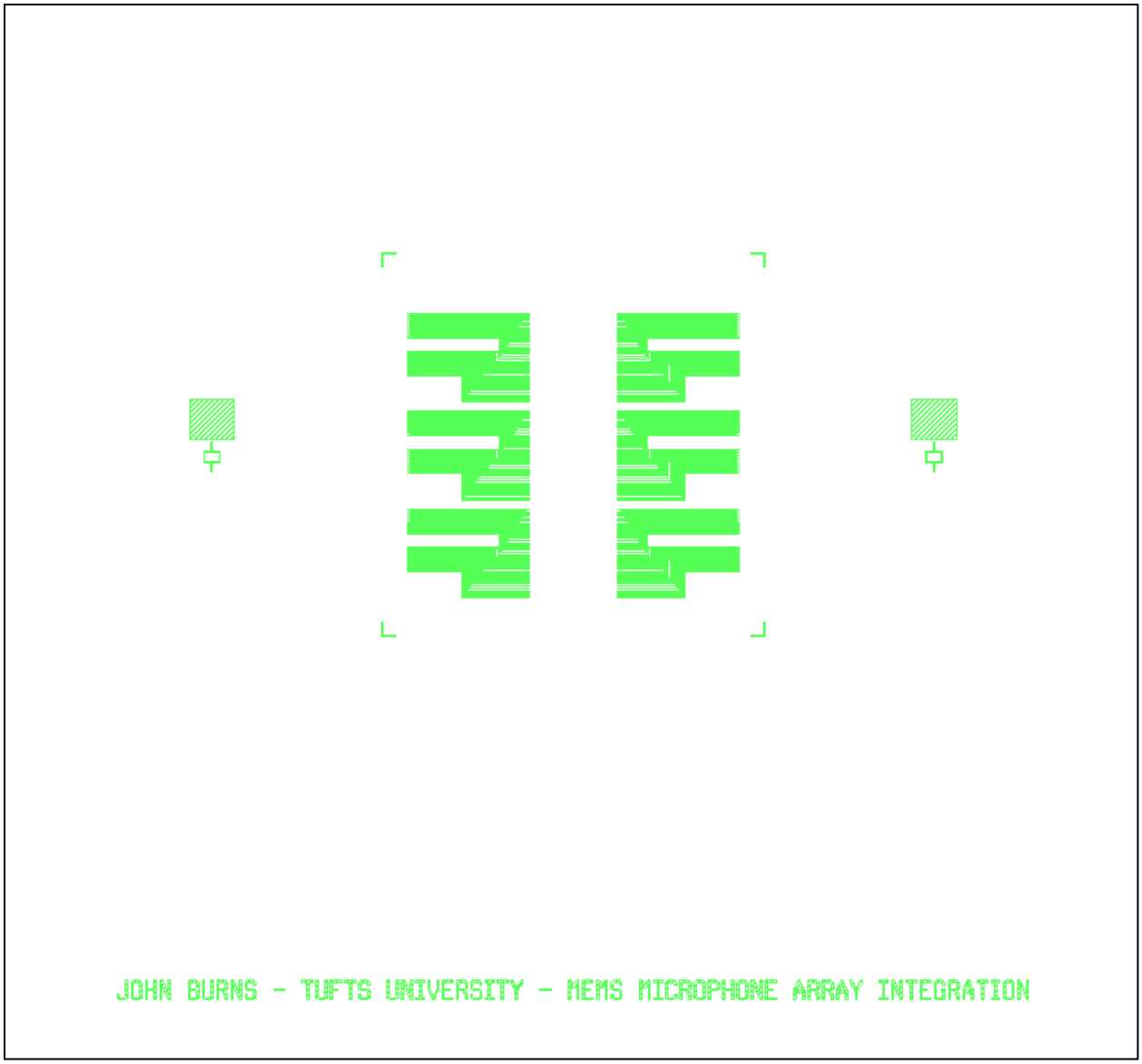
Labview Code/Graphic User Interface

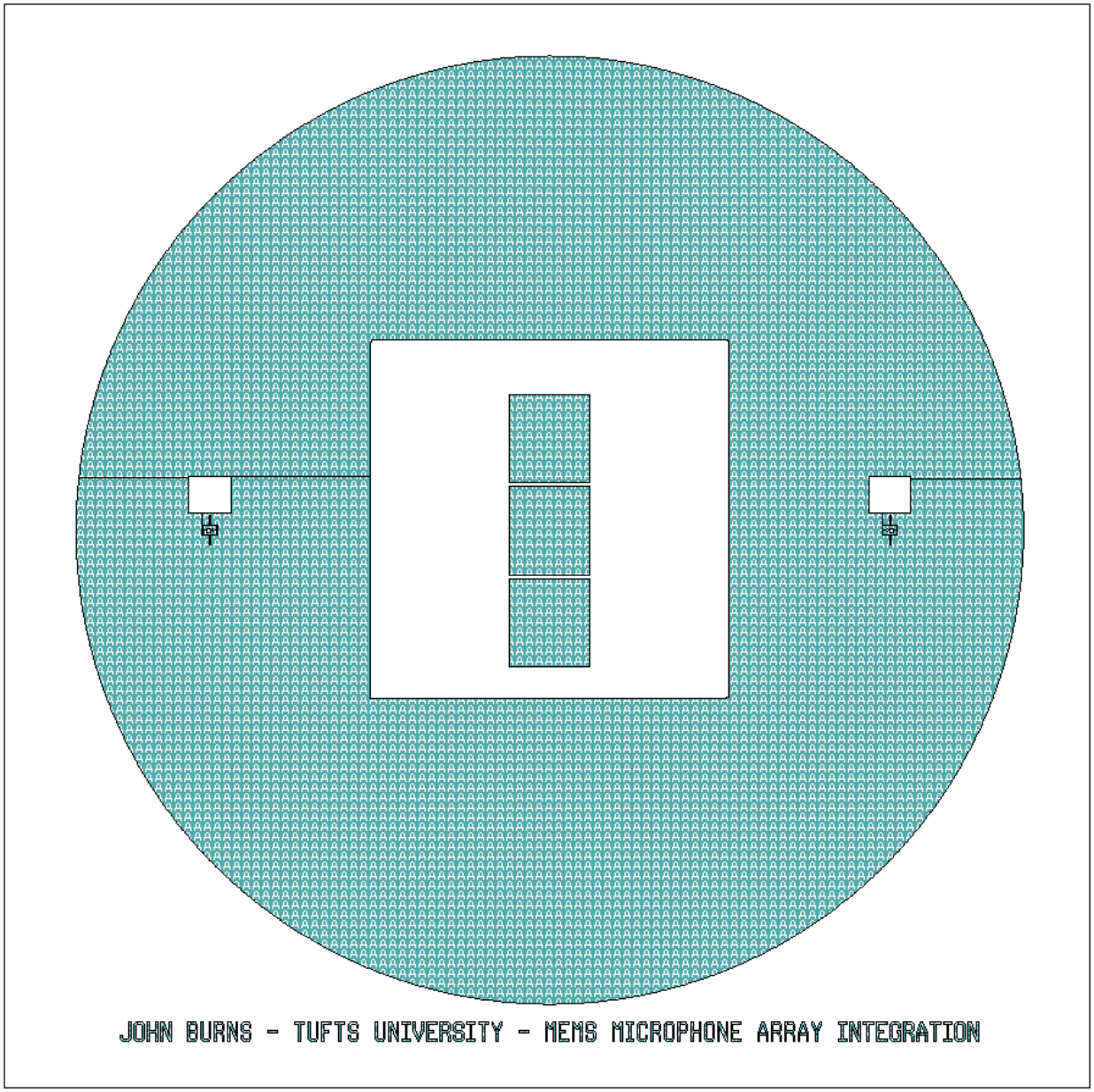




Six Masks Used for both Frontside and Backside Processing




JOHN BURNS - TUFTS UNIVERSITY - MEMS MICROPHONE ARRAY INTEGRATION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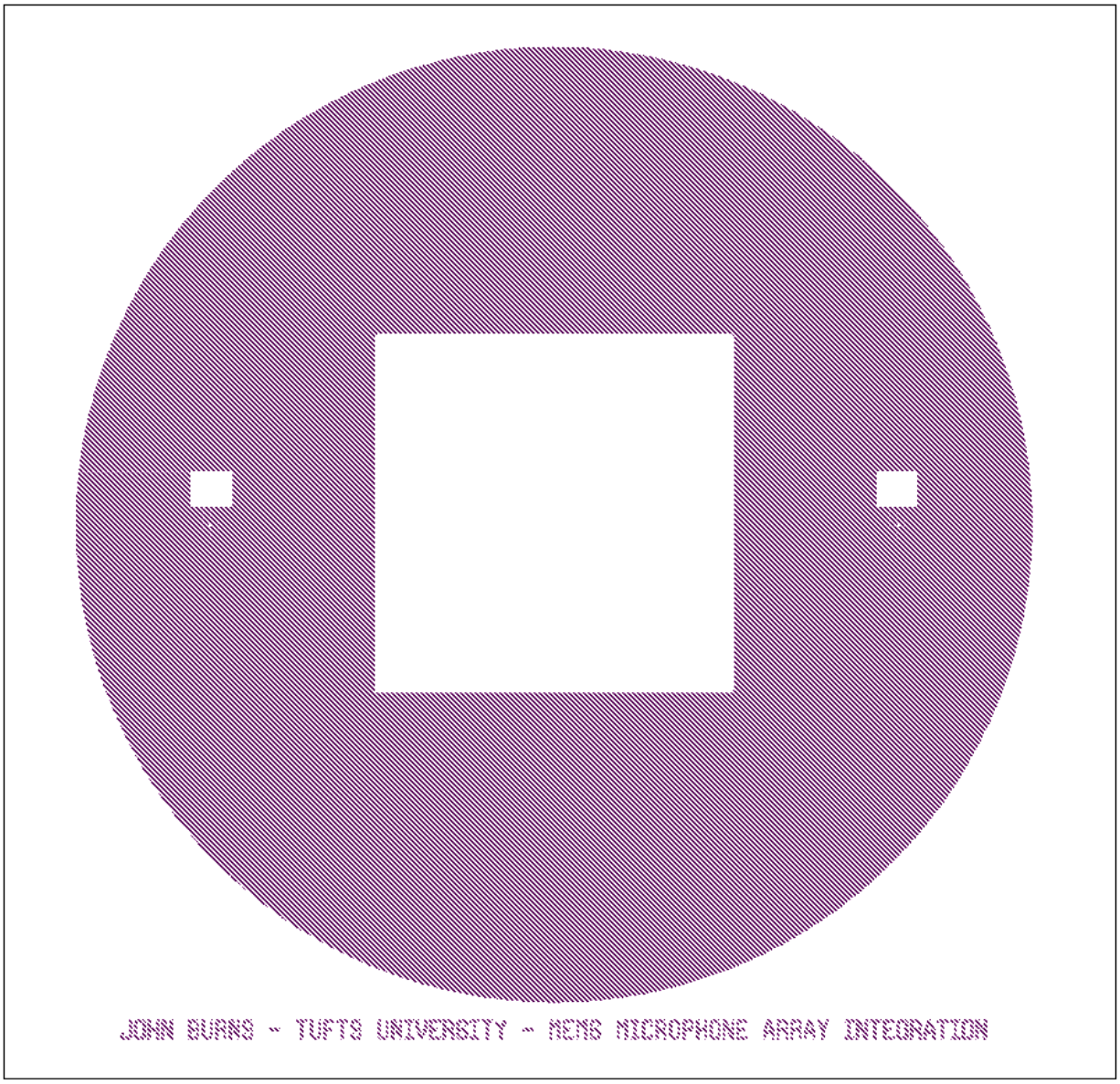
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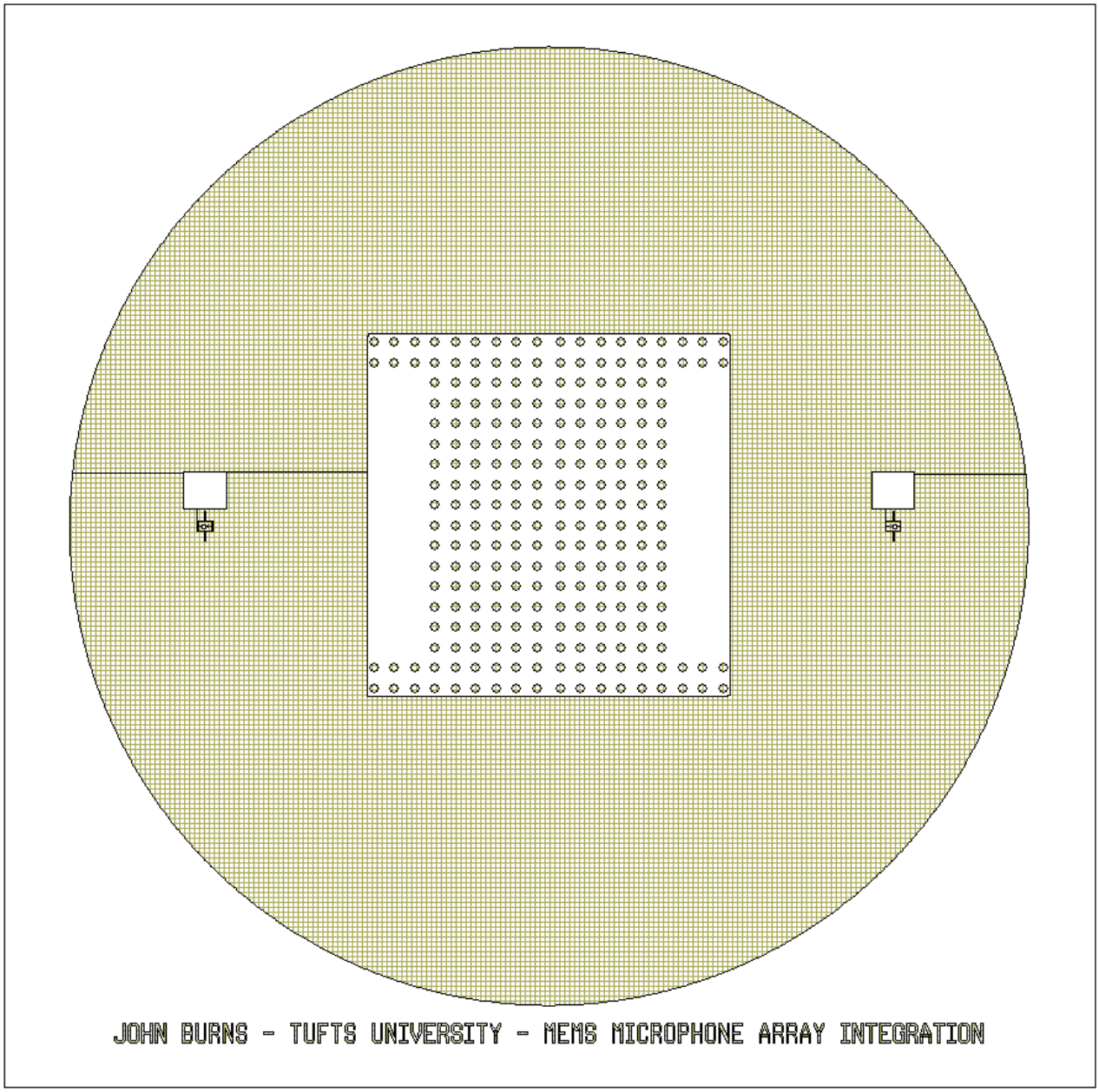
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