Effect of Interlayer Insertion into Bilayer Organic Solar Cells

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Senior Honors Thesis

May 2011

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Abstract

Organic solar cells show potential to be an alternative to conventional inorganic solar cells due to the possibility for lower processing costs, flexibility, and large-scale fabrication techniques. The goal of this project was to increase the efficiency of bilayer organic solar cells by increasing the maximum operating voltage. In this study, it was hypothesized that the addition of an insulating material into the active layer could boost the open-circuit voltage. A thin layer of either bathocuproine or lithium fluoride (LiF) was inserted at the interface of both copper phthalocyanine/fullerene ($CuPc/C_{60}$) and poly(3-hexylthiophene)/fullerene ($P3HT/C_{60}$) donor/acceptor organic solar cells. The insertion of LiF at the $P3HT/C_{60}$ interface increased the open-circuit voltage by 11.7% without a substantial reduction in the short-circuit current density. The other modified active layers did not show an improvement in overall solar cell performance. Active layer surface morphology was examined using tapping mode atomic force microscopy. The higher open-circuit voltage of the $P3HT/LiF/C_{60}$ device may be attributed to unique morphological changes in the active layer or other energetic effects.

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1 Introduction

The demand for energy is accelerating at an astonishing rate due to the rapid growth of developing nations and the emergence of new economies. Fossil fuels provide an estimated 86% of the world's energy needs.[1] The continuous burning of fossil fuels not only poses a serious threat to the climate, but also is an unsustainable method of energy production. In contrast, solar cells directly convert sunlight into electricity and have the potential to cleanly and sustainably meet future energy demands.

The cost of electricity generated from a solar cell is considerably higher than that of fossil fuels. In order for solar cells to become more competitive in the marketplace, solar cell production costs need to drop. Commercial solar cells are typically fabricated using inorganic materials such as silicon, but solar cells fabricated from organic materials have become an attractive alternative. Large scale roll-to-roll processing techniques can potentially print organic solar cells (OSCs) on plastic substrates using minimal amounts of material, resulting in a relatively lower-cost solar cell that is lightweight and flexible.[2,3] State-of-the-art OSCs approach commercial efficiencies of around 3 % whereas commercial inorganic solar cells (ISCs) are over 15%, thus the efficiency of OSCs must be improved in order to compete with ISCs.[2,4]

The goal of this research is to boost the efficiency of an OSC by increasing its maximum operating voltage – the open-circuit voltage (V_{OC}). The general consensus amongst researchers is that the open-circuit voltage cannot exceed the energy offset between active materials in a heterojunction OSC.[5,6] Therefore, the tunability of the energy offset is vital to the optimization of the device efficiency and understanding of the inner-working mechanisms of OSC devices. It

is postulated that the insertion of a third material into a bilayer heterojunction OSC device can increase the open-circuit voltage, thus directly improving the operating efficiency.

2 Background

At its most basic level, a solar cell is a semiconductor diode that converts photons (light) into electricity. The mechanisms by which organic solar cells accomplish this phenomenon are fundamentally different than those of inorganic solar cells. The following sections provide a brief background on the underlying physics of organic solar cells.

2.1 Organic vs. Inorganic Solar Cells

In both OSCs and ISCs, excitons (electron-hole pairs) are rapidly generated upon absorption of light by the semiconducting materials. The band gap energy (E_{gap}), the energy difference between the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO), characterizes a semiconductor. If the energy of a photon is greater than that of the band gap, electrons are promoted from the HOMO to the LUMO; as a result, excitons are generated. The optimum E_{gap} for an ISC is 1.4 eV; at this value, the maximum amount of solar energy is utilized in generating excitons.[1] OSCs rely on a different mode of electron-hole separation and there is not a single optimum band gap value that maximizes photon to exciton energy transfer. The band gaps of OSCs range from 1.7 to 3.0 eV and must be chosen wisely to ensure adequate exciton generation.[3,6,7]

The main difference between OSCs and ISCs lies in the mode of electron-hole separation. In a p-n junction ISC, the built-in electric potential is high enough at the p-n interface that free charge carriers are generated virtually upon light absorption. Excitons are electrostatically

bound together in OSCs due to the low dielectric constants of OSCs relative to ISCs; a low dielectric constant signifies a large electrostatic attraction between an electron and a hole.[8] As a result of the electrostatic attraction between an electron and a hole, an extra energetic driving force is necessary to separate them into mobile charge carriers. The location of charge separation occurs at the heterojunction between two organic semiconductors.

2.2 Organic Solar Cell Physics

In a bilayer OSC, a planar heterojunction comprises an active layer consisting of two distinct semiconducting materials – an electron donor and an electron acceptor. The difference between the HOMO / LUMO energy levels of the two materials creates an energy level offset at the heterojunction. A donor material typically has low ionization energy, and an acceptor material has high electron affinity. Good donor-acceptor candidates also have high charge-carrier mobility and conductance. The offset at the heterojunction provides the energy necessary to overcome the electrostatic binding energy of the exciton. Figure 1 summarizes the steps of free charge carrier generation in an OSC.

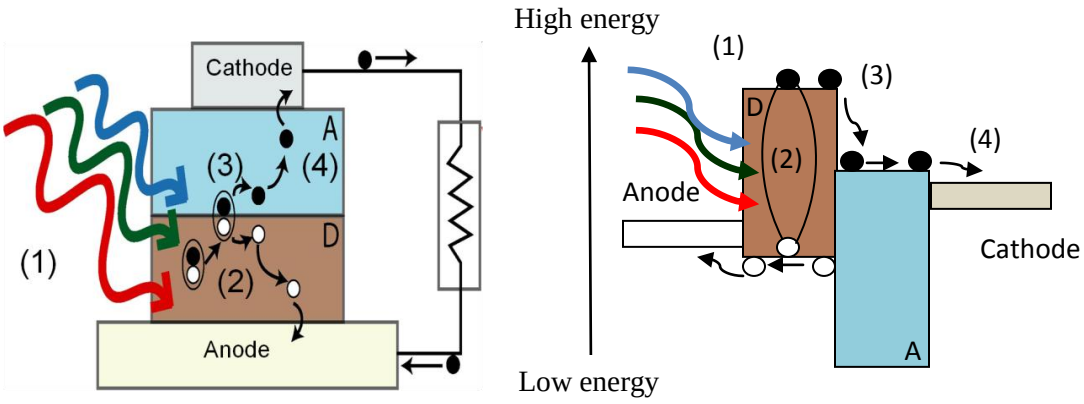


Figure 1. (a) Cross-sectional diagram (not drawn to scale) of a bilayer OSC, where "D" denotes the donor and "A" the acceptor. (b) An energy diagram representing the energy levels of each material in the device. The arrow represents increasing electron energy. Steps of current generation (electrons in black, holes in white): (1) The active layer of the cell absorbs photons, causing the generation of excitons (electron-hole pairs) within the cell, (2) Excitons diffuse to a heterojunction comprising a donor and acceptor, (3) A favorable energy offset between the organic layers separates the electron-hole pair into free charge carriers, (4) Electrons are collected at the cathode, and holes are collected at the anode. Mobile electrons may then flow through an external circuit.

2.3 Interlayer Insertion and the Open-circuit Voltage (V_{OC})

OSCs perform useful work under forward bias conditions, where electrons are injected from the cathode and holes from the anode (Figure 2 (a)). A bilayer cell consists of a planar interface between the donor and acceptor material. As excitons migrate towards the heterojunction, they become highly concentrated and establish an electrochemical potential energy gradient for the photogenerated electrons and holes to diffuse away from the heterojunction and out of the device. The V_{OC} is the theoretical maximum voltage at which a device can operate, occurring when the net current within the device is zero, and all holes and electrons recombine.

The physical effects governing the V_{OC} are still unknown. It has been shown that the V_{OC} in bilayer OSCs does not depend on the energy difference between the anode/cathode and the vacuum level as it does in single layer OSCs.[5] Thus far, research shows that the V_{OC} is a function of the energy level difference at the heterojunction, $E^D_{\text{HOMO}} - E^A_{\text{LUMO}}$ (represented by ΔE in Figure 2).[5,6] Therefore, an increase in this energy difference can directly cause an increase in the V_{OC}.

Insulating materials such as bathocuproine (BCP) have been used as exciton blocking layers to prevent excitons from quenching at the acceptor-cathode interface, which enhances the charge carrier collection at the cathode.[3] Lithium fluoride (LiF) has been used similarly to reduce the electron injection barrier at the acceptor-cathode interface.[9] In both cases, OSC performance was improved. A study conducted by Liu et. al demonstrated that the insertion of an interlayer material, a 5 Å layer of MoO_3 placed between the acceptor and donor, substantially increased the V_{OC} of a bilayer OSC.[6] The authors concluded that band bending at the edges of

the LUMO and HOMO levels occurred and that this increased the difference between E^D_{HOMO} and E^A_{LUMO}. Band bending is a phenomenon that occurs due to a dipole created between two materials, causing energy levels to shift.

This research study aims to boost the V_{OC} by inserting a thin insulating material (~2 nm) between the acceptor and donor layers. It is hypothesized that the V_{OC} can be boosted due to band bending and a decrease of charge-carrier recombination at the acceptor-donor interface under forward bias conditions. Charge accumulation at the acceptor-interlayer interface could increase the electrochemical potential gradient causing a boost in V_{OC}.

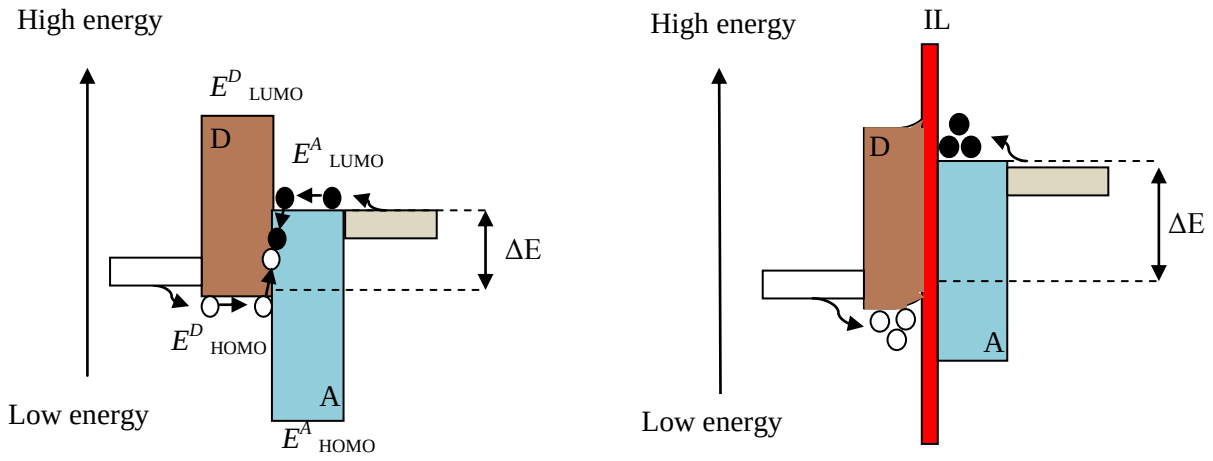


Figure 2. (a) Under forward bias conditions electrons and holes are respectively injected from the cathode and anode where they can recombine at the heterojunction. ΔE is the difference between the HOMO level of the donor and the LUMO level of the acceptor. (b) By insertion of a thin interlayer (IL), ΔE may increase due to band bending and a decrease in charge carrier recombination. Charges accumulate at the interface increasing the electrochemical potential of electron diffusion toward the cathode and hole diffusion toward the anode.

2.4 Performance Characterization

Current-voltage (*J*-*V*) curves are useful in analyzing the performance of OSCs (Figure 3). A bias is applied to a device under illumination to study photo-response behavior. The V_{OC} is found at the point at which the current is zero, and the J_{SC} (short-circuit current density) is found at the point at which the voltage is zero. The actual maximum operating power of the device is found by forming the largest possible rectangular area within the fourth quadrant. The efficiency of devices is typically characterized under AM 1.5 light, which mimics the solar spectrum; for the purposes of this research, an LED was used to generate monochromatic red, green, or blue light. The device efficiency corresponding to each color of light is calculated using the monochromatic efficiency equation [eq. (1)], where the incident power density of the light (P_L) can be measured with a thermal power sensor. Another important value is the fill factor (*FF*): the ratio between the maximum power delivered by the device and the product of J_{SC} and V_{OC} [eq. (2)].

(1) $$\eta_L = \frac{J_{max} \cdot V_{max}}{P_L}$$

(2) $$FF = \frac{J_{max} \cdot V_{max}}{J_{SC} \cdot V_{OC}}$$

By inserting an interlayer, it is postulated that the *J*-*V* curve will shift to the right (Figure 3) due to an increase in the V_{OC}. If the current is maintained at the same level prior to the insertion of the interlayer, then the maximum power of the device will increase by an amount proportional to the increase in voltage.

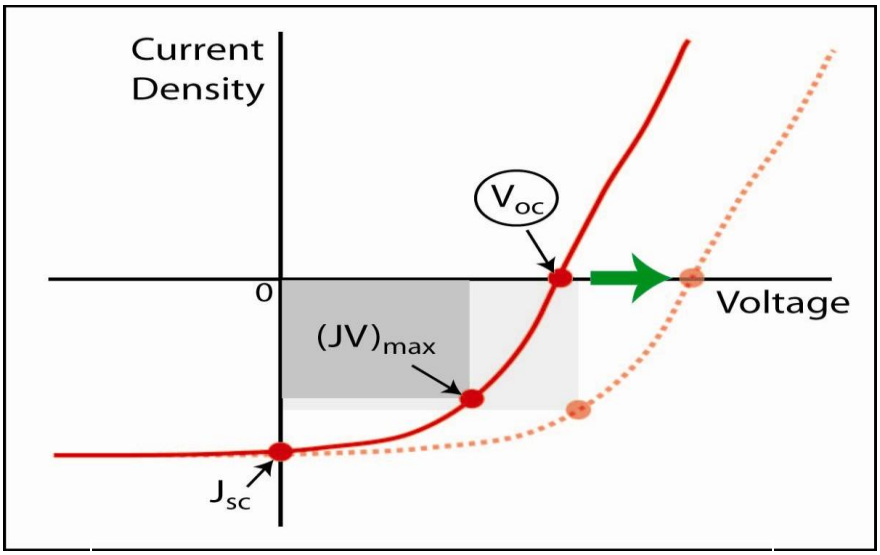


Figure 3. Current-voltage (*J*-*V*) response of a solar cell under illumination. The maximum power output of the cell is $(JV)_{max}$. Insertion of the interlayer could boost V_{OC}, as characterized by a shift in the curve to the right.

3 Experimental

The experimental procedure was adapted from previous research on bilayer devices. Film thicknesses were chosen to be relatively consistent with past solar cell devices that incorporate the same materials used for these experiments.[6,10,11,12]

Solar cell devices were fabricated using spin coating and thermal deposition methods. During spin coating, soluble materials - e.g. P3HT (poly(3-hexylthiophene)) and PEDOT:PSS (poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate)) - are added as droplets to a substrate and then the substrate is rapidly rotated. The centrifugal force creates a thin (nm scale), uniform layer of material on the substrate. All other materials were deposited using thermal deposition. Thermal deposition is typically performed under vacuum ($<10^{-6}$ mbar) to ensure that no unwanted particles interfere with the deposited material, and to obtain large mean free paths for sublimed (or evaporated) molecules. A small amount of material (< mg) is placed in a crucible that is heated by a resistive heating coil in the vacuum chamber. The solid material sublimes (or

evaporates) and upon reaching the substrate condenses rapidly to form a thin, uniform layer. The evaporation rate is usually kept low to favor layer uniformity.

The performance of each device was investigated by measuring current-voltage characteristics and analyzing surface morphology. Each solar cell contained six silver contact pads in order to ensure accurate device characterization.

3.1 Materials

Two distinct electron-donor materials were used in conjunction with two distinct interlayer materials. The morphology at the donor-interlayer interface significantly contributes to the performance of the solar cell. For these reasons, well-researched materials were chosen for these experiments.[6,10,11,12]

CuPc (copper phthalocyanine) (>99.99%, from Aldrich) and P3HT were used as donor-layer materials. P3HT (regioregularity ~92%, from Rieke Metals) was prepared at a concentration of 5 mg / mL dichlorobenzene solution, stirred for 40 min at 60 °C, and stored in a glove box under nitrogen atmosphere (<0.1 ppm O_2 and H_2O) because of sensitivity to air. BCP (>99.99%, from Aldrich) and LiF (>99.99%, from Aldrich) were used as interlayer materials. C_{60} (>99.5%, from nano C) was the only material used as the acceptor-layer. PEDOT:PSS (from H.C. Starck) was refrigerated and used as a buffer layer between the anode and active layer. ITO (indium tin oxide – the anode) on glass (from Thin Film Devices Inc.) was used as the substrate, and Ag (>99.99%, from American Elements) was used as the cathode. Finished devices were stored in the glove box under nitrogen atmosphere in order to prevent degradation.

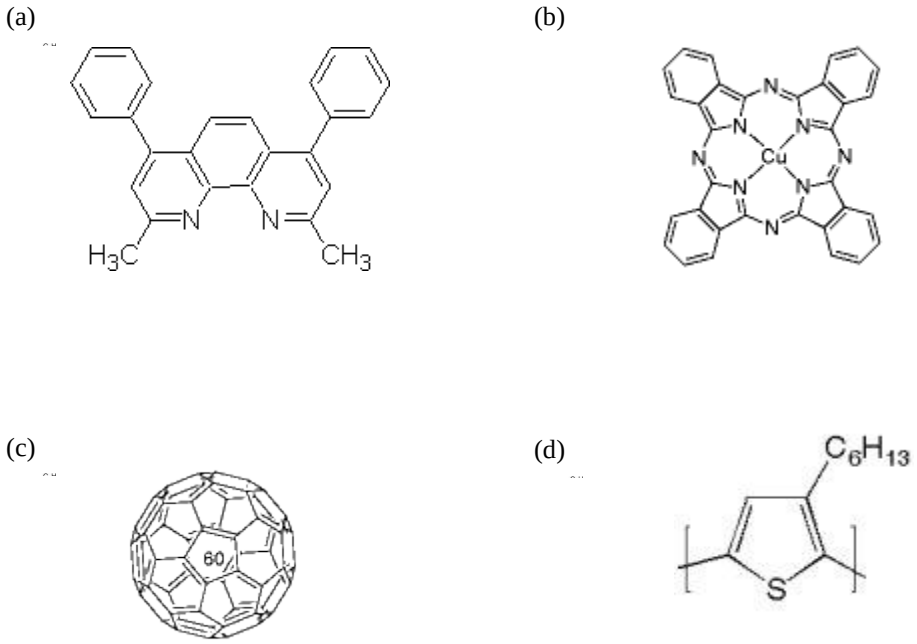


Figure 4. Chemical structure of organic materials used in the active layer of devices (a) BCP,[13] (b) CuPc,[13] (c) C_{60},[13] (d) P3HT[14]

3.2 Cleaning

Prior to device fabrication, ITO and silicon substrates were cleaned. Substrates were sonicated in a detergent solution (0.2% micro-90 in water) for 5 min, and subsequently transferred to deionized water and acetone where they were sonicated for 5 min in each solution. After being sonicated, substrates were placed in boiling isopropanol (~180 °C hotplate setting) for 5 min. Substrates were blow-dried using pure nitrogen, and placed in an O_2 plasma environment for 15 s to complete the cleaning process. †

† The first batch of cells (CuPc/LiF/C_{60} active layer) was placed in O_2 plasma for ~ 90 s. Upon investigation I-V characteristics of these cells (see results) the O_2 plasma time was reduced to 15 s for all proceeding experiments.

3.3 Device Fabrication

Bilayer devices were constructed in a stack formation (Figure 4), in which each material was individually deposited on top of the other, starting with the ITO-glass substrate. On the ITO substrate, PEDOT:PSS was spin coated at 4000 rpm for 60 s and baked for 10 min at 120 °C (hot plate temperature setting). For deposition of the P3HT donor layer, devices were transferred to the glove box, and the P3HT solution was spin coated at 900 rpm for 60 s. The P3HT films were dried in vacuum (~10^{-3} mbar) for 45 – 60 min, and transferred to the thermal deposition chamber where the devices were kept at vacuum (~10^{-6} mbar) for at least 30 min (or until pressure reached < $2*10^{-6}$ mbar) prior to deposition. For cells with CuPc as the donor layer, substrates were transferred to the thermal deposition chamber immediately after the baking of PEDOT:PSS, and kept at vacuum until deposition (evaporation rate ~1 Å/s). Interlayer materials (LiF and BCP) were deposited (evaporation rate ~0.5 Å/s) followed by the deposition of C_{60} (evaporation rate ~1 Å/s). Ag was added as the top contact of the device (evaporation rate ~1 Å/s) to create six individual testing pads, each with an active area of 0.15 cm^2. Devices were annealed at 150 °C on a hot plate for 30 min; some devices were tested before and after annealing.

In total, 10 devices were fabricated and tested. For each experiment, a standard control device was fabricated without the interlayer and one device was fabricated with the interlayer; a Si / PEDOT:PSS / P3HT (or CuPc) / LiF (or BCP) sample was fabricated with each device in order to investigate surface morphology. The following devices were fabricated and tested:

1) ITO / PEDOT:PSS (40 nm) / CuPc (20 nm) / LiF (2 nm) / C_{60} (40 nm) / Ag (65 nm)

2) ITO / PEDOT:PSS (40 nm) / P3HT (40 nm) / LiF (2 nm) / C_{60} (40 nm) / Ag (65 nm)

3) ITO / PEDOT:PSS (40 nm) / P3HT (40 nm) / BCP (9 nm) / C_{60} (40 nm) / Ag (65 nm)

4) ITO / PEDOT:PSS (40 nm) / P3HT (40 nm) / BCP (2.5 nm) / C_{60} (40 nm) / Ag (65 nm)

5) ITO / PEDOT:PSS (40 nm) / CuPc (20 nm) / BCP (2.5 nm) / C_{60} (40 nm) / Ag (65 nm)

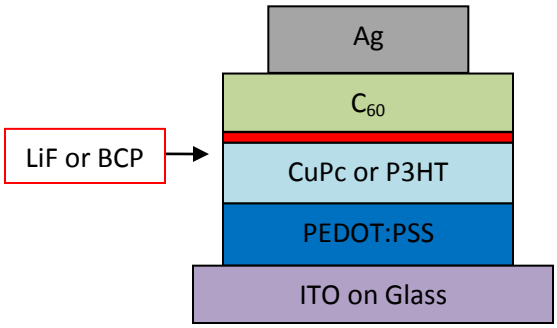


Figure 5. Solar cells fabricated in a stack formation. ITO on glass was used as the substrate.

3.4 Morphology and Film Thickness

To properly assess film thickness and deposition rate, each material was calibrated using an Inficon SQM -160 quartz crystal monitor (QCM) and atomic force microscopy (AFM; Digital Instruments Dimension 3100 operated in tapping mode) or ellipsometry (J.A. Woolam Co. VASE Ellipsometer). Materials were deposited onto a silicon substrate, and the thicknesses of the films were measured using AFM or ellipsometry. The QCM parameters were adjusted and tested until the QCM-measured thickness matched the physical thickness of each film. With each device, a clean silicon substrate was included in the fabrication process but removed after the deposition of the interlayer. The surface morphology of the interlayer on the donor was then investigated using AFM for nm-scale imaging, and an optical microscope (Olympus BX45) for μm-scale imaging.

3.5 Current-Voltage Testing

The current-voltage characteristics of each device were tested with and without illumination. Devices were removed from the glove box and placed in a black testing box (to block external ambient light) with the active layer of the device facing up towards an LED (from Lamina Titan RGB NT-53F0-0428). Using a Keithley 2602A System Sourcemeter, voltage was swept across the devices in 0.01 V increments from -0.5 V to 1.5 V, and the current was measured with the devices in the dark (dark-current). Devices were then illuminated under red, green, or blue light – with the LED powered at 800 mA (and corresponding LED-set voltage). For this LED model, the relative spectral distribution of each type of light is shown in Figure 6. Blue, green, and red light respectively reach peak power at ~460, 520, 635 nm; green light comprises the largest spectra of wavelengths. The incident power of each color of light corresponding to 800 mA current input was measured using a thermal power sensor (from ThorLabs PM100D). The incident power density of red, green, and blue light were respectively measured as 19 mW/cm^2, 15 mW/cm^2, and 35 mW/cm^2. Similar to the dark-current measurement, voltage was swept across the device, and the current of the device under illumination was measured (light current). Devices were in air for a maximum of 30 minutes.

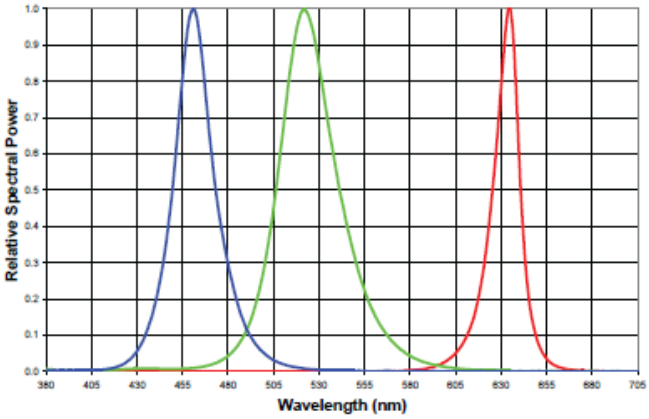


Figure 6. Lamina Titan RGB NT-53F0-0428 spectral distribution[15]

4 Results and Discussion

For multiple contact pads on each device, the open-circuit voltage (V_{OC}), short-circuit current density (J_{SC}), fill factor (FF), and monochromatic efficiency (η_L) were calculated. The values were averaged (when applicable) to characterize the overall device performance. In Table 1, for example, V_{oc} = 0.401 ± 0.006 (V) for a LiF-interlayer device under red light, where the reported value (0.401) is the average open-circuit voltage of multiple pads on this device plus or minus one standard deviation (0.006). During red-light illumination of CuPc-donor layer devices, it was observed that CuPc devices without the interlayer were far less efficient. Additionally, green and blue light were absorbed poorly by these devices, so multiple pads were not tested in some cases, as it was not considered pertinent to the investigation of the interlayer effects. The reported value for these cases is not an average, but rather a single value, so there is no standard deviation.

A current density (mA/cm^2) vs. voltage (V) plot was made for three different device sets in order to investigate device performance; similarly, a semi-log plot of the absolute value of current (Amps) vs. voltage (V) was made for the same devices to more easily see the difference in V_{OC} between the interlayer and standard devices. Furthermore, the semi-log plot exhibits the performance of the devices in the dark and under illumination. The highest η_L from the corresponding table was found, and a single pad that closely resembled the average V_{oc} and J_{SC} at that incident color was chosen as the plotted curve. AFM images are presented to explain morphological effects on these devices.

4.1 P3HT / LiF / C_{60} Active Layer

The interlayer device consisted of ITO / PEDOT:PSS (40 nm) / P3HT (40 nm) / LiF (2 nm) / C_{60} (40 nm) / Ag (65 nm), and the standard device consisted of ITO / PEDOT:PSS (40 nm) / P3HT (40 nm) / C*60* (40 nm) / Ag (65 nm). The performance characteristics of these devices under different colors of light are summarized in Table 1.

Table 1

Color of Light and Device	V_{OC} (V)	J_{SC} (mA/cm^2)	*FF*	η_L (%)
Red w/LiF	0.401 ± 0.006	-3.33 ± 0.12	0.433 ± 0.042	3.04 ± 0.42
Red no LiF	0.357 ± 0.004	-3.13 ± 0.49	0.380 ± 0.032	2.25 ± 0.54
Green w/LiF	0.410 ± 0.003	-5.60 ± 0.63	0.419 ± 0.024	6.25 ± 0.46
Green no LiF	0.367 ± 0.003	-5.40 ± 0.63	0.372 ± 0.007	4.85 ± 0.54
Blue w/ LiF	0.388 ± 0.008	-7.90 ± 0.639	0.364 ± 0.040	3.18 ± 0.47
Blue no LiF	0.349 ± 0.006	-8.46 ± 1.19	0.327 ± 0.017	2.71 ± 0.38

Under each color of light, the interlayer device (w/LiF) clearly has a higher V_{OC} than the standard device (no LiF) by an average of 11.7 %. The η_L of the interlayer device appears to be higher under the illumination of red and blue light but within the error range; under green light, the interlayer device exhibits a η_L that is higher than the standard device outside of the error range. Although the J_{SC} of the interlayer and standard devices are similar (within the error range) under green light, the η_L of the interlayer device is higher because of the increase of the V_{OC} and the *FF*.

The device efficiency is highest under green illumination. P3HT/C_{60} devices have a peak light-to-power conversion efficiency at approximately 490 nm and good power conversion efficiency from 480 to 530 nm, whereas below 490 nm, the efficiency drops off more rapidly.[10]

From Figure 6, it can be seen that at 490 nm green and blue exhibit equal spectral power distributions. Since the device has peak conversion efficiency around this wavelength, and good conversion over the LED green light wavelength range, it makes sense that the device would exhibit its highest η_L under green light. It should be noted that most solar-cell devices are typically tested under white light (sun-mimicking conditions) that contains various wavelengths that are not absorbed well by the solar cell. The monochromatic efficiency should not be judged as the efficiency at which the cell would perform under the sun – a value that would most likely be lower.

Figure 7 shows the current-density vs. voltage (*J*-*V*) characteristics of the interlayer device and the standard device under green light. The V_{OC} is higher for the interlayer device but the J_{SC} is lower (within the error range). Both devices clearly exhibit solar cell behavior.

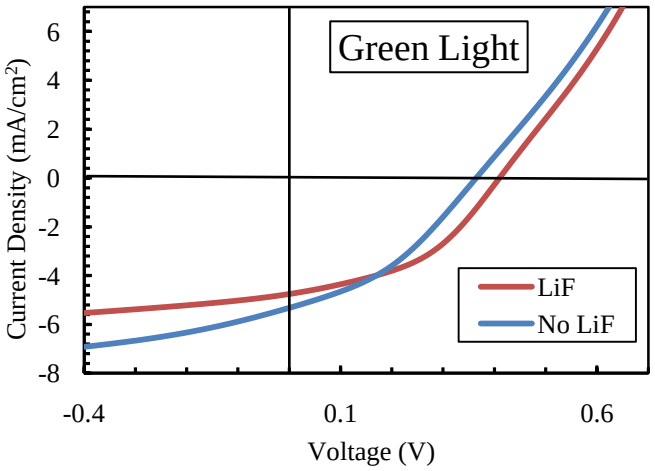


Figure 7. Current density (*J*) vs. voltage (*V*) characteristics of the interlayer device (LiF) and standard device (No LiF) illuminated with green light.

Figure 8 shows a semi-log plot of the absolute value of current vs. voltage for the interlayer device and standard device in the dark and under green-light. Both devices exhibit significant improvement in current response under illumination. The V_{OC} is the point at which the absolute value of current reaches a minimum. The increase in current and voltage under illumination show that both devices are acting as functional solar cells. The current under illumination of the interlayer device is lower

than that of the standard device up until about 0.5 V, where the two devices attain the same value.

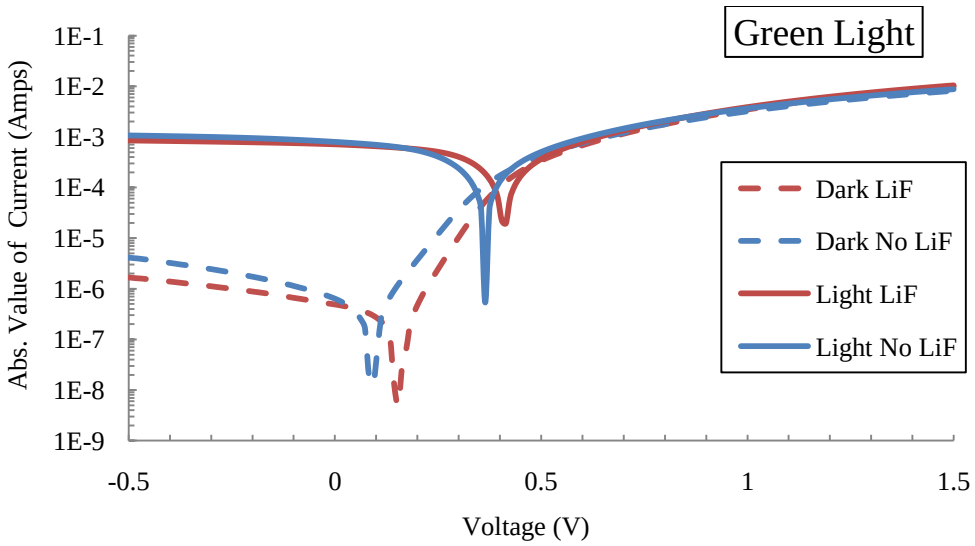


Figure 8. Semi-log plot of absolute value of current (Amps) vs. voltage (V) characteristics of the interlayer device (LiF) and standard device (No LiF) in the dark and illuminated with green light.

Figure 9 shows AFM height images of Si / PEDOT:PSS (40 nm) / P3HT (40 nm) / LiF (2 nm), Si / PEDOT:PSS (40 nm) / P3HT (40 nm) / C_{60} (40 nm), and ITO / PEDOT:PSS (40 nm) / P3HT (40 nm) . The surface height of LiF on P3HT varies more than that of C_{60} on P3HT or P3HT only, as judged by the much brighter spots on the LiF image. When LiF is deposited onto P3HT, small granules appear to form, as can be seen from the textured circular features in the AFM image. LiF is most likely not forming a uniform layer, and is accumulating in clusters on the P3HT surface. C_{60} appears to form circular globules on P3HT with similar surface height. P3HT alone has the least amount of surface height variation.

Although the LiF layer is by far the thinnest film at 2 nm, the surface displays the most variability in height. Since the surface height seems to reach its peak in clusters of granules, it might be possible that LiF is diffusing into P3HT, thus creating micropores that would account for the variation in surface height. If this were the case, upon depositing C_{60} onto the LiF-interlayer device, C_{60} would fill P3HT/LiF micropores. Unlike the P3HT / C_{60} active layer, which exhibits a more planar interface between the two materials, based on the globules and lowered surface height, the P3HT / LiF / C_{60} active layer would have a structure that resembles interlocked-fingers. Therefore, the P3HT / LiF/ C_{60} device would have more surface contact area between the donor and acceptor and allow for increased electron-hole separation into mobile charge carriers. This effect would increase the efficiency of the device. Alternatively, the cell performance may not strongly depend on the surface morphology at the interface of LiF and P3HT. A V_{OC} improvement of up to 0.4 V has been observed upon 5 Å interlayer insertion, but

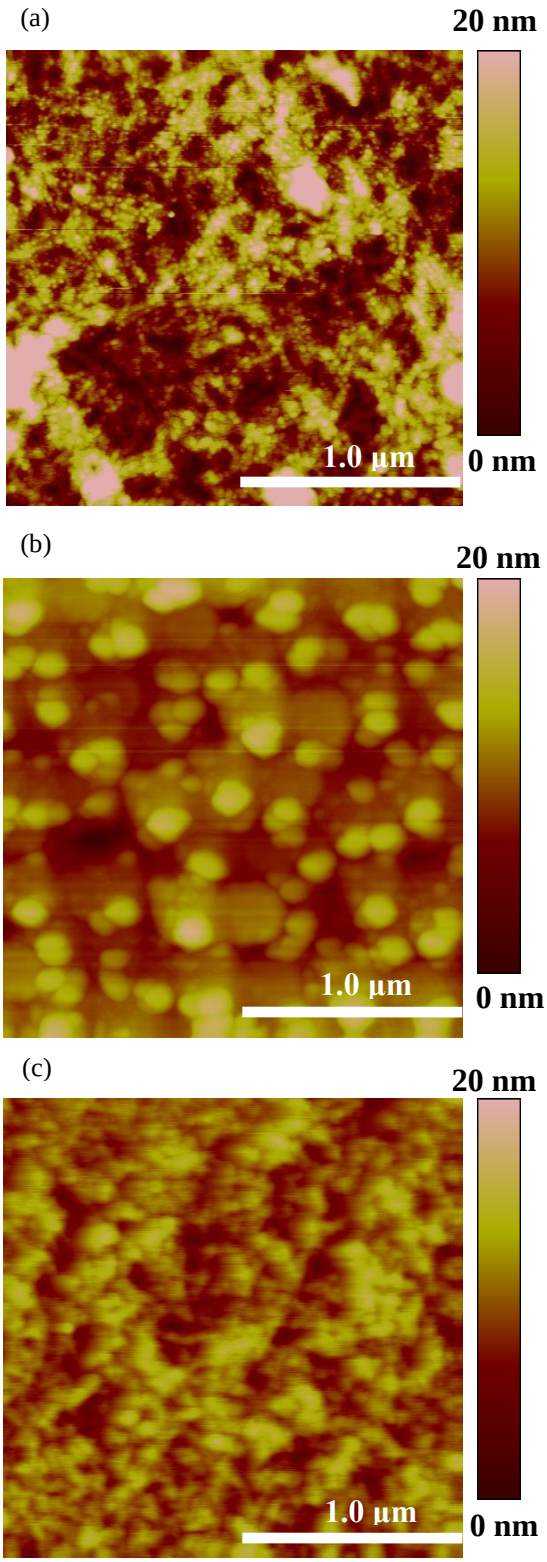


Figure 9. AFM images of (a) P3HT / LiF; (b) P3HT / C_{60}; (c) P3HT. Height varies on a 0-20 nm color scale.

with a decrease in J_{SC} of ~4 mA/cm^2; this effect was attributed to band bending of the acceptor and donor materials.[6] Band bending could similarly be the cause of the observed increase in V_{OC} upon insertion of the LiF interlayer.

4.2 P3HT / BCP / C_{60} Active Layer

Two BCP-interlayer devices were tested. The first device consisted of ITO / PEDOT:PSS (40 nm) / P3HT (40 nm) / BCP (9 nm) / C_{60} (40 nm) / Ag (65 nm); the second device consisted of the same materials except with a 2.5 nm interlayer of BCP and a 2.5 nm BCP exciton blocking layer between C_{60} and Ag. Although both devices behaved as diodes in the dark, under illumination neither produced power under forward bias. This implies that although the device is able to generate free charge carriers when illuminated, the charge carriers cannot be collected at the anode and cathode. In effect, the addition of the BCP interlayer is interfering with charge collection by increasing the resistivity of the active layer. To make sure that this performance was not a result of human error during fabrication, the standard devices were tested and performed similarly to previous standard P3HT / C_{60} devices. The morphology of BCP was also analyzed to determine why the BCP-interlayer devices failed to produce power.

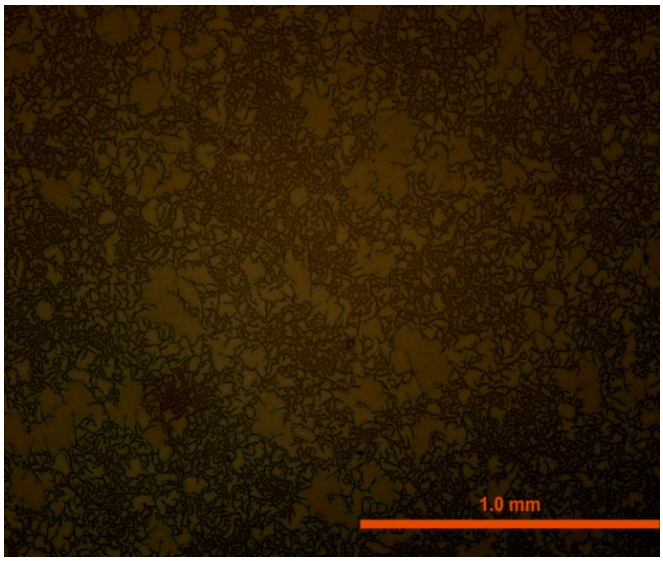
The surface morphology of the Si / PEDOT:PSS (40 nm) / P3HT (40 nm) / BCP (9 nm) and Si / PEDOT:PSS (40 nm) / P3HT (40 nm) / BCP (2.5 nm) samples were investigated using the optical microscope. Figure 10 displays the microscopic images of the two samples. The surface of the 9 nm BCP sample exhibits multiple branched rods. An AFM scan over a rod showed a variation in surface height of up to 200 nm – an unrealistic measurement considering that the total thickness of the deposited layers is only ~84 nm. The AFM software had difficulty tracking properly over the rod, so the 200 nm measurement is most likely not accurate. It is

possible that the BCP diffused through the P3HT and PEDOT:PSS layers, so that pinholes were created from the BCP surface down to the Si surface, thus creating height variation on the scale of the total thickness of the deposited materials.

Orange dots were observed on the surface of the 9 nm BCP sample. The P3HT solution is orange but turns a purplish color after drying. From this observation, it was speculated that the P3HT did not adequately dry prior to deposition of the BCP interlayer; this may have caused the branched rods.

As shown in Figure 11, a transparent region surrounding the cathode was observed on both the interlayer device and standard device, an effect presumably caused by evaporation around the electrodes during annealing. Taking these two factors into account, subsequently-fabricated BCP devices were subjected to longer P3HT drying times, and tested before and after annealing.

(a)



(b)

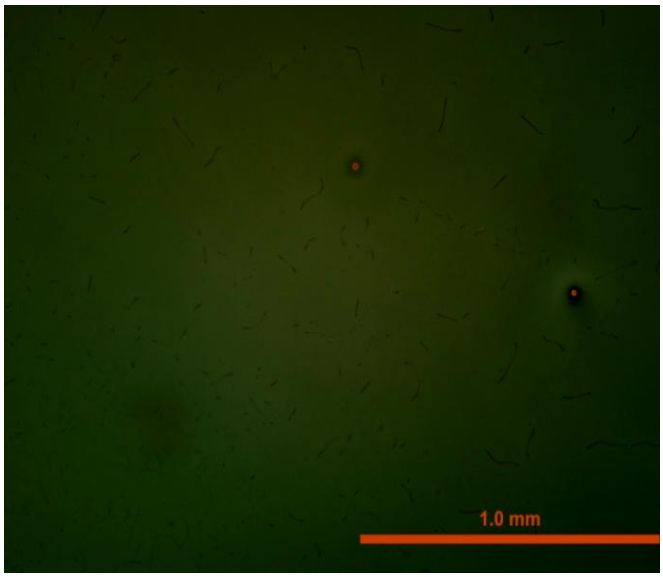


Figure 10. Microscopic images of (a) BCP (9 nm) on P3HT and (b) BCP (2.5 nm) on P3HT

As previously mentioned, the ITO / PEDOT:PSS (40 nm) / P3HT (40 nm) / BCP (2.5 nm) / C_{60} (40 nm) / BCP (2.5 nm) / Ag (65 nm) device failed to perform like a solar cell before or after annealing, even though the P3HT layer was subjected to ~8 hours of drying. Therefore, the addition of the BCP interlayer must be the cause of lower performance. It is likely that the BCP is creating pinholes (contact between the anode and cathode) in the device that cause a short circuit, or that the BCP reduces the conductivity of the device.

The clear area around the cathode, as observed with the previous 9 nm BCP interlayer and standard device, was visible on the 2.5 nm BCP interlayer device only after annealing; the standard device did not exhibit the clear area around the cathodes before or after annealing. Whether the addition of a BCP interlayer contributes to this effect is uncertain, since a standard device (containing no BCP) also exhibited a clear region around the cathode after annealing. It is possible that when the device was tested pre-annealing in air, silver oxidized to form Ag_2O, and Ag_2O could have caused degradation of the active layer during annealing.

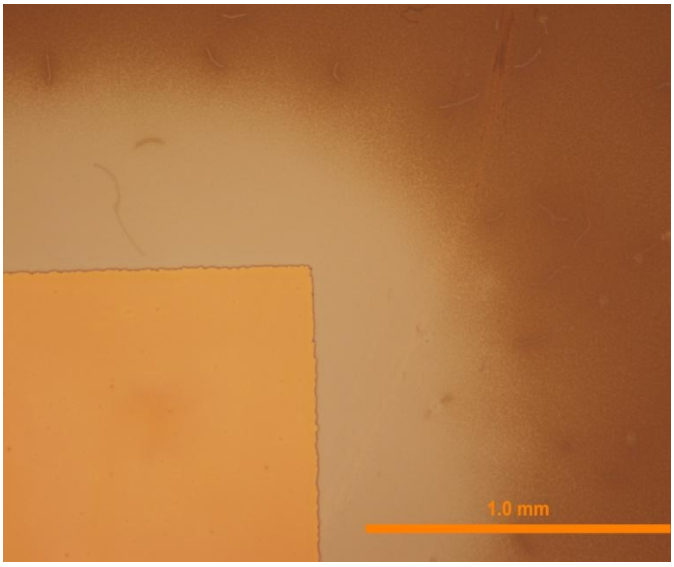


Figure 11. Microscopic image of the Ag cathode surrounded by a transparent region. The bright orange square is the cathode and the brown area is the solar cell area between cathodes.

The surface of the PEDOT:PSS (40 nm) / P3HT (40 nm) / BCP (2.5 nm) still displayed rods (without branching) and orange dots, despite the fact that P3HT was dried for ~8 hrs and a 2.5 nm layer of BCP was added. This surface morphology re-emphasizes the fact that BCP must create pinholes, or vacancies in the active layer. Presumably, 8 hrs is a sufficient length of

time to allow P3HT to dry, and the orange dots seen on the surface must be a result of P3HT melting and reorganizing as BCP condenses on the P3HT surface. Alternatively, a study done by Chen et. al demonstrated that the annealing of PCBM on P3HT at 150 °C for 30 min results in the formation of long needle-like structures with bright centers.[16] The authors concluded that these needles were in fact PCBM molecules that had segregated from P3HT and crystallized. Although no annealing was performed on the BCP sample tested in this case, BCP could be crystallizing on the surface of P3HT immediately upon condensation during deposition. Considering that these rod-like structures form without annealing, favorable surface morphology between BCP and P3HT is thermodynamically limited. In summary, the P3HT / BCP / C_{60} active-layer devices investigated do not generate power upon absorption of light and exhibit unfavorable surface morphology.

4.3 CuPc / LiF / C_{60} Active Layer

The interlayer device consisted of ITO / PEDOT:PSS (40 nm) / CuPc (20 nm) / LiF (2 nm) / C_{60} (40 nm) / Ag (65 nm), and the standard device consisted of the same structure without the interlayer. The performance characteristics of these devices under different colors of light are summarized in Table 2.

Table 2

Color of Light and Device	V_{OC} (V)	J_{SC} (mA/cm^2)	*FF*	η_L (%)
Red w/LiF Red no LiF	0.568 ± 0.031 0.554 ± 0.016	-2.95 ± 0.47 -4.00 ± 0.56	0.337 ± 0.036 0.309 ± 0.013	3.02 ± 0.88 3.61 ± 0.70
Green w/LiF Green no LiF	0.557 0.526	-0.669 -1.20	0.334 0.321	0.830 1.39
Blue w/ LiF Blue no LiF	0.555 0.543	-1.50 -3.30	0.299 0.293	0.703 1.48

Under all colors of light, η_L is higher for the standard device, though under red light the η_L values fall within the experimental range of each other. The V_{OC} is higher for the interlayer devices under green and blue light, but without multiple test pads over which values can be averaged it is difficult to conclude that the V_{OC} has been increased by the addition of the LiF interlayer. In all cases, the J_{SC} has distinctively been reduced by the addition of the LiF interlayer. The fill-factors for both devices appear to be relatively similar, and for the case of red light, the values fall within the experimental range of each other.

The peak absorption wavelength of CuPc is at ~620 nm, and the LED generates red light with a peak power at ~635 nm.[11] As expected, the devices exhibit the highest η_L under red light because of their ability to absorb more photons than when illuminated with blue or green light.

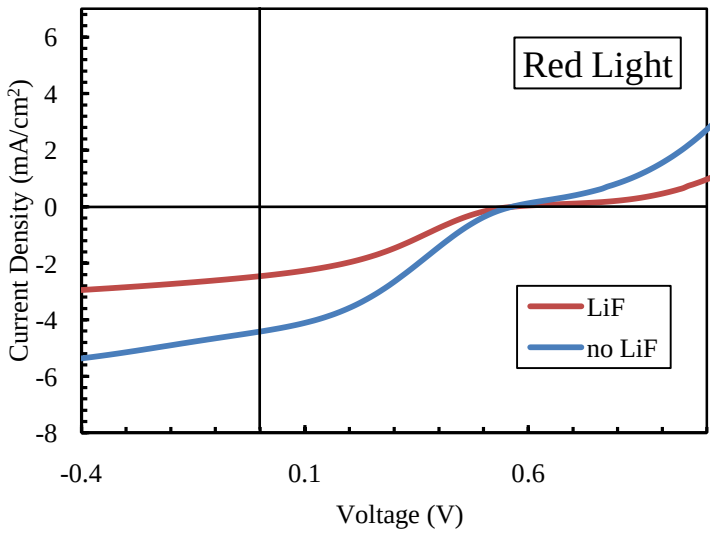


Figure 12. Current density (J) vs. voltage (V) characteristics of the interlayer device (LiF) and standard device (No LiF) illuminated with red light.

Figure 12 shows the J-V characteristics of the interlayer device and the standard device under red light. The V_{OC} of both devices are approximately the same, but the current density of the interlayer device is almost half of the current density of the standard device; this specific pad on the standard device had an exceptionally high J_{SC}. Both curves exhibit s-shapes, which can be caused – among other

reasons – by plasma etching between 10 and 100 s.[17] These two devices were the first fabricated and tested for this research study, and all subsequent devices were subjected to ~ 15 s of O_2 during the cleaning process.

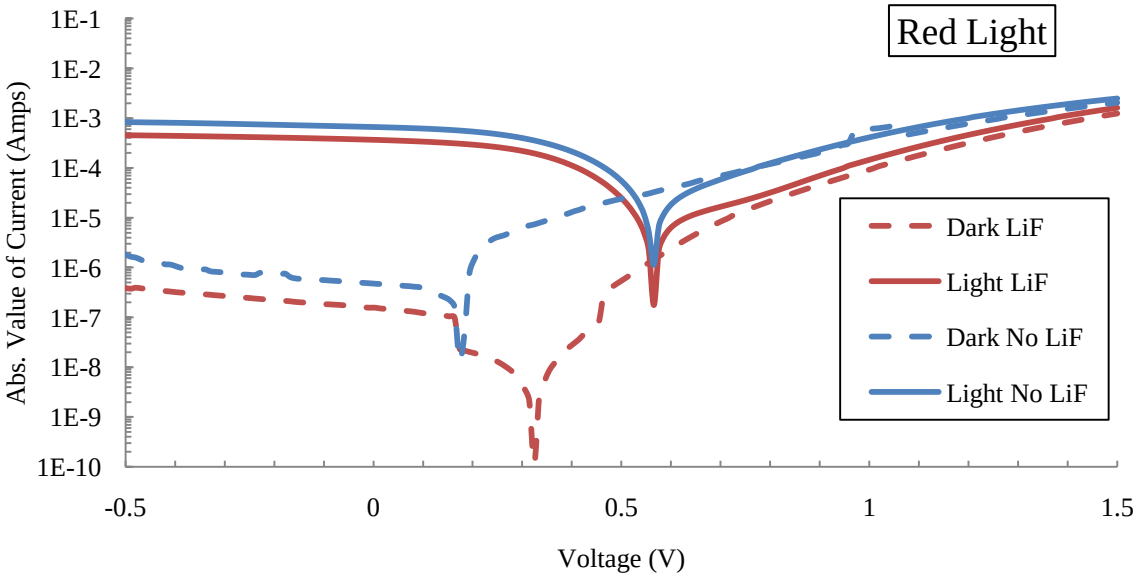


Figure 13. Semi-log plot of absolute value of current (Amps) vs. voltage (V) characteristics of the interlayer device (LiF) and standard device (No LiF) in the dark and illuminated with red light.

Figure 13 shows a semi-log plot of the absolute value of current vs. voltage for the standard device versus the interlayer device in the dark and under red light. Both devices exhibit significant improvement in current response under illumination. The V_{OC} of each device is approximately the same, as can be seen at the minimum current of the two device curves under illumination. The current of the standard device is higher than that of the interlayer device.

The tabulated values and *J-V* plots show that the V_{OC} remained unchanged with the addition of the interlayer, and that the J_{SC} and η_L were reduced by the addition of the interlayer. The combination of these two factors shows that the interlayer device is less efficient than the standard device, most likely due to reduced conductance of the active layer.

4.4 CuPc / BCP / C_{60} Active Layer

The interlayer device consisted of ITO / PEDOT:PSS (40 nm) / CuPc (20 nm) / BCP (2.5 nm) / C_{60} (40 nm) / Ag (65 nm), and the standard device consisted of the same structure without the interlayer. The performance characteristics of these devices under different colors of light are summarized in Table 3.

Table 3

Color of Light and Device	V_{OC} (V)	J_{SC} (mA/cm^2)	*FF*	η_L (%)
Red w/ BCP Red no BCP	0.509 ± 0.059 0.549 ± 0.004	-1.13 ± 0.12 -4.03 ± 0.45	0.354 ± 0.003 0.345 ± 0.004	1.08 ± 0.12 4.01 ± 0.45
Green w/BCP Green no BCP	0.519 0.514	-0.208 -0.885	0.330 0.332	0.237 1.01
Blue w/ BCP Blue no BCP	0.494 ± 0.061 0.542 ± 0.006	-0.402 ± 0.169 -2.65 ± 0.49	0.315 ± 0.024 0.291 ± 0.000	0.173 ± 0.062 1.19 ± 0.22

The V_{OC} is nearly the same for both devices under green light, but lower for the interlayer device when under red or blue light, though within the error range. Although the fill factors are virtually the same for both devices under green light, the fill factor is slightly higher for the interlayer device under red and blue light. It is clear that J_{SC} and η_L are lower for the interlayer device under all colors of light.

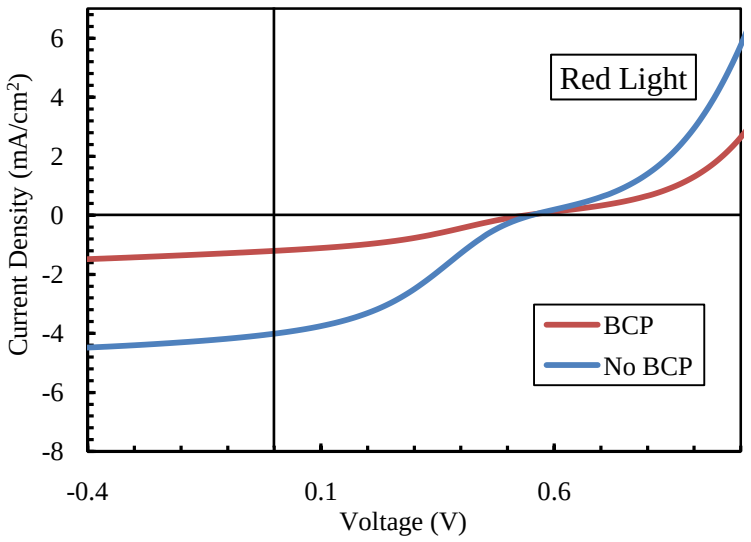


Figure 14. Current density (*J*) vs. voltage (*V*) characteristics of the interlayer device (BCP) and standard device (No BCP) illuminated with red light.

Firgure 14 shows the *J-V* characteristics of the interlayer device and the standard device under red light. The V_{OC} of both devices are approximately the same, but the J_{SC} of the interlayer device is almost a quarter of the standard device's J_{SC}. Both curves still display s-shaped behavior, despite being subjected to only 15 s of O_2 plasma. Multiple reasons have been cited for the cause of s-shape curves, including fast cathode deposition rates (40 nm/s) and barrier regions to charge carrier transport.[17,18] Since the cathode was deposited slowly, and s-shape behavior was not exhibited with P3HT based devices, the interface between CuPc and PEDOT:PSS could act as a barrier to hole transport, and the optimal thickness of PEDOT:PSS with CuPc should be investigated. Furthermore, the active layer might have oxidized during testing in air, which could have contributed to the s-shape behavior.

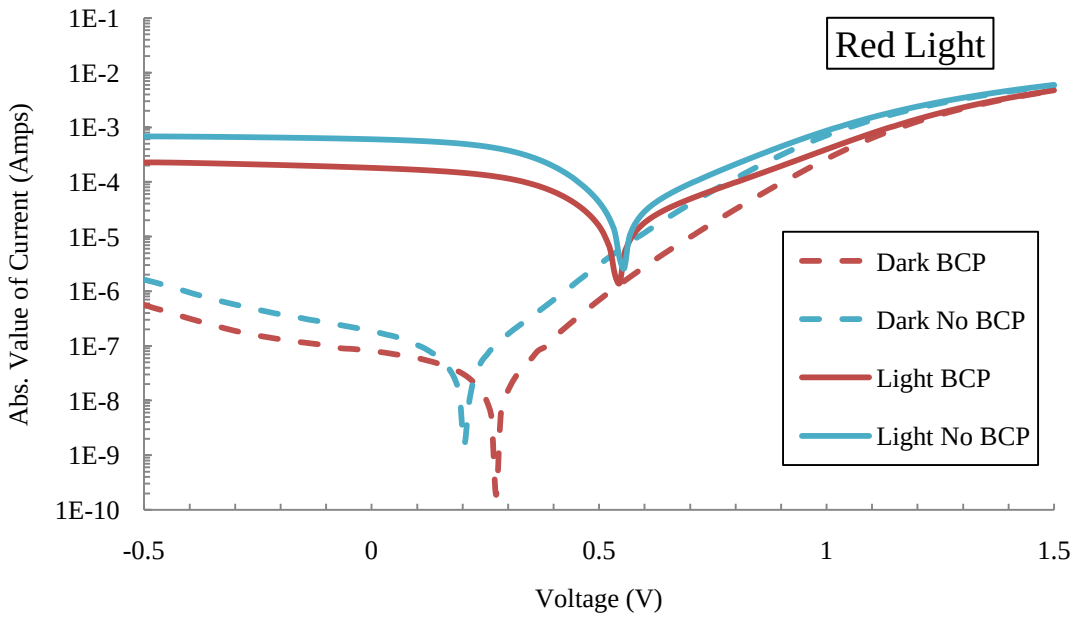


Figure 15. Semi-log plot of absolute value of current (Amps) vs. voltage (V) characteristics of the interlayer device (BCP) and standard device (No BCP) in the dark and illuminated with red light.

Figure 15 shows a semi-log plot of the absolute value of current vs. voltage for the standard device versus the interlayer device in the dark and under red light. Both devices generate more current when illuminated. Relative to the *J-V* plot, the standard device's V_{OC} is more apparent. The semi-log plot re-emphasizes the findings from the table and *J-V* plot; the J_{SC} and V_{OC} are both reduced by the addition of the interlayer.

These results show that the addition of the BCP interlayer negatively effects device performance. AFM imaging (Figure 16) shows that BCP forms a relatively uniform layer on CuPc. The layer exhibits consistent granules across the surface, and is relatively smooth. With a smooth layer of BCP, the active layer resembles that of a theoretical stacked-layer device, where CuPc, BCP, and C_{60} have planar interfaces. Potentially, a rough interlayer, as seen with P3HT / LiF, could be preferential to a smooth layer because the donor-acceptor interface area can be increased with structural rearrangement at the interface. Although CuPc / LiF surface images were not obtained, this interface could also form a smooth layer that would reduce contact area between CuPc and C_{60}, thereby reducing the J_{SC} and V_{OC}. Spectroscopic methods are necessary to conclusively observe band bending and fully describe the reasons for which CuPc / LiF (or BCP) active-layer devices performed poorly.

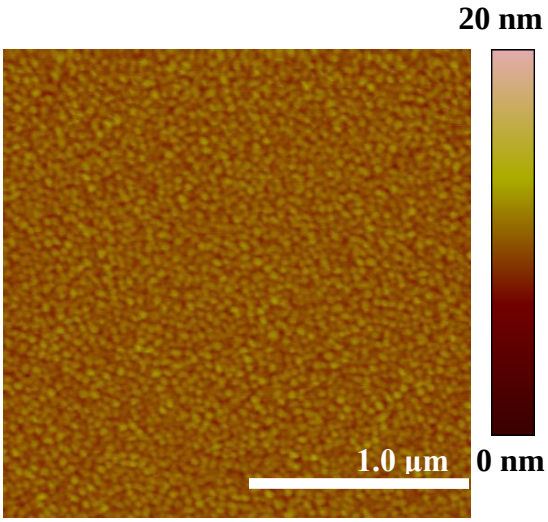


Figure 16. AFM image of BCP on CuPc.

5 Conclusions and Recommendations

A thin layer of LiF or BCP was inserted between the donor-acceptor interface in OSCs with the goal of boosting the V_{OC}. The insertion of LiF (2 nm) into a P3HT / C_{60} acceptor-donor OSC resulted in an 11.7% improvement in the V_{OC} without exhibiting a decrease in the J_{SC}. The improvement in V_{OC} can be attributed to preferential morphological changes at the interface of P3HT and LiF. Though not explored, band bending could be the main cause of V_{OC} improvement, as it has been observed by other research groups. The insertion of BCP (9 nm and 2.5 nm) into a P3HT / C_{60} acceptor-donor OSC resulted in devices that did not generate power. These results can be attributed to reduced device conductance caused by BCP and unfavorable surface morphology, where branched, rod-like BCP structures either created pinholes or segregated from the P3HT layer. Similarly, CuPc / BCP or LiF / C_{60} devices failed to exhibit V_{OC} or η_L improvement.

Since a boost in V_{OC} was accomplished by the insertion of a LiF interlayer into a P3HT / C_{60} active-layer OSC, additional research should be conducted to further analyze the reasons for the increase in V_{OC}. This experiment should be replicated multiple times to ensure that the device performs consistently. To further investigate the effects of band bending, the LiF thickness could be reduced (< 1 nm) and inspected with spectroscopic methods such as ultraviolet photoemission spectroscopy and x-ray photoemission spectroscopy.

The CuPc-donor and BCP-interlayer devices revealed many unexpected results, such as s-shaped curves and unfavorable surface morphologies. Oxidation of the active layer or cathode could have been the cause of s-shape curve behavior and requires further analysis.

It should be noted that the Si / PEDOT:PSS / P3HT (or CuPc) / LiF (or BCP) samples used for surface morphology analysis were not annealed, but some devices were tested only after

annealing. Therefore, these samples could be re-fabricated and observed after annealing. Investigation of the optimal annealing temperature for specific combinations of materials should also be considered based on the observation of a transparent region around the cathodes in some devices. Overall, the goal of boosting the open-circuit voltage was achieved via the insertion of a LiF interlayer, creating opportunities for future work in the advancement of bilayer OSCs.

6 Acknowledgements

The author would like to thank Tufts University and the Office of the Provost for funding the Summer Scholars program, under which this research began. The author gives a special thanks to Professor Matthew Panzer, whose mentorship and expertise helped make this project a success.

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