Modeling Asynchronous Sigma-Delta Modulators

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Abstract

This thesis studies *asynchronous sigma-delta modulators (ASDM)* which are the core part of *asynchronous sigma-delta converters (ASDC)*. The asynchronous sampling techniques provide a low power, clock-less data acquisition approach with a less sophisticated design constrains offering significant power savings while keeping increasing speed in scaled deep submicron technologies.

Our contribution in this thesis is briefly listed as below:

1) thoroughly analyzed the different error sources in a bi-level ASDM
2) compared multi-level ASDM with bi-level ASDM
3) introduced the band-pass ASDM and analyzed it

Commonly, ASDCs consist of two main parts:

1) a *duty-cycle modulator (DCM)* which transforms amplitude information of the input signal to the time information

2) a time-*to-digital converter (TDC)* following the DCM unit which quantizes and digitizes the time information.

Mainly focusing on the DCM part of ASDCs, in the first part of this thesis, after discussing the architecture of ASDMs, it has been shown that they are an acceptable realization of DCMs. In following, we evaluate different types of errors affecting

performance of such systems. We have shown that how fixed and dynamic errors affect the performance of the ASDM.

The second part of the thesis is focused on alternative architectures of ASDMs. A *multi-level asynchronous sigma-delta modulator (ML-ASDM)* generates a multi-level square wave signal whose duty-cycle is modulated by input signal. The resulting signal can be then quantized by any following TDC block. We have proved that in a ML-ASDM converting input amplitude information to multi-level duty-cycle modulated square waves not only doesn't help improving the performance of the modulator but also it introduces non-harmonic distortion in the band of interest which drastically degrades the performance of the modulator, compared with bi-level ASDM.

Another different ASDM structure discussed in this report is a *band-pass asynchronous sigma-delta modulator (BP-ASDM)*. This type of ASDM, for the first time, is introduced in this thesis. It is targeted to be implemented in narrow-band radio-frequency applications. In case of implementing a high resolution TDC, we have shown that this type of modulator helps converting high-frequency signals to digital domain.

This thesis is dedicated to:

My dearest Wife and Family,

whose love and support have been the main driving force of whatever little I have achieved.

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Terms and Abbreviations

Abbreviation	Definition
ASDM	Asynchronous Sigma-Delta Modulator
ADC	Analog-to-Digital Converter
BP-ASDM	Band-Pass Asynchronous Sigma-Delta Modulator
DAC	Digital-to-Analog Converter
DCM	Duty-Cycle Modulator
FS	Full Scale
MD	Modulation Depth
ML-ASDM	Multi-Level Asynchronous Sigma-Delta Modulator
OCR	Over Cycling Rate
OF	Overlap Factor
OSR	Over Sampling Rate
PWM	Pulse-Width Modulator
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
TDC	Time-to-Digital Converter
TDM	Time-Decoding Machine
TEM	Time-Encoding Machine

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Chapter 1

Introduction

The ongoing down-scaling of the minimum feature size of transistor processes necessitates scaling down supply voltages accordingly to reduce power dissipation and increase reliability. However, this reduction in power supply results in continuing decrease in dynamic range of *analog-to-digital converters (ADC)*. Decreasing dynamic range, in turn results in reduction in quantization steps, making the design process more difficult. Moreover, this reduction in the supply voltage also increases the power consumption of analog circuits even when the required performance is kept constant [1]. Therefore, designers try to shift the resulting analog complexities toward the digital domain to decrease power consumption while increasing speed and accuracy. On the other hand, this reduction in minimum feature size comes with increase in time resolution. This feature has led to the use of over sampled ADCs where amplitude information of a signal is converted to time information, one-by-one. A high-precision amplitude quantizer is replaced with a coarse quantizer, typically a 1-bit comparator, within a feedback loop that is oversampled, which significantly reduces the analog complexity while preserving signal resolution. That is, instead of quantizing instantaneously, amplitude information is converted to time information which is then decoded to full resolution using low power digital circuits [2].

In this thesis, in addition to re-citing a typical method of amplitude to time conversion reported in the literature, our contribution is:

4) thoroughly analyzed the different error sources in a bi-level ASDM
5) compared multi-level ASDM with bi-level ASDM
6) introduced the band-pass ASDM and analyzed it

In the following, we will more disclose our contribution in this thesis.

To map amplitude information into the time domain, a modulated square wave with a *time-variant period*, $T(t)$, and a *time-variant pulse* width, $\alpha(t)$, can be employed. As can be seen in Figure 1-1, an ideal *duty-cycle modulator (DCM)* transforms amplitude information of the input signal to time-variant duty-cycle square wave pulses:

$$\frac{\alpha(t)}{T(t)} = \frac{v(t)+1}{2} \tag{1-1}$$

$$\frac{\omega_i(t)}{\omega_c} = 1 - v(t)^2 \tag{1-2}$$

where ω_c is a constant *center frequency* while there is no input signal; $v(t) = 0$ [3]. This center frequency is called *limit-cycle frequency*. As we will discuss in the next chapter, this frequency plays a key role in the design of such a modulator.

To realize such duty-cycle modulators, *asynchronous sigma- delta modulators (ASDM)* are reportedly used in the literature. As depicted in Figure 1-2, clock-less ASDMs have no quantizer inside the loop unlike their clocked counterparts,

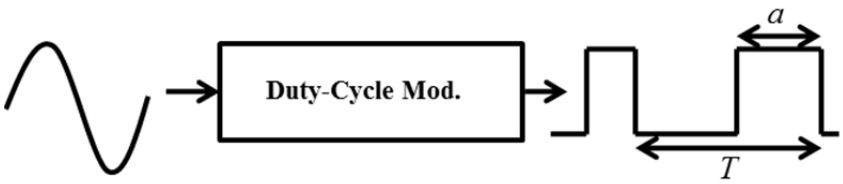


Figure 1-1: Ideal Duty-Cycle Modulator

continuous-time sigma-delta modulators (CT-SDM). In the former, the quantization process happens in the *time-to-digital converter (TDC*) following the sigma-delta loop. The benefit of placing the time quantizer in the loop is shaping the quantization noise out of the band of interest and improving *signal to noise and distortion ratio (SNDR)*. This may seem as disadvantage of ASDM equipped ADC's, but it helps design a more relaxed and reliable analog loop by eliminating the clock and sample-and-hold circuit from the loop. The quantization process takes place in a higher resolution TDC right after the loop.

However, because of some structural nonlinearity in the nature of asynchronous sigma-delta modulators, they are not fully matched with the characteristics of an ideal duty-cycle modulator but they show acceptable results. In chapter 2, these non-idealities are discussed in more detail.

Like continuous–time sigma-delta modulators, various architectures of asynchronous sigma-delta modulators can be implemented. Chapter 3 discusses two alternative architectures of ASDMs including multi-level and band-pass modulators.

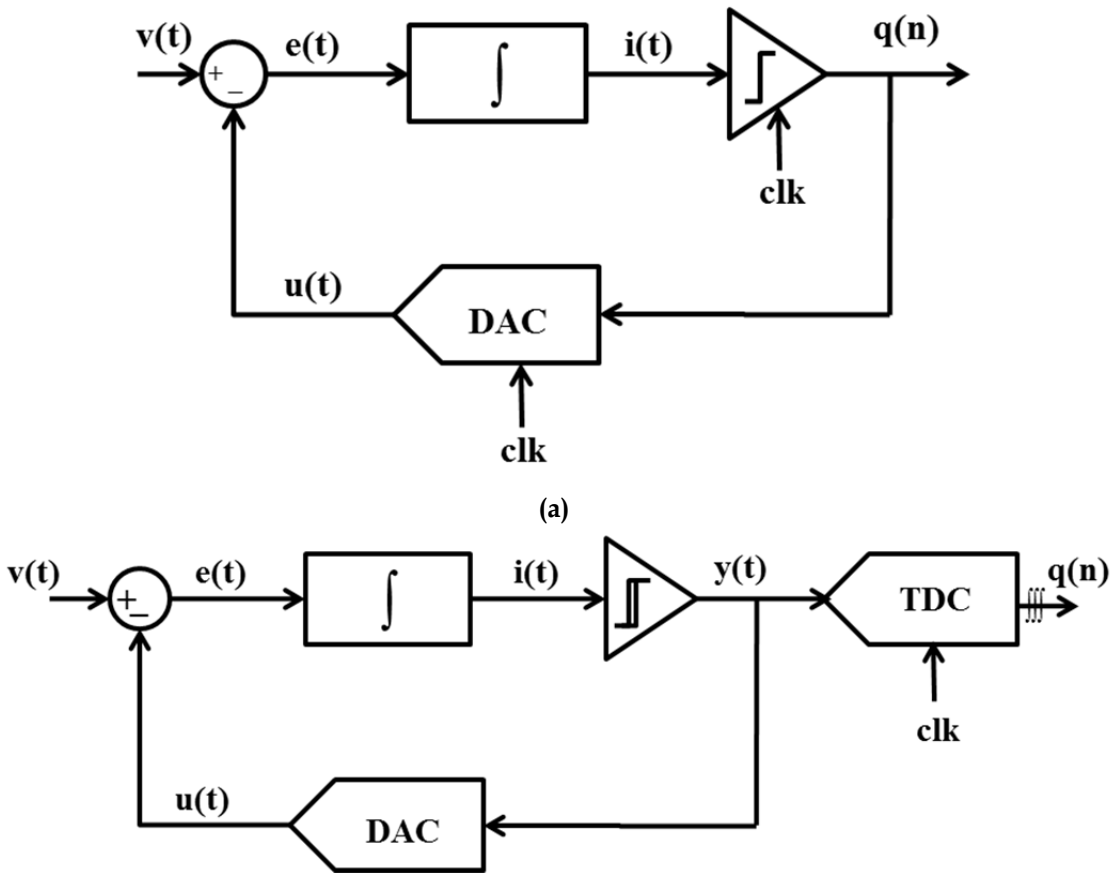


Figure 1-2: A comparison between CT-SDM-based ADCs and ASDM-based ADCs (a) a 1-bit first-order CT-SDM-based ADC, (b) an ASDM following an N-bit TDC

In the continuous–time sigma-delta modulators, higher *over sampling ratio (OSR)* yields a higher SNDR over the band of interest. That is, higher input signal frequency needs a higher clock rate to achieve a more accurate result. OSR's on the order of 16 to 32 are the highest achievable with today's fabrication technology. To make up for this low oversampling ratio and achieve high dynamic ranges, multi-bit DACs are needed [4]. Our study on the ML-ASDMs shows that this idea is not valid for ASDMs in general.

A detailed review on the architecture of the *band-pass sigma-delta asynchronous modulators (BP-ASDM)* is presented in chapter 3. Advantages and difficulties of designing a BP-ASDM are discussed in this chapter. This type of ASDM is not reported in the literature yet and is a novel approach presented for the first time in this thesis.

Finally, we sum up the results achieved during this study and suggest research directions for future studies.

1.1.Performance Metrics

Here we briefly present the performance metrics that we used to qualify the output results of the tested modulators and ADCs. The metrics mentioned here are based on spectrum calculations for a single tone signal.

1.1.1. Signal to Noise and Distortion Ratio (SNDR)

Signal to noise and distortion ratio (SNDR) is the ratio of the power of the fundamental signal to the total noise and distortion power within a certain frequency band, i.e.

$$SNDR = 10 \times \log(\frac{signal\ power}{noise\ and\ distortion\ power}) \quad (1\text{-}3)$$

To measure the noise and distortion power, based on the Parseval's theorem, the power of the each frequency bin of the output spectrum (except for the fundamental) is integrated over the band of interest.

1.1.2. Spurious-Free Dynamic Range (SFDR)

Measured over a certain band of frequency, *spurious-free dynamic range (SFDR)* is ratio of the power of the fundamental to the power of the highest frequency tone appeared in the band, i.e.

$$SFDR = 10 \times \log(\frac{signal\ power}{biggest\ spurious\ power}) \quad (1\text{-}4)$$

1.1.3. Signal to Noise Ratio (SNR)

Signal to noise ratio (SNR) is the ratio of the signal power to the noise power measured over a certain band of frequency, i.e.

$$SNR = 10 \times \log(\frac{signal\ power}{noise\ power}) \quad (1\text{-}5)$$

Chapter 2

Modeling and Analyzing Asynchronous Sigma-Delta Modulators

2.1. Introduction

Synchronous signal processing requires an analog-to-digital converter to transform an analog input signal into a discrete data set that can be processed using digital signal processors. The analog input signal must be sampled at twice rate of its maximum bandwidth component to accurately characterize the signal.

Downscaling of CMOS technologies makes analog circuits more complex and difficult to design. Therefore, it is desirable to shift these analog complexities toward the digital domain and take the advantage of the low power consumption digital circuits [1]. On the other hand, shrinking CMOS technology increases the timing resolution which can be utilized to meet high precision analog-to-digital conversion requirements, as mentioned in Chapter 1. That is, the amplitude information of an input analog signal can be converted to timing information using an ideal duty-cycle modulator. Then, using a high precision time-to-digital converter, it can be quantized and digitized. Finally, amplitude information of the original signal can be recovered from the output signal of the time-to-digital converter (Figure 2-1).

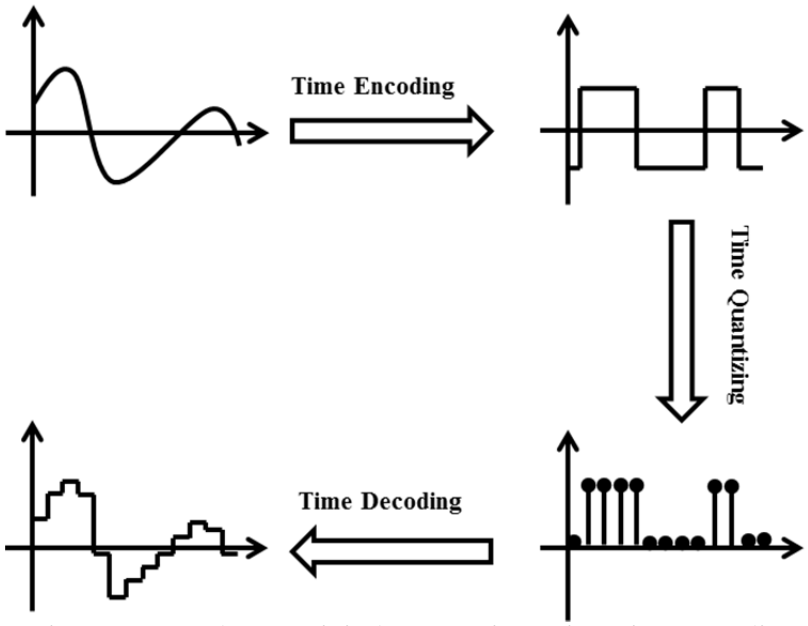


Figure 2-1: Analog-to-Digital Conversion using Time Encoding

To realize such a duty-cycle modulator, time-*encoding machines (TEM)* must be employed [3]. Different types of TEMs are reported in the literature but *asynchronous sigma-delta modulators (ASDM)* are widely used as a nearly perfect duty-cycle modulator [5].

In Figure 2-2(a), a typical model of a bi-level ASDM is demonstrated. If a single tone sinusoidal signal is applied as the input signal, such as the signal in Figure 2-2(b), then the error signal resulted from subtracting feedback signal from input signal looks same as Figure 2-2(c). Then, this error signal is filtered out by the low-pass filter, resulting in Figure 2-2(d). The output of the low-pass filter is limited to hysteresis values $\pm h$ (in Figure 2-3 the hysteresis parameters are demonstrated) and when it reaches to any of these values it forces the comparator toggle its output. Figure 2-2(e) shows the output of the comparator.

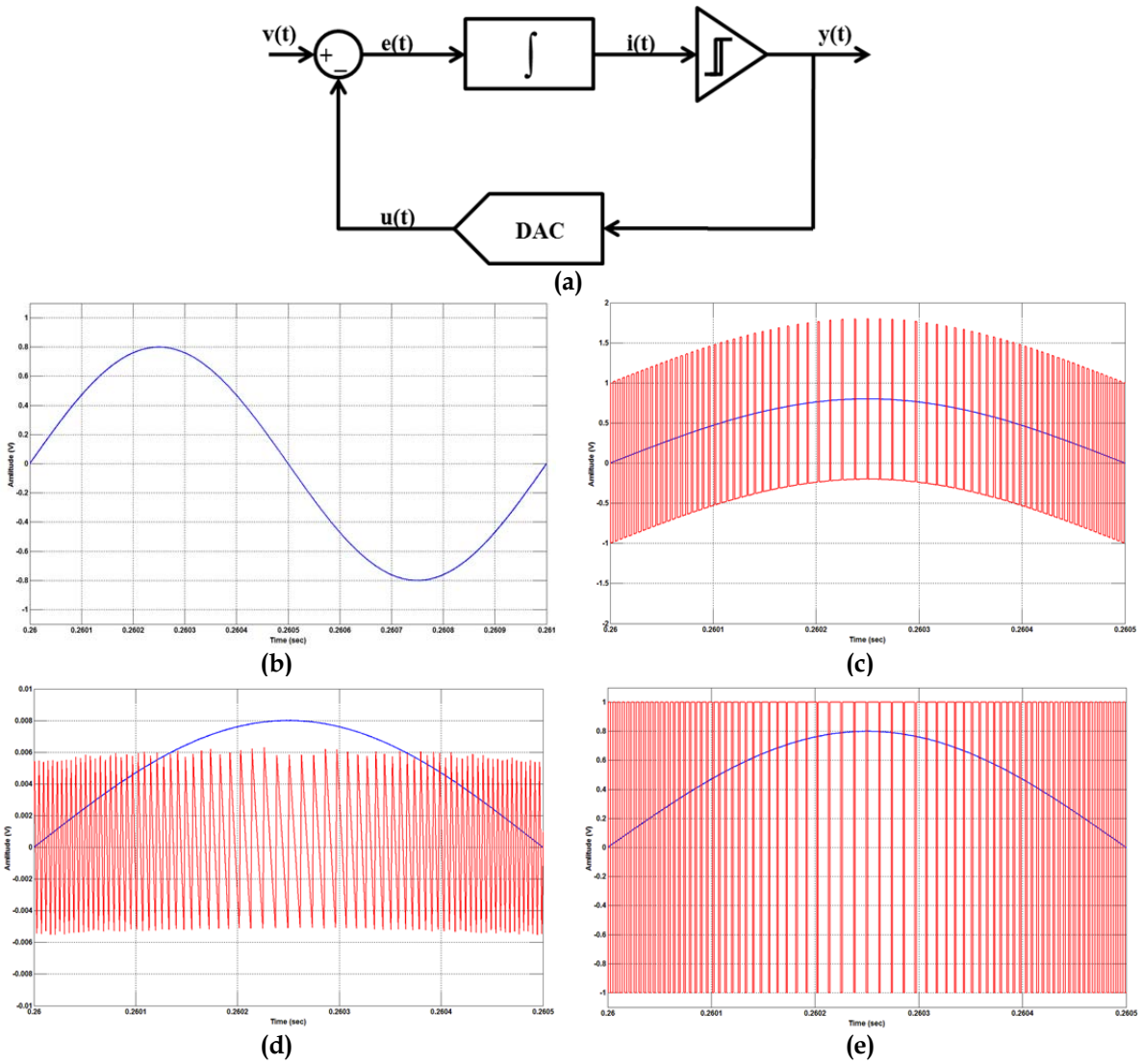


Figure 2-2: A asynchronous sigma-delta modulator
(a) architecture of ASDM, (b) input signal, (c) error signal, (d) integrator output (e) output signal

This chapter analyzes an asynchronous sigma-delta modulator loop and discusses its systematic errors which degrade its performance of an ideal DCM. These errors are placed in two categories: *fixed errors* and *dynamic errors*.

Fixed errors, originating from the implementation of the sigma-delta loop, are independent of the input signal and can be affected by the performance of

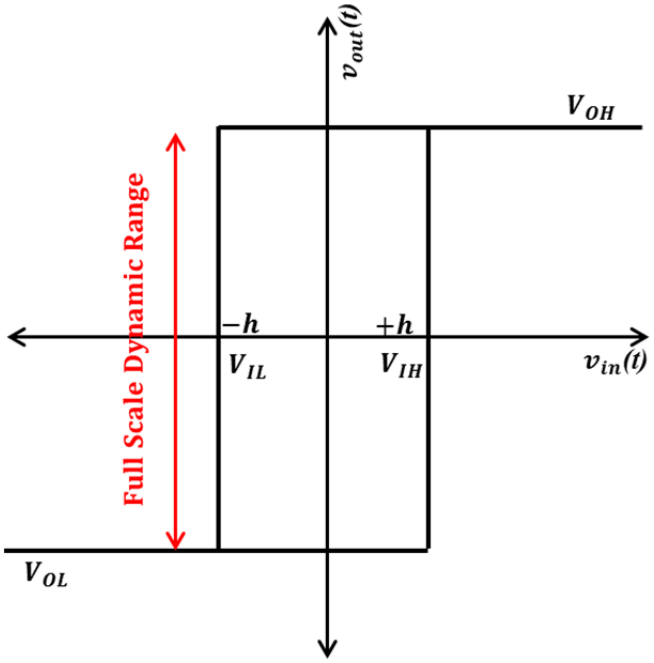


Figure 2-3: Hysteresis waveform of the comparator

components in the loop. Fixed errors, such as *excess loop delay*, *nonlinearities*, and *noise*, are discussed in current chapter.

Dynamic errors are error sources that depend on the amplitude or frequency of the input signal. These sources can be avoided through careful design or can be compensated by using digital back ground calibration. *Overload* and *integrator's saturation effect* are the errors that belong to this subset.

In this chapter, the sigma-delta modulator structure will be presented in depth followed by a comprehensive study of the various error sources and their effect on the performance of the modulator.

Parameter	Symbol	Value
Input frequency	f_{in}	$1KHz$
Bandwidth of interest	BW	$10KHz$
Input offset	V_{ofs}	$0V$
Dynamic range	DR	$2V$
Modulation depth	MD	80%
Maximum input amplitude	A_{max}	$1V$
Integrator coefficient	$1/k$	$\frac{1}{RC} = \frac{1}{(20pF \times 10M\Omega)} = 5KRad/s$
Sampling rate	F_s	$8\,MSample/s$
Number of FFT samples	N	$2^{24}\ Sample/s$
Hysteresis value	h	$5mV$
Comparator high input level	V_{IH}	$+5mV$
Comparator low input level	V_{IL}	$-5mV$
Comparator offset	V_{ref}	$0V$
Comparator high output level	V_{OH}	$+\frac{DR}{2} = +1V$
Comparator low output level	V_{OL}	$-\frac{DR}{2} = -1V$
Input noise power	σ_N^2	$-60dB$
Input signal	$v_{in}(t)$	$A_{max} \times MD \times \sin(2\pi f_{in} t) + Noise$

Table 2-1: Default simulation parameters assumed for ASDM throughout this chapter (unless otherwise stated)

In this thesis, such bi-level ASDMs are targeted for low power sensor application, such as biomedical sensor applications. Thus, the frequency is selected low enough to consider all complexities of low frequency design accompanied with this type of modulators and converters.

From this point onward, parameters of the ASDM circuit in all simulations and experiments are same as the ones reflected on Table 2-1, unless otherwise it will be clarified.

2.2. An Analytical Review

During this section, based on both *Fourier* analysis (frequency domain) provided in [3] and *non-harmonic* analysis (time domain) discussed in [6, 7], an intuitive review of the concept behind asynchronous sigma-delta modulators is provided.

To adopt an approach to map amplitude information of the input signal into timing information of the output square-wave signal, an ideal duty-cycle modulator is needed (see Figure 1-1). In duty-cycle modulators, both period, T, and pulse-width, α, of the output square-wave are modulated by the input signal amplitude. The modulation process for an input signal, $v(t)$, can be formulated by:

$$\frac{\alpha(t)}{T(t)} = \frac{v(t)+1}{2} \tag{2-1}$$

$$\frac{\omega_i(t)}{\omega_c} = 1 - v(t)^2 \tag{2-2}$$

where $\alpha(t)$ and $T(t)$ are instantaneous pulse-width and period, respectively. ω_c is a constant center frequency while there is no input signal, $v(t) = 0$, and is called *limit cycle frequency*.

To implement such scheme, a sigma-delta modulator can be used. Figure 2-4 shows a block diagram and output waveform of an ASDM. This block diagram consists of:

(1) linear filtering block, $L(\omega)$, which is usually an ideal integrator combined with a gain stage to control modulation parameters

(2) a nonlinear component, $N(A,\omega)$, which in general can be realized as any type of a nonlinear component that is dependent on input signal's *amplitude*,A

(3) a feedback loop, which subtracts output signal with a reasonable weight from input signal [8].

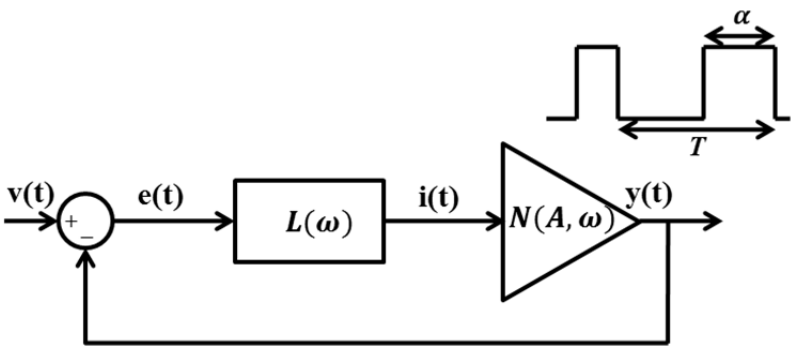


Figure 2-4: Block diagram of an ASDM and the output waveform

If the nonlinear component in this figure is replaced with a *hysteresis-type comparator,* then the time interval between consecutive transitions of the output signal show duty-cycle modulated information of the input signal. However, such a sigma-delta loop shows nonlinearities degrading its performance from an ideal duty-cycle modulator.

The *limit cycle oscillation* frequency of the ASDM can be extracted by applying the *Barkhausen criterion* over the loop:

$$1 + N(A,\omega).L(\omega) = 0 \qquad (2\text{-}3)$$

For a single-bit hysteresis quantizer this equation reduces to

$$\sum_{k=1,3,5}^{\infty} \frac{1}{k}\, Im[L(jk\omega_c)] = \pm \frac{\pi h}{4} \tag{2-4}$$

where ω_c is unforced limit cycle frequency (with zero input), and h is hysteresis value. If the system is symmetric and input is unforced, ω_c is considered the center frequency, since in this case output square wave oscillates with 50% duty-cycle [2]. On the other hand, the existence of hysteresis helps a loop with a first-order linear filter to provide the phase shift required to satisfy the *Barkhausen criterion*. For higher-order filters this hysteresis is not required for oscillation but it is still needed to alleviate noise effect on triggering comparator output.

In equation (2-4), if we put an ideal integrator in place of linear filter then:

$$L_1 = \frac{G}{j\omega} \rightarrow \omega_{c1} = G.\frac{\pi}{2h} \tag{2-5}$$

Here, G is a simple gain stage which helps to increase the limit-cycle oscillation frequency but degrades the loop stability. In fact, increasing G decreases the effective hysteresis, h, which in turn increases ω_c. If the filter is replaced with first-order or second-order analog filters, then center frequency in the case of the first-order filter is:

$$L_2 = \frac{\omega_p}{j\omega + \omega_p} \rightarrow \omega_{c2} = (\omega_p).\frac{\pi}{2h} \tag{2-6}$$

and in the case of the second-order filter:

$$L_3 = \frac{(\omega_{p1}\omega_{p2})}{\omega_z}.\frac{(j\omega + \omega_z)}{(j\omega + \omega_{p1})(j\omega + \omega_{p2})} \rightarrow \omega_{c3} = \frac{(\omega_{p1}\omega_{p2})}{\omega_z}.\frac{\pi}{2h} \tag{2-7}$$

The instantaneous limit cycle frequency, $\omega(t)$, in terms of the center limit cycle frequency is formulated as:

$$\frac{\omega(t)}{\omega_c} = 1 - v(t)^2 \tag{2-8}$$

where $v(t)$ is the instantaneous amplitude of the input signal normalized to 1. Based on equation (2-8), the output of the modulator is described by:

$$\frac{\alpha(t)}{T(t)} = \frac{v(t)+1}{2} \tag{2-9}$$

where $T(t) = \frac{2\pi}{\omega(t)}$ is the instantaneous period of the output square wave signal and $\alpha(t)$ is its pulse width. In [3], it is proved that the baseband and first-harmonic band of the output signal spectrum of a first-order ASDM for an input monotone signal $v(t) = v_m cos\mu t$ are:

$$y_0(t) = \frac{2\alpha}{T} - 1 \tag{2-10}$$

$$y_1(t) = \frac{2}{\pi}\sum_{n=-\infty}^{\infty}\sum_{m=-\infty}^{\infty} J_m(\beta_1) \times J_{2n}(\beta_2) \times cos\left(m\frac{\pi}{2}\right) cos(\omega_0 t + (2n+m)\mu t) \tag{2-11}$$

with

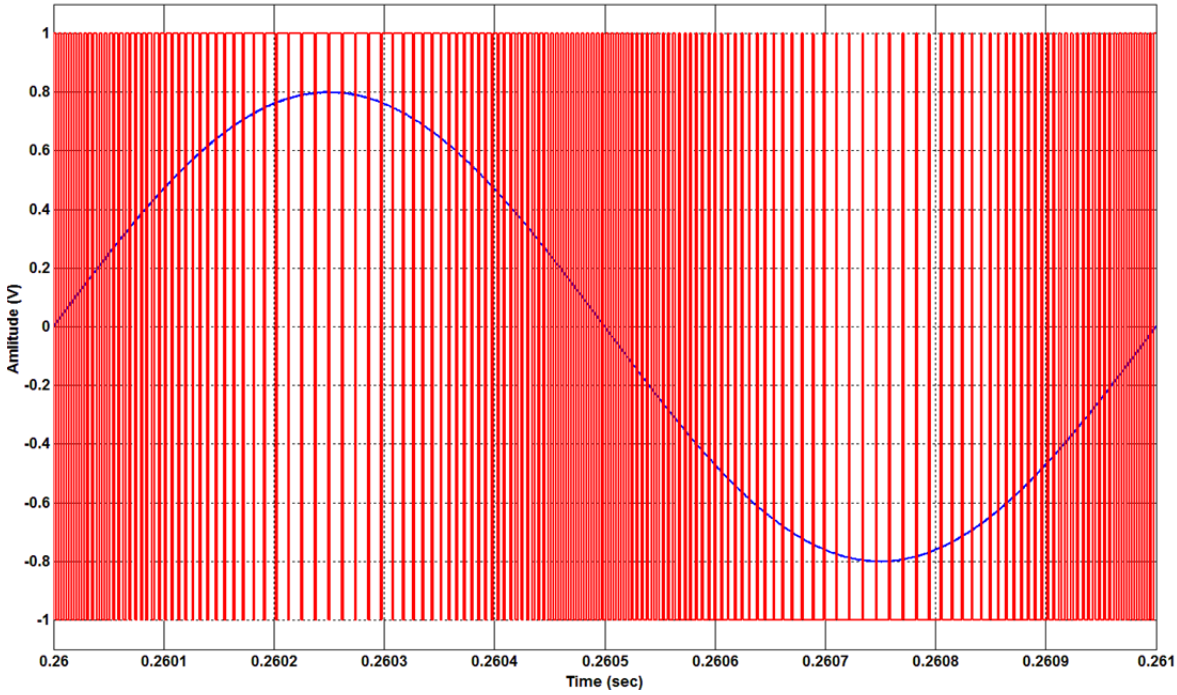
$$\beta_1 = v_m.\frac{\pi}{2}, \quad \beta_2 = v_m^2.\frac{w_c}{4\mu}, \ and\ \omega_0 = (1 - \frac{v_m^2}{2})\omega_c$$

Let's first define the term *modulation depth (MD)* as the ratio of amplitude of the input signal to the full scale or dynamic range of the feedback signal.

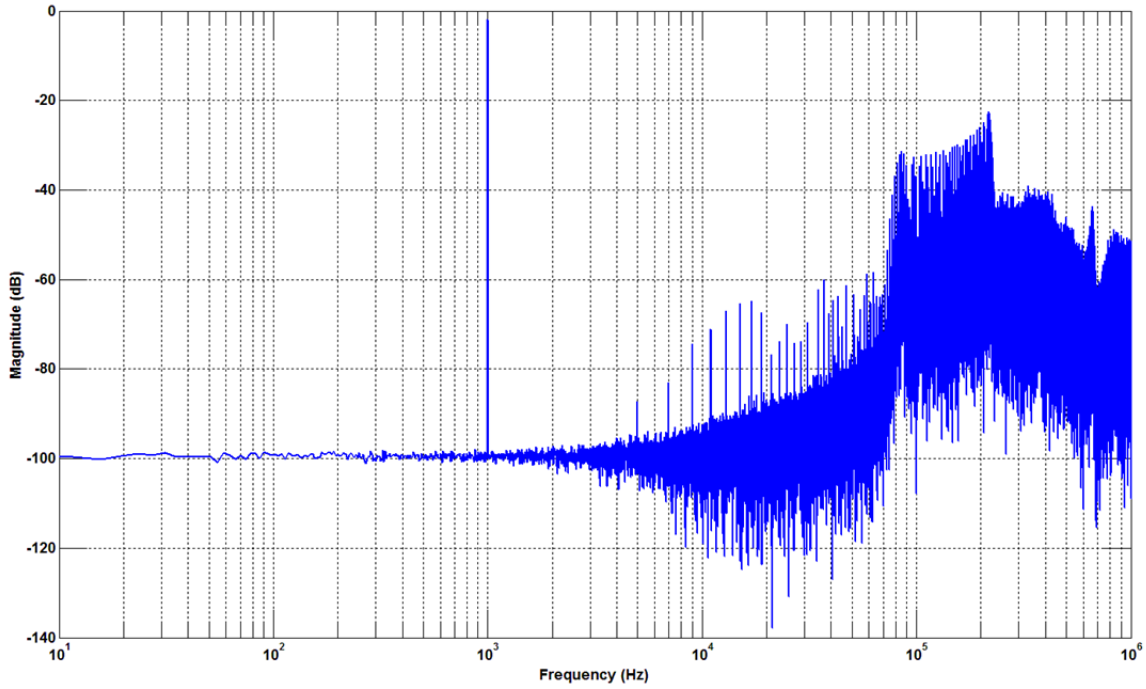
Equation (2-10) satisfies requirement for an ideal DCM but this is not a complete expression for the output signal. As described by equation (2-11), the frequency components (*Bessel components*) of the output signal depend on the input amplitude (v_m), the input frequency (μ), and the order of the filter. That is, y_1 shows that, in the presence of a single-tone signal, the output of the modulator is modulated and the *Bessel components* are spread around the limit cycle center frequency (which can be inferred as a carrier frequency). These Bessel sums are infinite; however terms of (2-11) close to the limit cycle frequency are distinguishable from the noise floor for low modulation depths [8].

Equation (2-11) is used to provide an estimate of the limit cycle oscillation. The limit cycle oscillation should be considered large enough to prevent Bessel harmonics penetrating into the required band of interest. Same as *over-sampling ratio (OSR)* in continuous-time sigma-delta ADCs, we define *over-cycling ratio (OCR)* which is the ratio of *limit cycle oscillation* frequency, ω_c, to the bandwidth of interest , ω_B. A higher OCR yields a wider bandwidth free of Bessel components which, in turn, yields a higher SNDR.

Figure 2-5(a) shows the output of an ASDM when a single-tone sine-wave is given as an input. This picture demonstrates how the time interval between any consecutive edges of the output square-wave is modulated by the amplitude of the input sine-



(a)



(b)

Figure 2-5: Output of an ASDM in response to a 1KHz input signal at 80%MD (a) transient response, (b) frequency response (rectangular window)

wave. Figure 2-5(b) shows the spectrum of the output signal. As is evident in this picture, the ASDMs noise floor is shaped out of the band of interest; however, unlike

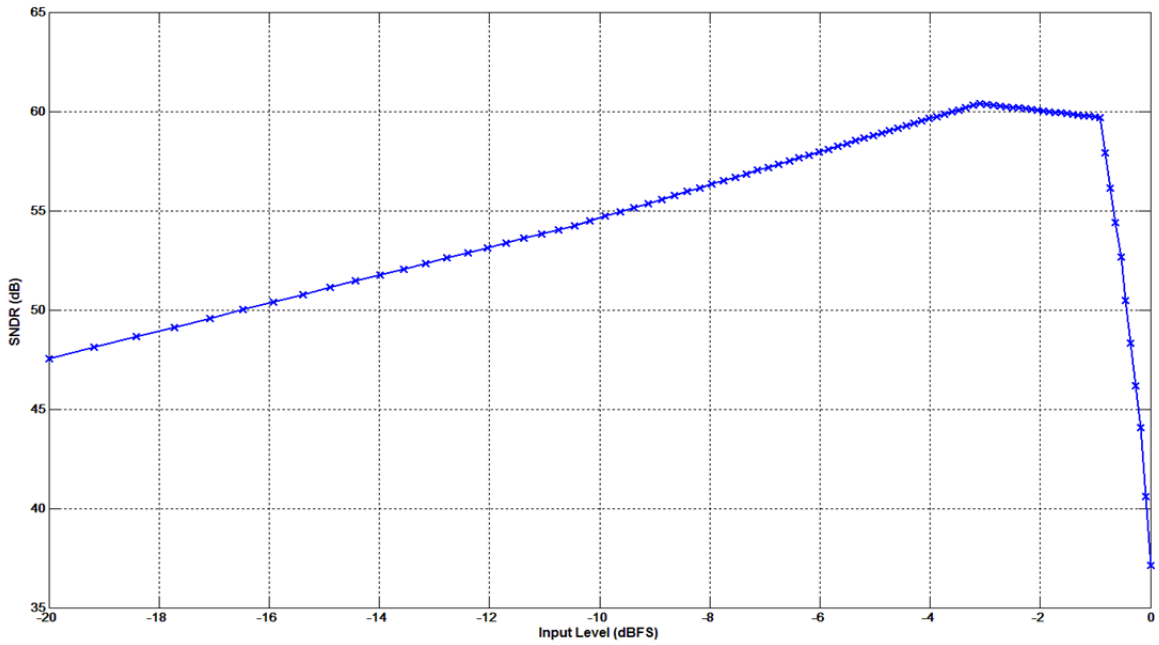


Figure 2-6: SNDR variations vs. input modulation depth

continuous-time sigma-delta modulators, no quantization occurs in the loop and thus no quantization noise shows up. The noise floor that is shaped out of the band is just the *thermal noise* and *flicker noise* of the components inside loop. It should be noted that, in order to perform a precise FFT, in some cases in this report, *Hanning windows* are used which help minimize spectral leakage and scallop loss [9]. In each case the type of window is notified.

Figure 2-6 shows how the SNDR degrades with increasing modulation depth. As is illustrated in the graph, as modulation depth approaches 90% of the full scale amplitude, the SNDR drops dramatically. Since *Bessel components* come out of the root noise this degradation happens and increases the instability and nonlinearity of the system.

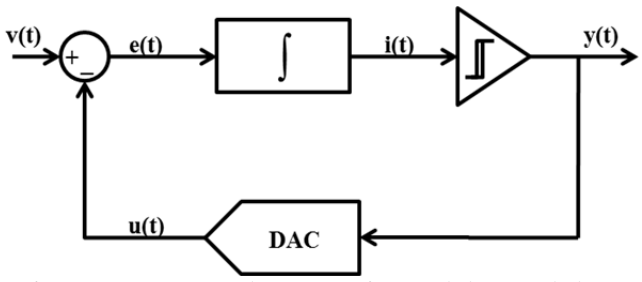


Figure 2-7: A asynchronous sigma-delta modulator

Based on calculations provided in [3], an ASDM approximately implements an ideal duty-cycle modulator, provided that the input signal is slow enough such that its variations are monotonic within one period of the instantaneous carrier frequency, $\omega_i = \omega(t)$.

In Figure 2-7, the error signal, $e(t)$, generated by subtracting the output signal from the input signal, is filtered out by a linear filter $F(\omega)$. The low pass filter output then triggers the comparator and the output signal, $sgn[e(t)]$, is fed back to be subtracted from input signal. Thus if a DC signal, V, is fed to the input of the circuit then the $sgn[e(t)]$ is the filtered representation of the error signal, $e(t)$.

Writing the time domain equation around the loop gives us:

$$\left[V - sgn[e(t)]\right] \otimes f(t) = e(t) \qquad (2\text{-}12)$$

where $f(t)$ is the pulse response of the low-pass filter $F(\omega)$ and $\otimes$ denotes convolution operator [3]. The Fourier series expansion of the output periodic square wave with a fixed pulse width of α_0 and a fixed period of $T_0 = \frac{2\pi}{\omega_0}$ results in [3]:

$$sgn[e(t)] = \left(2\frac{\alpha_0}{T_0} - 1\right) + 4Re\sum_{n=1}^{\infty}\frac{sin(n\pi\frac{\alpha_0}{T_0})}{n\pi}e^{jn\omega_0 t} \tag{2-13}$$

Time moments of zero crossings of the square wave coincide with the moments that the error signal, $e(t)$, crosses the hysteresis values $\pm h$:

$$\begin{aligned} e(t) &= h \;@\; t = -\frac{\alpha_0}{2} + kT_0 \\ e(t) &= -h \;@\; t = \frac{\alpha_0}{2} + kT_0 \end{aligned} \tag{2-14}$$

where k is an integer.

To satisfy oscillation criteria for a dynamic input signal $v(t) = v_m cos\mu t$, it can be supposed that the stationary output square wave in (2-13) is modulated with the input signal amplitude. This is a valid assumption since the output square wave in DC signal is expanded in Fourier series. Then all sinusoidal components in the expansion equation can be modulated by the input signal individually. Thus, referred to more detailed calculations in [3] we have:

$$v - \left(2\frac{\alpha}{T} - 1\right) = \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{ReF(n\omega_i)}{nF(\mu)}\sin(2\pi n\frac{\alpha}{T}) \tag{2-15}$$

$$\sum_{n=1}^{\infty}\frac{1}{n}ImF(n\omega_i)sin^2(\pi n\frac{\alpha}{T}) = -\frac{\pi}{4}h \tag{2-16}$$

where $F(\omega)$ is the transfer function of the low-pass filter based on equations (2-6) or (2-7). This loop performs as an ideal duty-cycle modulator as in the equation (2-1) as long as,

$$\sum_{n=1}^{\infty} \frac{ReF(n\omega_i)}{nF(\mu)} \sin(2\pi n \frac{\alpha}{T}) \ll \frac{\pi}{2} \tag{2-17}$$

Then equation (2-15) turns to:

$$\frac{\alpha}{T} = \frac{v+1}{2} \tag{2-18}$$

Moreover, to satisfy equation (2-2), based on equation (2-16), the higher the out-band suppression, $F(n.\omega(t))$, over the pass-band, $F(\mu)$, the better the approximation. Also, it is shown that if (2-17) is not satisfied then the most significant distortion term is the third harmonic with the distortion ratio of:

$$\Delta_3 = \frac{\pi^2}{6} \frac{ReF(\omega_o)}{F(\mu)} v_m^2 \tag{2-19}$$

If the loop filter is considered as (2-7), then

$$\Delta_3 = \frac{\pi^2}{6} \frac{\mu^2}{\omega_o^2} v_m^2 \tag{2-20}$$

Thus, to design a quasi-ideal duty-cycle modulator it is critical to keep $\omega_c$far enough from base band. To do so, we need a filter with acceptable suppression ratio over the stop-band and reasonable DC gain. Also, a proper hysteresis value for the comparator is required.

2.3.Circuit Implementation

In order to implement an *asynchronous sigma-delta modulator* circuit, a behavioral model was first built in *Simulink®/MATLAB®*. Depicted in Figure 2-8, this model consists of an ideal integrator in place of a linear low-pass filter. A gain stage, k, used in front of the integrator decreases the effective hysteresis value which is now given by $\frac{h}{k}$. This effective decrease helps increase the limit cycle frequency, ω_c, when hysteresis parameter, h, is fixed.

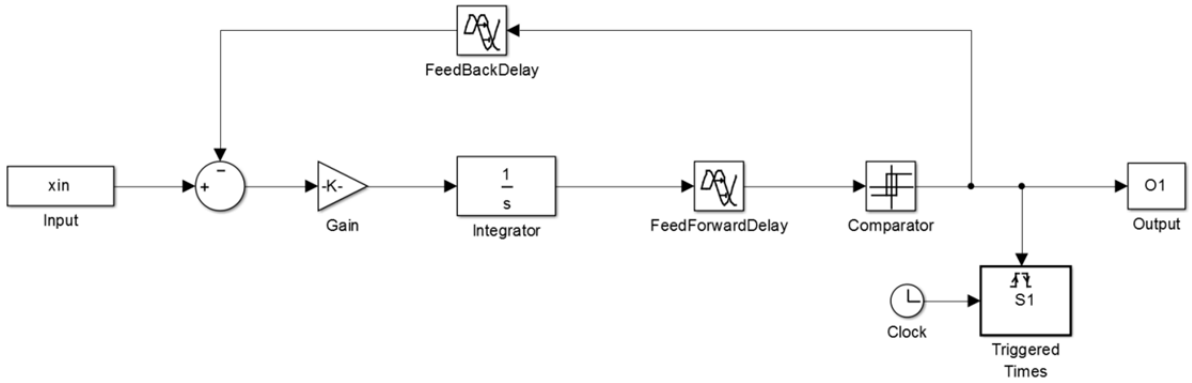
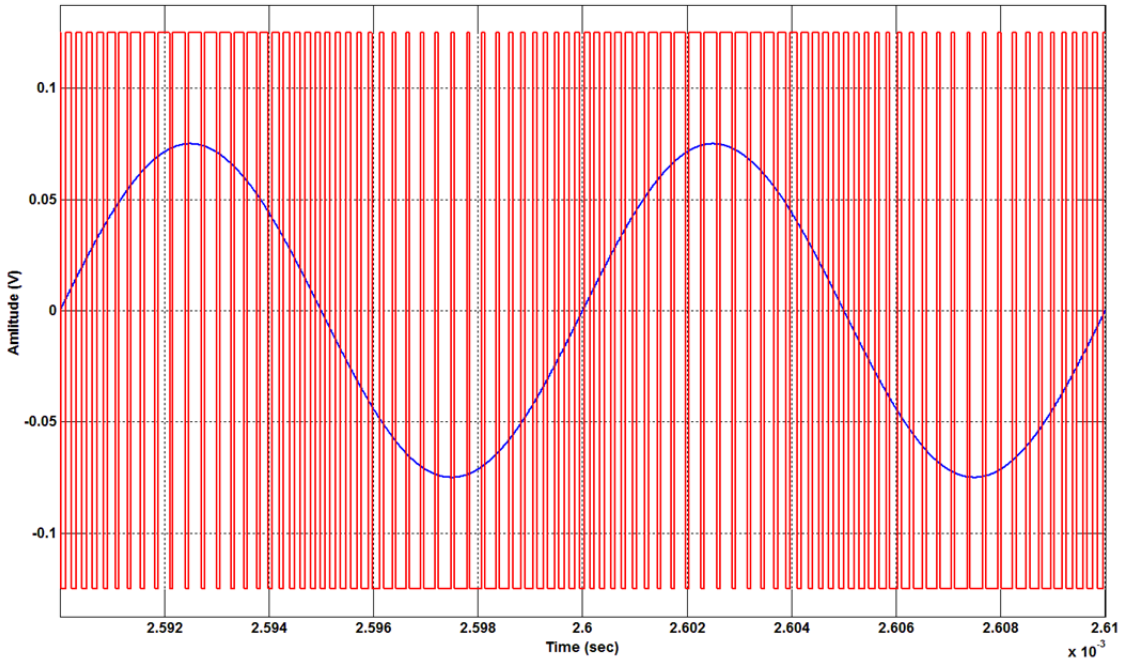


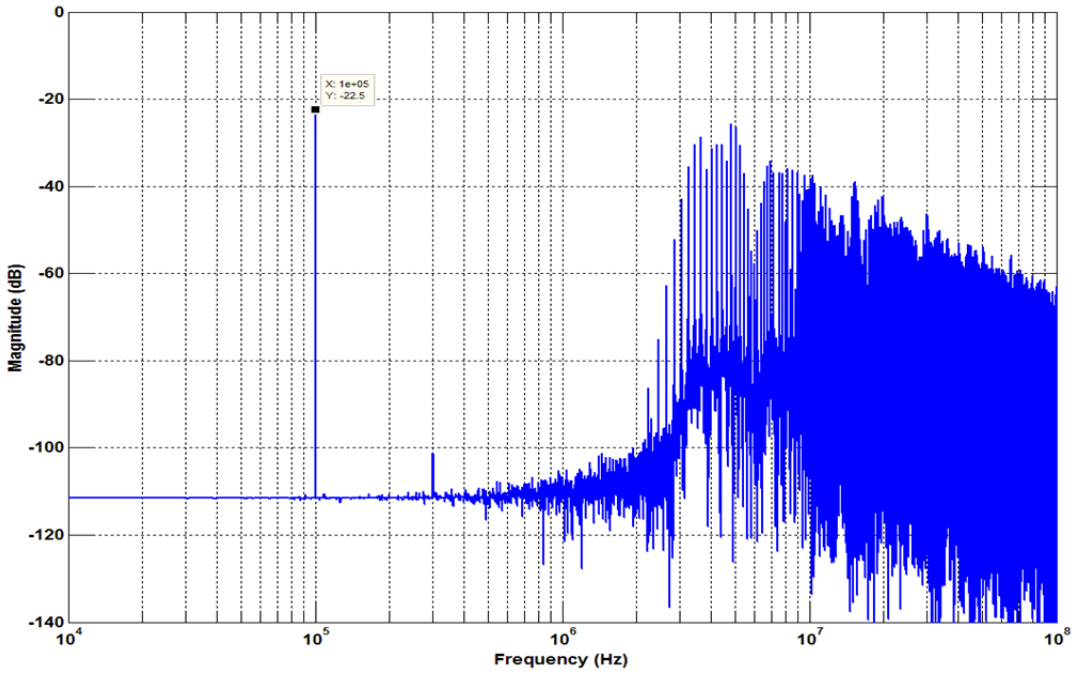
Figure 2-8: Behavioral model of an ASDM

A hysteresis comparator is used as the nonlinear component in the loop. Figure 2-9(a) shows the transient response of the circuit for a $100KHz$ (this frequency is selected in order to comply with the circuit level simulation test criteria) input signal with a 50% modulation depth while Figure 2-9(b) shows the output spectrum.

To realize such a configuration at the transistor level, a non-ideal integrator in place of the linear filter is used. As presented in Figure 2-10, this is an OTA based single pole RC integrator. The structure of the integrator facilitates subtraction of the output



(a)



(b)

Figure 2-9: Output of an ASDM (behavioral model) in response to a 100KHz input signal at 50%MD (a) transient response, (b) frequency response (rectangular window)

signal from input signal by passing each through a resistor and then subtracting the resulted currents.

Parameter	Symbol	Value
Input frequency	f_{in}	$100KHz$
Bandwidth of interest	BW	$5MHz$
Input offset	V_{ofs}	$150mV$
Dynamic range	DR	$300mV$
Modulation depth	MD	50%
Maximum input amplitude	A_{max}	$150mV$
Integrator coefficient	$1/k$	$\frac{1}{RC} = \frac{1}{(10pF \times 10M\Omega)} = 10KRad/s$
Sampling rate	F_s	$400\ MSample/s$
Number of FFT samples	N	$2^{24}\ Sample/s$
Hysteresis value	h	$30uV$
Comparator high input level	V_{IH}	$150.03mV$
Comparator low input level	V_{IL}	$149.97mV$
Comparator offset	V_{ref}	$150mV$
Comparator high output level	V_{OH}	$300mV$
Comparator low output level	V_{OL}	$0V$
Input noise power	σ_N^2	$-50dB$
Input signal	$v_{in}(t)$	$A_{max} \times MD \times \sin(2\pi f_{in} t) + Noise$

Table 2-2: Simulation parameters for the gate-level ASDM

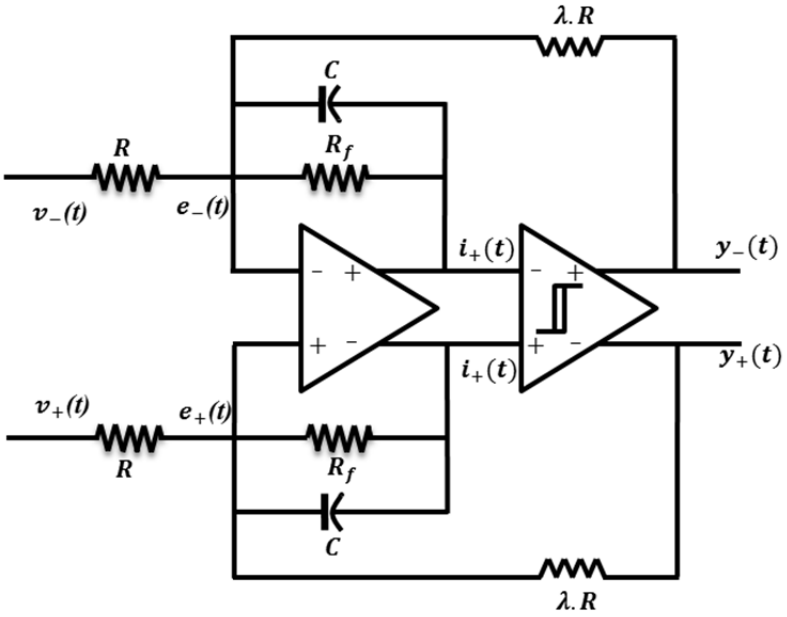
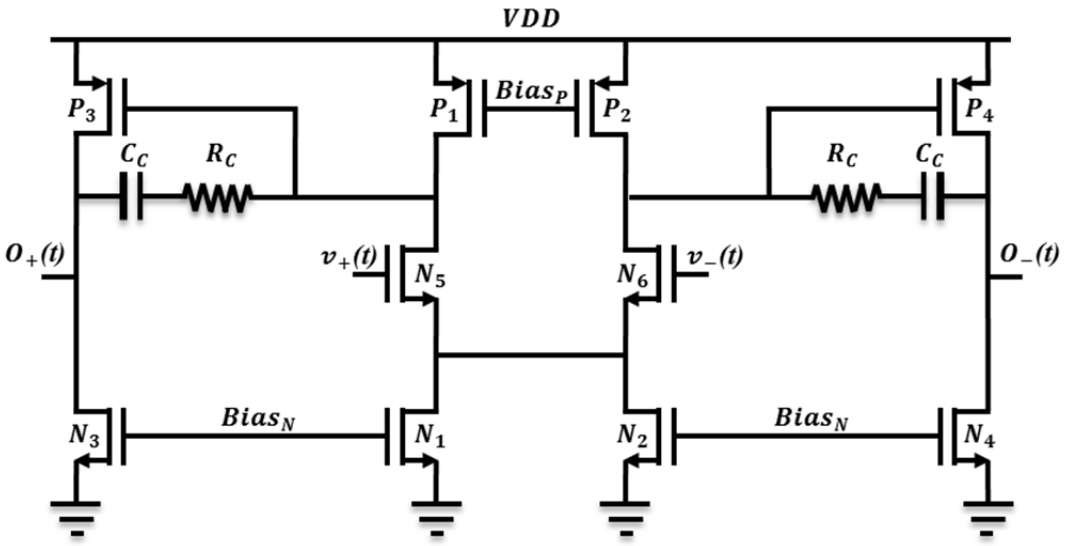
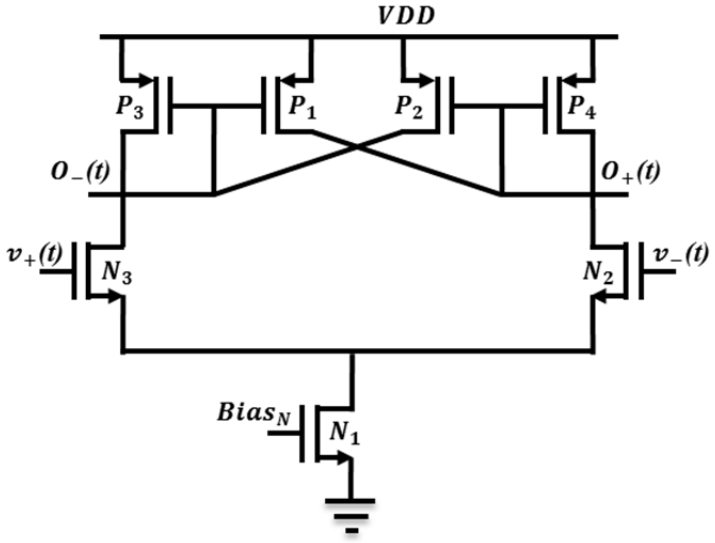


Figure 2-10: Schematic of the Implemented ASDM



(a)



(b)

Figure 2-11: Circuit diagram of (a) differential OTA (CMFB is not shown), (b) hysteresis-type comparator

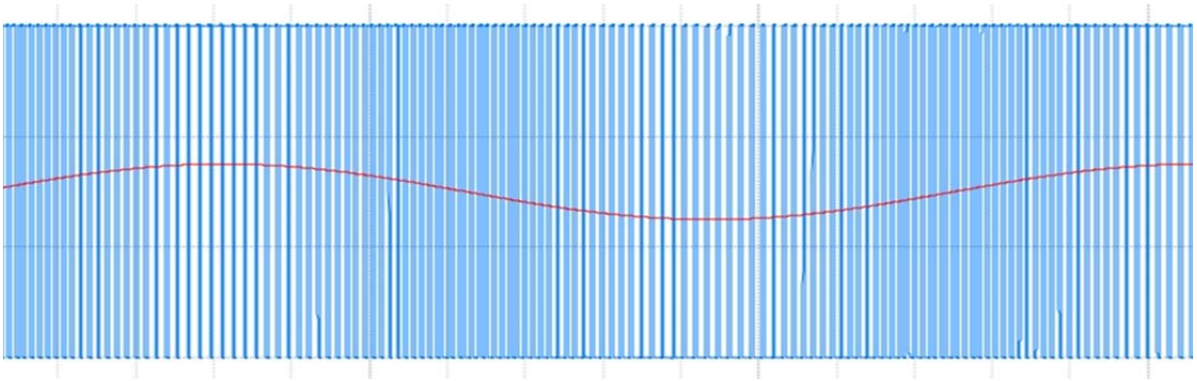
Typically $G_m - C$ filters are used to realize ideal integrators. The main issue with such filters is their nonlinearity arising from the nonlinear $G_m$stages. Also, the nonlinear nature of semiconductor capacitors introduces harmonics into the band of interest degrading the linearity of whole circuit. These nonlinearity issues can be minimized using a fully differential structure.

Figure 2-11(a) shows transistor level view of the OTA used in this circuit. The common mode feedback circuit is not shown in this picture.

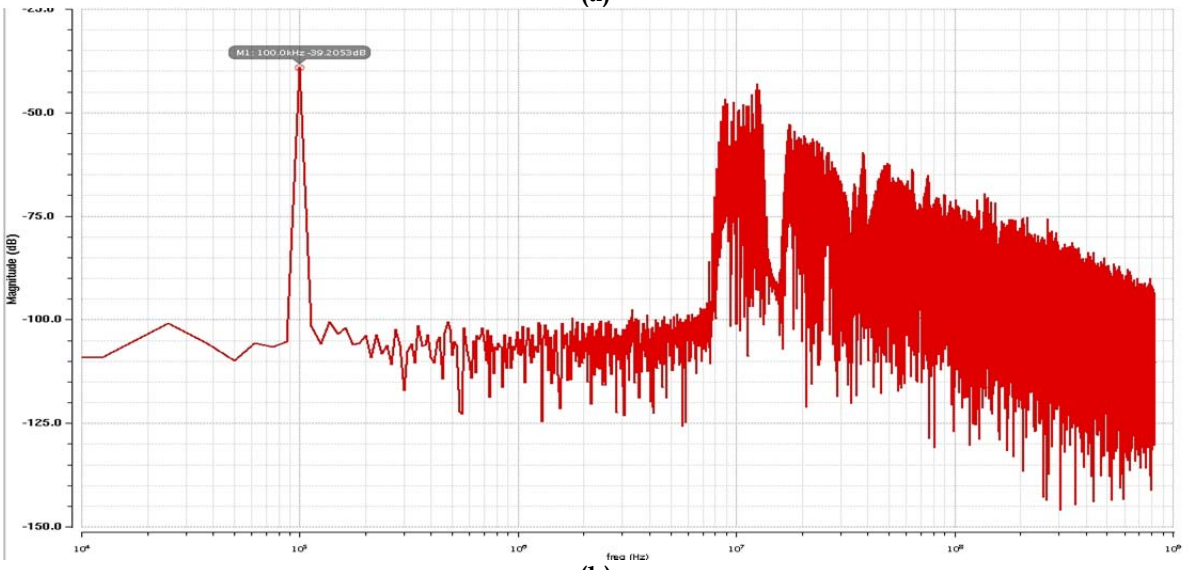
Based on the structure provided for hysteresis comparators in [10], the schematic of the nonlinear component is presented in Figure 2-11(b). The fixed hysteresis value,h, is given by the following equation:

$$h = 2\sqrt{\frac{I_{bias}}{\mu C_{ox}\left(W/L\right)_q}}.\frac{\sqrt{\delta}-1}{\sqrt{\delta+1}} \tag{2-21}$$

where the feedback coefficient $\delta = \left(W/L\right)_{cc}/\left(W/L\right)_{dc}$ is the ratio between the cross-coupled and diode-connected transistors, I_{bias} is the tail biasing current and $\left(W/L\right)_q$ is the aspect ratio of the input pair. For $\delta > 1$, the load acts as negative resistance and hysteresis is introduced.



(a)



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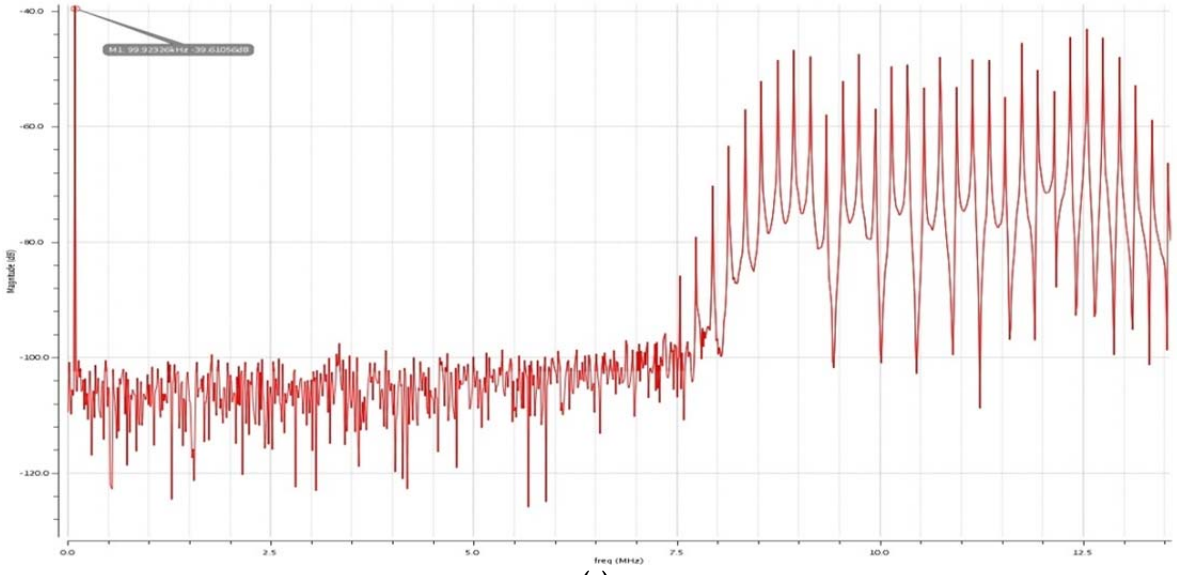


(c)

Figure 2-12: Output signal of the ASDM circuit in response to a 100 KHz input sine wave at 50% MD (a) transient response (b) spectrum in log mode (c) spectrum in linear mode (Hanning window). 89dBFS SNR and 96dBFS SFDR is achieved over a 5MHz baseband

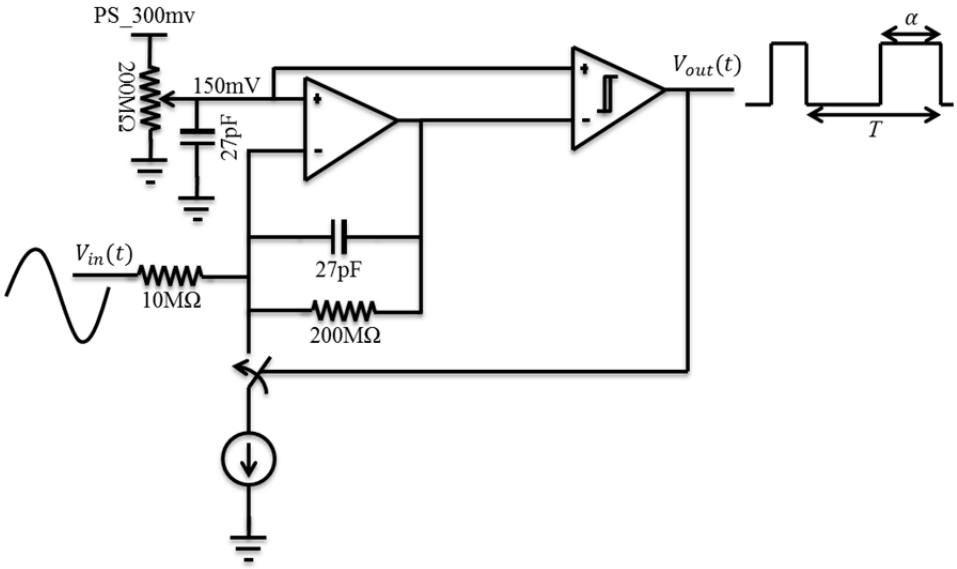


Figure 2-13: The ASDM made out of on-chip components

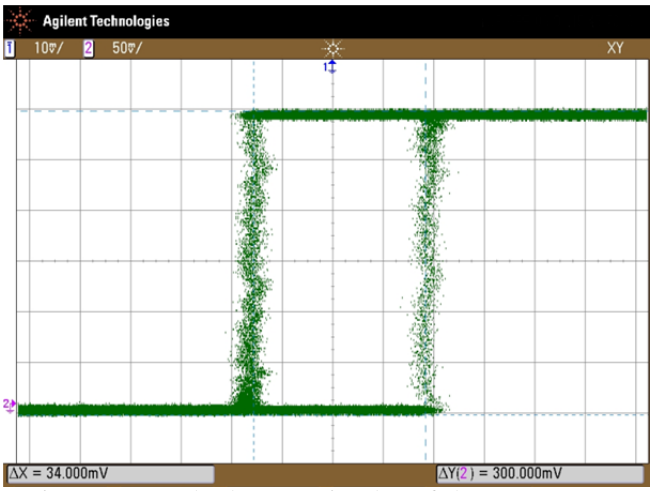


Figure 2-14: The hysteresis plot of the comparator

Figure 2-12(a) represents transient response of a $100KHz$ input signal with modulation depth of 50%. Figure 2-12(b, c) show the output spectrum of the same signal.

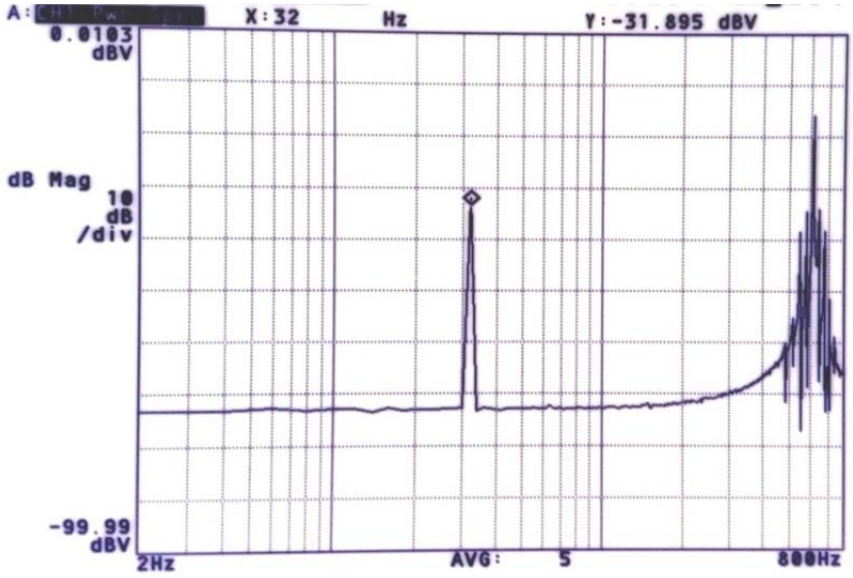
To implement a semiconductor level ASDM, we used an already fabricated chip containing a number of individual components such as *current sources (CS)*, *operational trans-conductance amplifiers (OTA)*, and *Schmitt-trigger comparators (STC)*. The

Parameter	Symbol	Value
Input frequency	f_{in}	32
Bandwidth of interest	BW	400
Input offset	V_{ofs}	$150mV$
Dynamic range	DR	$300mV$
Modulation depth	MD	17% & 34%
Maximum input amplitude	A_{max}	$150mV$
Integrator coefficient	$1/k$	$\frac{1}{RC} = \frac{1}{(340pF \times 10M\Omega)} = 300Rad/s$
Sampling rate	F_s	$2\,MSample/s$
Number of FFT samples	N	$2^{24}\ Sample/s$
Hysteresis value	h	$17mV$
Comparator high input level	V_{IH}	$167mV$
Comparator low input level	V_{IL}	$133mV$
Comparator offset	V_{ref}	$150mV$
Comparator high output level	V_{OH}	$300mV$
Comparator low output level	V_{OL}	$0V$
Input noise power	σ_N^2	$-50dB$
Input signal	$v_{in}(t)$	$A_{max} \times MD \times \sin(2\pi f_{in} t) + Noise$

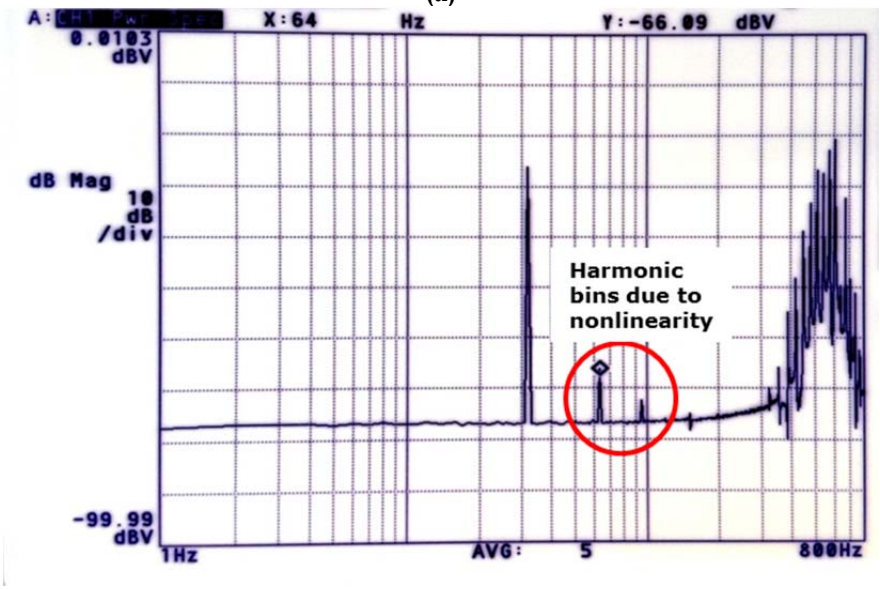
Table 2-3: Circuit and simulation parameters for the fabricated ASDM

architecture of the ASDM made out of the on-chip components is depicted in Figure 2-13. The hysteresis plot of the comparator used in this circuit is depicted in Figure 2-14.

As illustrated in Figure 2-13, constructing components of this ASDM are all single-ended. Thus, a high level of input-dependent harmonic distortion is expected. Figure 2-15 shows the output spectrum of this ASDM for a 32Hz sine-wave with two different values of modulation depth. As is evident from the picture, increasing the modulation depth of the input signal leads to an increase in magnitude of the input-dependent harmonics and makes them bump out of root noise level. As mentioned



(a)



(b)

Figure 2-15: Output spectrum (Hanning window) of the fabricated ASDM circuit in response to (a) a 32Hz-50mVpp input sine wave at 17% MD; (b) a 32Hz-100mVpp input sine wave at 34% MD;

before, these input-dependent harmonics are result of the nonlinearities in the basic components of the circuit.

Finally it is important to note that the test conditions were set for low frequency signals. Thus, calculating FFT of the output signal was time-consuming. The results

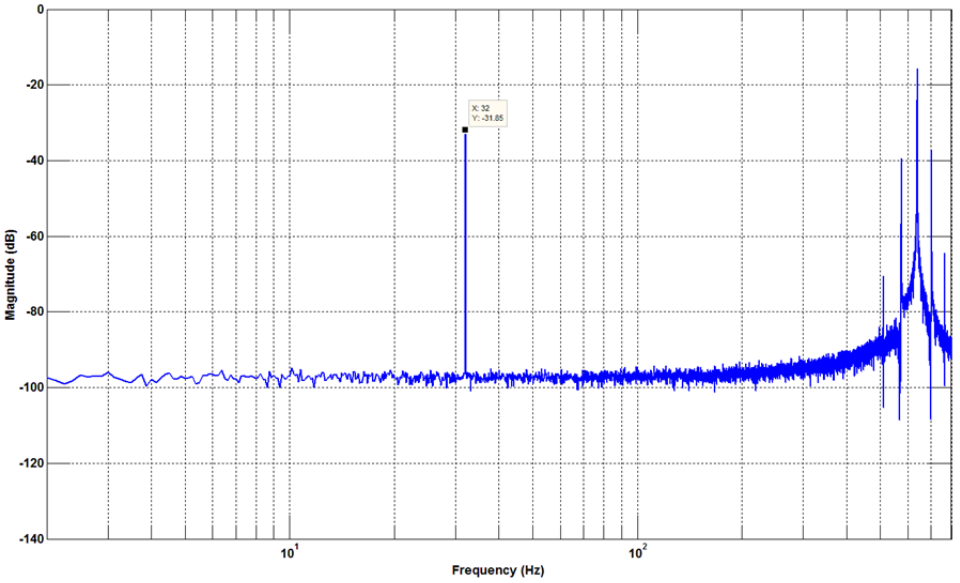
Noise Source	SFDR (dB)	SNDR (dB)	SNR (dB)	Figure #
	@400Hz BW	@400Hz BW	@400Hz BW	
Fabricated circuit 32Hz-50mVpp 17% MD	41.3	23.8	24.4	Figure 2-15(a)
Fabricated circuit 32Hz-100mVpp 34% MD	41.6	17.0	32.1	Figure 2-15(b)
Simulated circuit 32Hz-50mVpp 17% MD	55.4	26.1	27.9	Figure 2-16(a)
Simulated circuit 32Hz-100mVpp 34% MD	59.1	34.4	36.7	Figure 2-16(b)

Table 2-4: Simulations results compared with lab experiments results for an ASDM

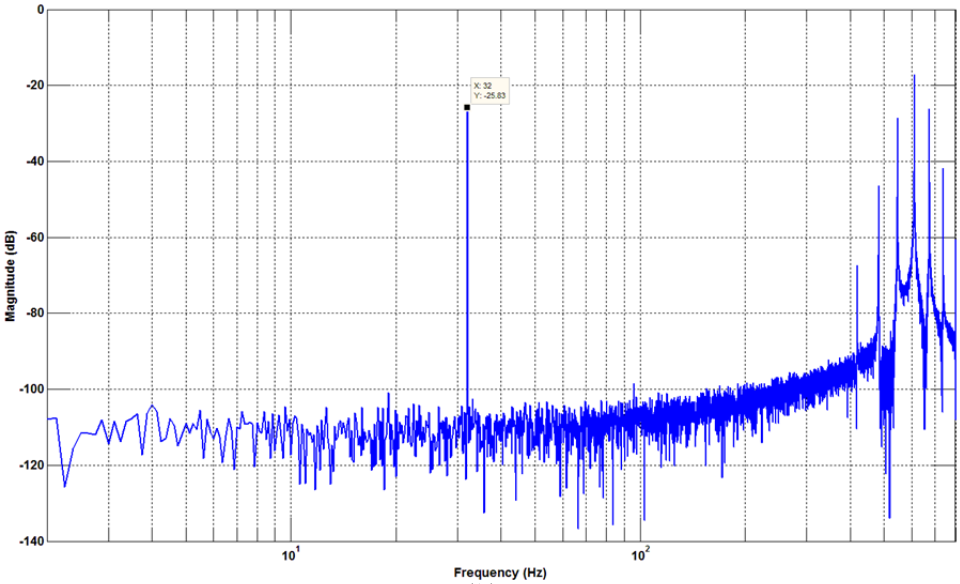
shown in Figure 2-15 are obtained with a spectrum analyzer to validate the previous analysis.

A comparison between simulation results and lab experiments are tabulated in Table 2-5. With a small difference due to the more precise digital calculations in Matlab® than spectrum analyzers the achieved results are the same. Figure 2-16 has demonstrated the spectrum of simulated ASDM circuit in Matlab® same as Figure 2-15.

Hereafter, all data is obtained from scopes with high-rate regular sampling and analyzed using MATLAB®. It should also be noted that the sampling period must be smaller than minimum time interval between any two consecutive triggering edges of the output signal. At least half of this minimum time interval must be considered as sampling period to prevent aliasing of high frequency components.



(a)



(b)

Figure 2-16: Output spectrum (Hanning window) of the simulated ASDM in response to (a) a 32Hz-50mVpp input sine wave at 17% MD; (b) a 32Hz-100mVpp input sine wave at 34% MD;

2.4.Fixed Errors in Asynchronous Sigma-Delta Modulators

As defined earlier, *fixed errors* are classified as fixed sources of error originating from the nature of the sigma-delta loop. They are independent of the input signal and are affected by the performance of individual components in the loop. *Excess loop delay*, *nonlinearity*, and *noise* are types of fixed errors discussed further in this chapter.

2.4.1. Excess Loop Delay

In continuous-time sigma delta modulators, excess loop delay is defined as "nonzero delay between the quantizer clock edge and the time when a change in output bit is seen at the feedback point in the modulator" [11]. The excess loop delay is a direct effect of propagation delay of the comparator in the CT-SDM loops.

This delay can be modeled as a linear delay, τ_d, of the comparator latency and a first order linear system with a time constant, τ_c, because of the propagation delay of the comparator. The linear system model for excess loop delay can be expressed as [12]:

$$H_{ELD}(s) = \frac{e^{-\tau_d s}}{1 + \tau_c s} \tag{2-22}$$

The linear delay, linearly shifts the events in time, while the first order pole added from parasitic components at the output node increases the order of the *open loop* transfer function of the whole system. This added order, results in increasing the order of the *noise transfer function (NTF)* of the loop which causes instability and degrades the *Signal to Noise Ratio (SNR)* of the modulator.

Performance	SFDR (dB)	SNDR (dB)	SNR (dB)	ω_c (KHz)	Figure #
	@10KHz BW	@10KHz BW	@10KHz BW		
$\tau_d = 60ns$; $\tau_r = 300ns$ (Low)	70.6	65.1	66.7	165	Figure 2-17(a)
$\tau_d = 610ns$; $\tau_r = 3.0\mu s$ (Medium)	50.8	51.1	53.3	47	Figure 2-17(b)
$\tau_d = 6.1\mu s$; $\tau_r = 30.0\mu s$ (High)	0.3	0.1	0.1	4.3	Figure 2-17(c)

Table 2-5: Performance of an ASDM in the presence of excess loop delay modeled with a linear system as equation (2-22)

In ASDMs this error also exists and like in CT-SDM it consists of linear delay and propagation delay. However, in ASDMs this delay can be interpreted as the delay between the time that integrator's output passes $\pm h$ and the time the current switch of the feedback DAC is activated.

In CT-SDMs, as modeled in (2-22), the added pole decreases stability of the loop. This error is accumulated in the integrator through the feedback loop and degrades SNR. However, in an ASDM, since there is no clock to be synchronized with, decisions are made continuously and instantly. That is, if the delay is not too high, the feedback loop has enough time (not restricted to half a clock cycle) to compensate the error and avoid saturating the integrator.

Figure 2-17 shows the output spectrum of an asynchronous sigma-delta modulator in the presence of -60dB input noise. Same as parameters mentioned in Table 2-1, the modulation depth is selected as 80% to achieve the best SNR and SNDR out of circuit. In this case, the loop is experiencing three different delay values. The results are tabulated in Table 2-5. The related output spectrums are plotted in Figure 2-17.

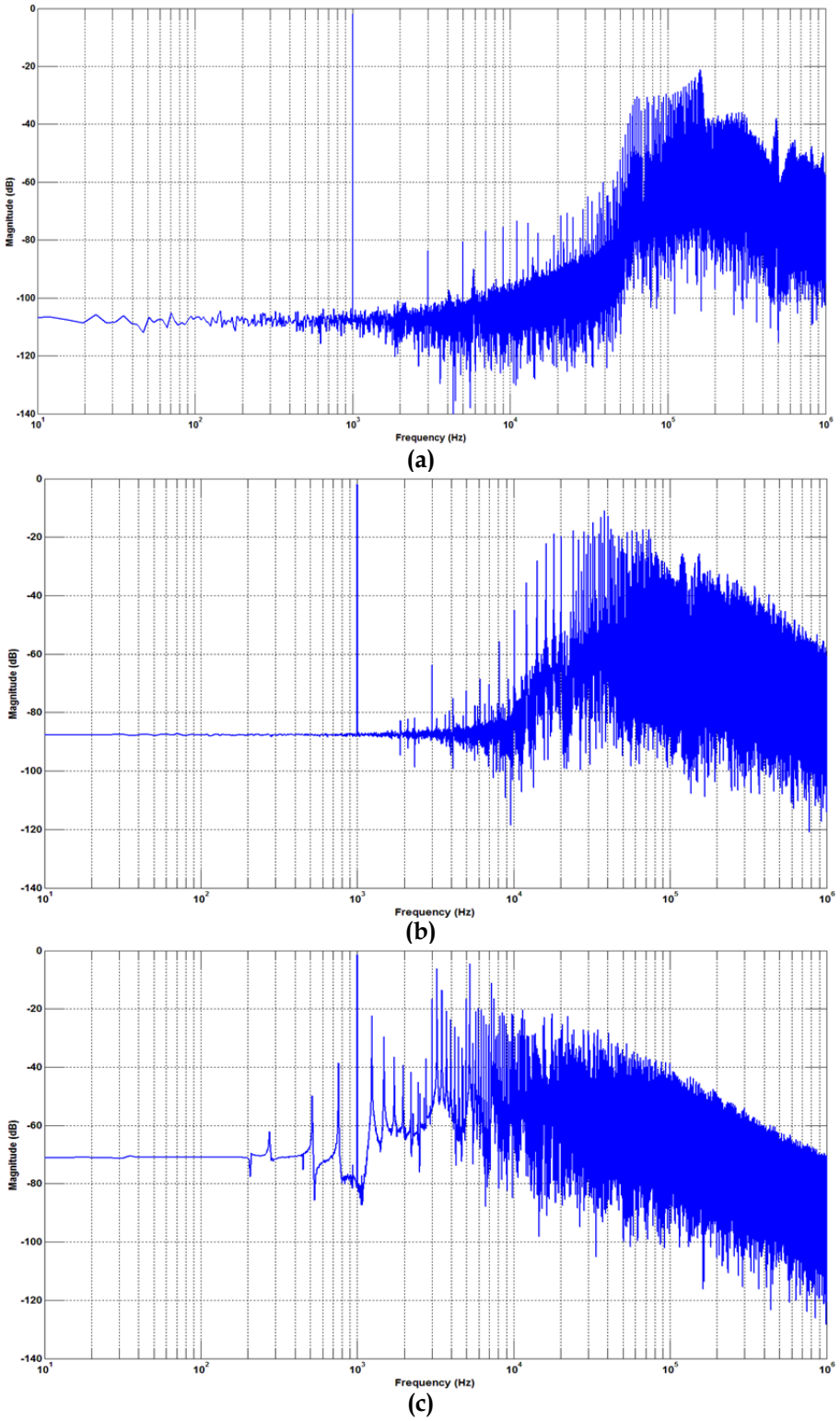


Figure 2-17: Output spectrum of an ASDM with (a) low, (b) medium, (c) high excess loop delay appeared in the loop (refer to Table 2-5)

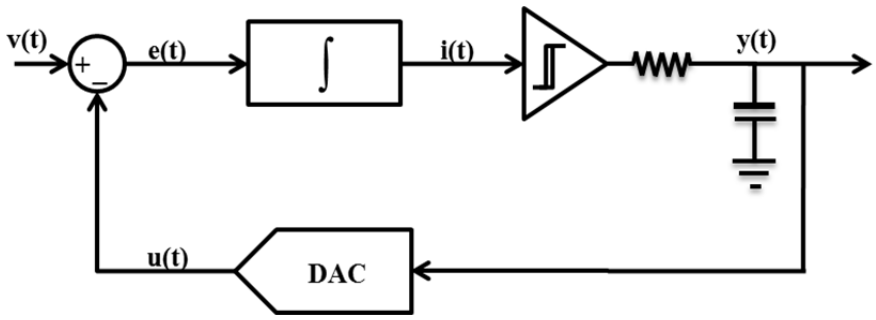


Figure 2-18: The model developed for simulating excess loop delay

Results prove that this delay severely affects the performance of the circuit. Increase in this delay has an effect same as increase in the hysteresis value; i.e., the center carrier frequency drops and more harmonics appear from the noise floor degrading the circuit performance.

The model implemented to simulate the excess loop delay is depicted in Figure 2-18. Based on equation (2-22) this delay is implemented by a linear shift delay and a single pole linear system.

Another way to model the propagation delay of a comparator is to treat it as an input dependent delay; as the input level of the comparator (output level of the integrator in sigma-delta loop) passes the reference voltage the delay exponentially increases. The formula derived for this delay is [13]:

$$t_p = \tau_r \ln\left[\frac{1}{1-\left|\frac{v_{in(min)}}{v_{in}}\right|}\right] \qquad (2\text{-}23)$$

where h is the hysteresis, $v_{in(min)} = \frac{V_{OH}-V_{OL}}{2A_V}$ is the minimum voltage required to start transition. τ_r is the rise-time constant (fall-time constant) in equation (2-22). This

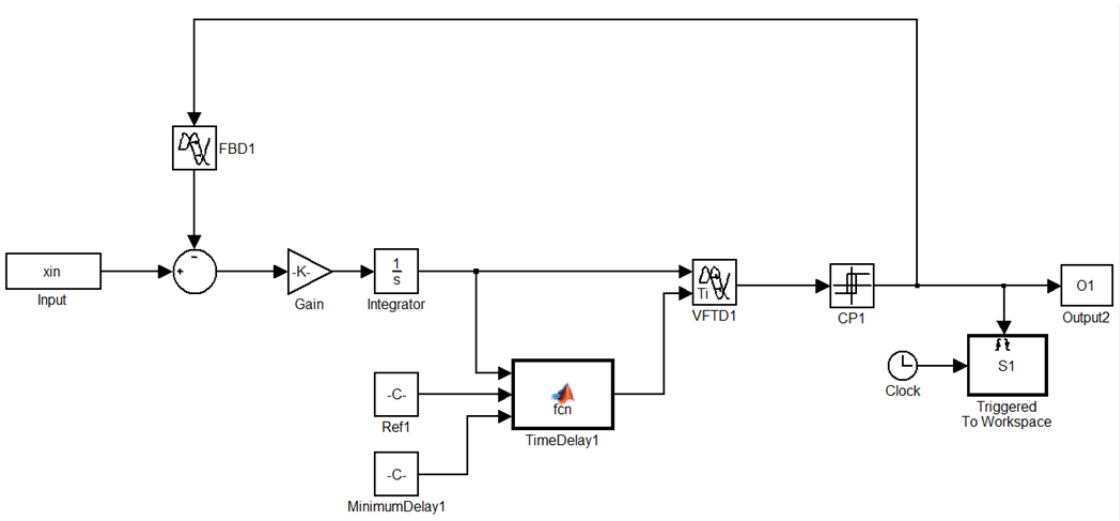


Figure 2-19: Variable time dependent delay model to simulate propagation delay of a comparator

model is implemented in Simulink® as in Figure 2-19. The results show a good match between this *variable time dependent delay* model and the linear model.

Simulation results demonstrate that increasing t_p results in a higher distortion level in a fixed bandwidth. Additionally, the distortion caused by the propagation delay is similar to the distortion caused by the hysteresis value of the comparator; increasing propagation delay increases distortion in the baseband due to harmonics of $\omega_c$in the baseband.

2.4.2. Nonlinearity

The main sources of nonlinearity in ASDMs are from the nonlinearity of the integrator used as a low-pass filter and the feedback multi-bit DAC. The effects of both of these nonlinearities have been discussed in Section 2.3.

In [14], a brief discussion on the effects of a non-ideal integrator is reported. In case of o*p-amp-based RC integrators, finite op-amp gain* results in a leaky integrator. In case of

Noise Source	SFDR (dB) @10KHz BW	SNDR (dB) @10KHz BW	SNR (dB) @10KHz BW	Figure #
Comparator	82.0	72.4	72.4	Figure 2-20(a)
Integrator	28.5	27.3	42.3	Figure 2-20(b)
Input/Feedback	64.1	55.1	55.1	Figure 2-20(c)

Table 2-6: Noise suppression analysis in ASDM

$G_m.C$ integrators, the nonlinearity arising from nonlinear $G_m$stages is critical. Several circuit techniques have been reported to design linear trans-conductors.

In case of feedback DAC, the main source of nonlinearity is the mismatch between unit elements in the DAC array. The effect of the nonlinearity seen in ASDM is similar to what is observed for CT-SDMs, and therefore was not investigated in detailed here [15, 16]. Approaches that work to improve the linearity metrics in CT-SDM are more or less equally applicable here.

2.4.3. Noise

No quantization happens inside the ASDM loop, so no quantization error is introduced inside the loop. Thus, noise from the sigma-delta loop comes from thermal and flicker noise of the in-loop components; this is also the case in CT-SDMs. The circuit level noise sources from LP-Filter and feedback DAC can be modeled as additive noise sources to the input signal and the *signal transfer function (STF)* filters them, but the noise contributed from comparator are filtered out with the *noise transfer function (NTF)* of the sigma-delta loop.

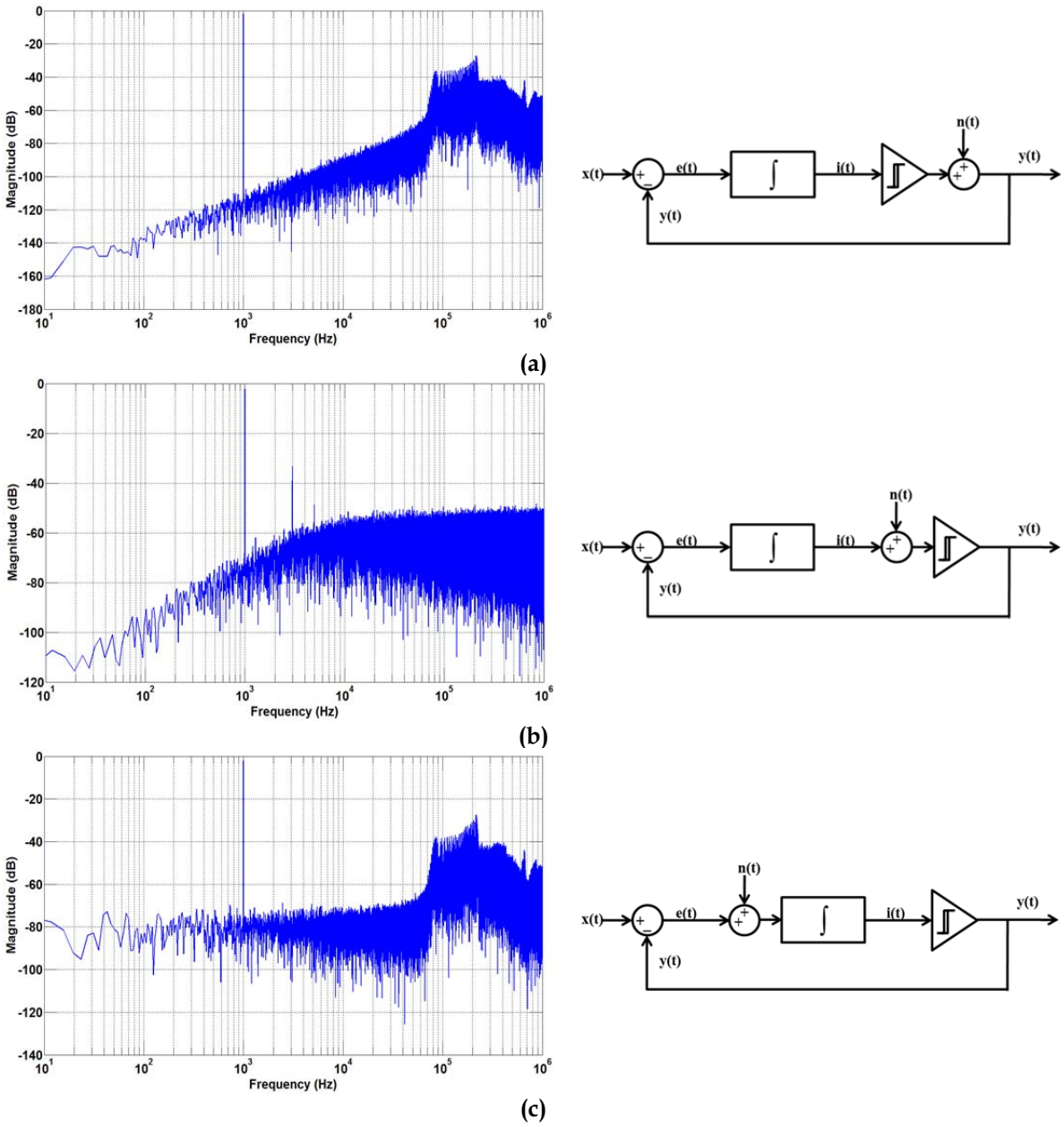


Figure 2-20: Output spectrum (Hanning window) of an ASDM in the presence of noise (a) comparator noise, (b) integrator noise, (c) input and/or feedback circuitry noise the noise sources added in these 3 models are white noise with power of -20dB

Figure 2-20 compares the effect of sigma-delta loop on three different noise sources in the loop. The results are also tabulated in Table 2-6. The simulation parameters are same as in Table 2-1 except that the noise sources added in these three models are $-20dB$ white noise sources. A *Hanning window* is applied to the output data in all

three cases. As can be seen from the spectrums, ASDM loop, like in CT-SDM case, filters out the comparator noise but the input/feedback circuitry noise is almost intact.

Finally, it can be concluded that, ASDMs show better noise performance metrics than CT-SDMs. Since no quantization error is being aggregated in the integrator, ASDMs are more robust than CT-SDMs.

2.5. Dynamic Errors in Asynchronous Sigma-Delta Modulators

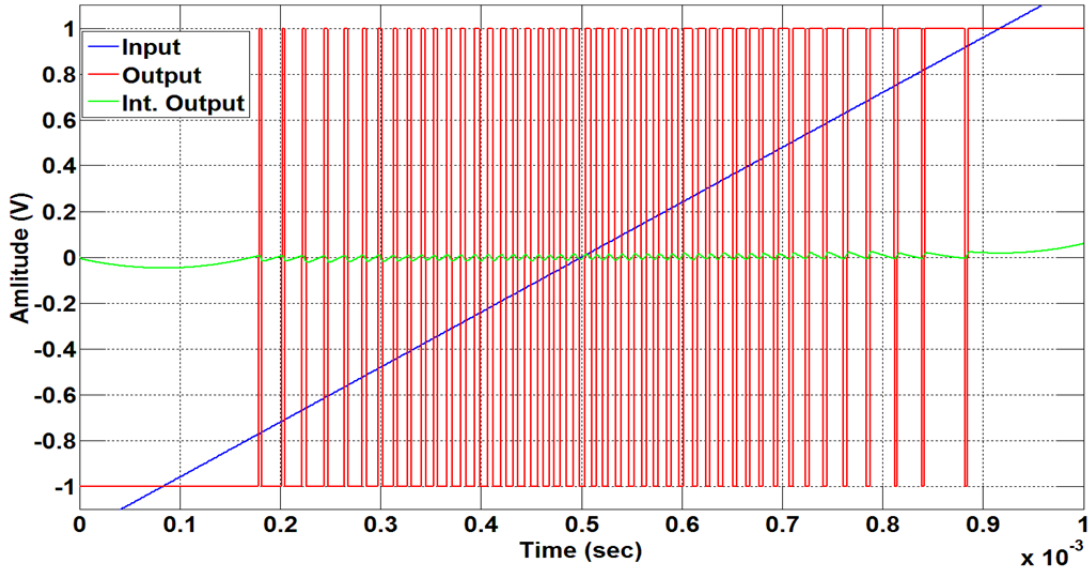
Dynamic errors are classified as error sources which depend on amplitude or frequency of the input signal. These sources can be avoided through careful design or can be compensated for using digital back ground calibration. *Overload* and *saturated integrator* are the errors belonging to this subset.

2.5.1. Overload

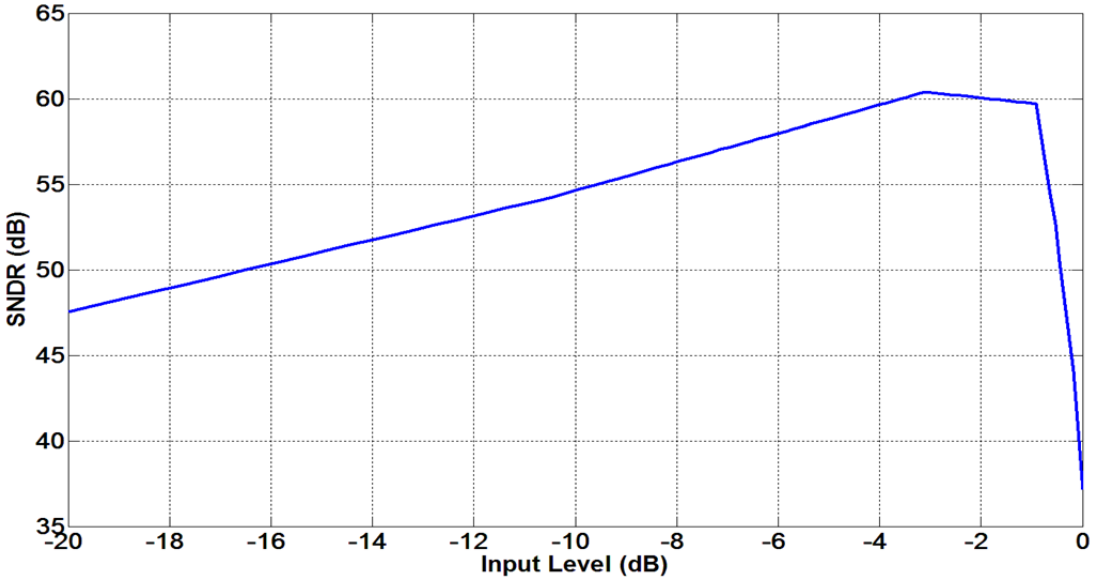
Input dynamic range of the ASDM must be less than dynamic range of the feedback signal. If the input signal exceeds this limit, it overloads. The error accumulated in integrator due to overload makes the integrator output exceed $\pm h$ boundaries. This phenomenon leads to instability of the whole sigma-delta loop.

Because of the odd symmetry nature of square waves, the output spectrum of an asynchronous sigma-delta modulator does not bear any even harmonics of the center frequency, ω_c. Thus, as calculations in section 2.2 prove, this system is more vulnerable to the Bessel tones of the first and third harmonics of ω_c penetrating into the band of interest than other harmonics. However, input signal level adversely affects the distortion level. It forces the unwanted Bessel harmonics of the center frequency penetrate into the band of interest degrading the performance of the whole circuit. Thus the amplitude of input signal should be bounded in order to prevent from any distortion.

In [17], a descriptive analysis of non-overload criteria in clocked sigma-delta modulators is presented. In the case of asynchronous sigma-delta modulators, in the



(a)



(b)

Figure 2-21: Overload Test; (a) integrator output (saw-tooth waveform) is changing linearly with input amplitude (ramp) except in the overload condition, (b) SNDR variation vs. modulation depth

absence of the quantization noise, this criterion can be formulated as:

$$|R| \geq |STF|.\|v_{in}\|_{\infty} \tag{2-24}$$

where $|R|$ is half of the full scale range, $|STF|$ is the magnitude of the input-output (signal) transfer function, and $\|v_{in}\|_{\infty}$ denotes the maximum amplitude of the input

signal. However, in ASDMs, where a hysteresis comparator is used as nonlinear component in the loop, the closed-form equation of (2-24) is difficult to determine analytically. Thus, we should rely on simulations or empirical results.

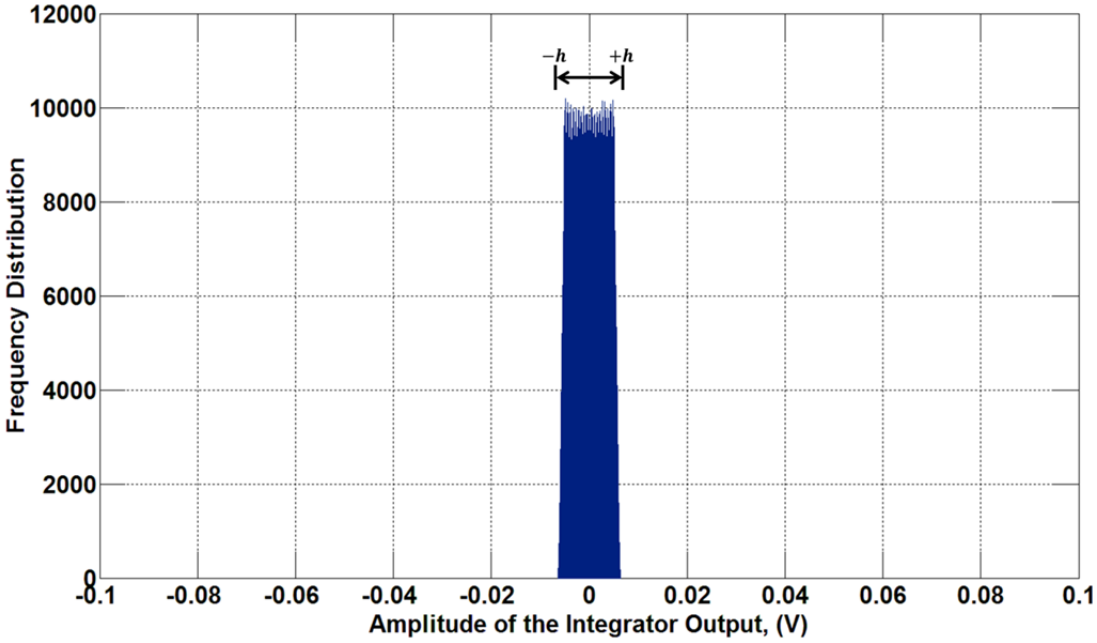


Figure 2-22: Histogram of output of the integrator

To simulate what happens in an ASDM as input overloads, a ramp signal, varying from -1.2V to 1.2V is applied to the input of the modulator (for -1V to 1V full scale). As shown in the Figure 2-21(a), the duty-cycle of the output square wave changes linearly with the amplitude of the input ramp. In this picture, the saw-tooth waveform (output of the integrator) varies between +h and -h (hysteresis levels of comparator).

However, as input amplitude reaches (roughly) 90% of the full-scale level, nonlinearity in integrator output appears and SNDR drops rapidly (Figure 2-21 (b)). In Figure 2-22, the distribution of the instant amplitudes of the integrator output is

plotted. This histogram proves that the output of the integrator is bounded to ±h. As conclusion, the loop is stable as long as the input is not overloaded.

2.5.2. Saturated integrator

As discussed in section 2.5.1, as long as the input voltage signal is bounded to levels less than approximately 90% of the dynamic range of the feedback signal, the output of the integrator is bounded to $\pm h$. Unlike continuous-time sigma-delta modulators, the output of the integrator in ASDMs never clips, since the magnitude of the hysteresis level is always designed to be much less than full scale dynamic range. That is, if $|v_{in}(t)| \leq c < \frac{DR_{FS}}{2}$ then the output of the integrator$|I(t)| \leq h$. This, in turn, leads to the stability of the sigma-delta loop. In Figure 2-22, it is obvious that the output of the integrator is bounded to$\pm h$, a value much less than the full scale output dynamic range of the integrator.

2.6. **Reconstruction**

As stated before, an asynchronous sigma-delta modulator can be interpreted as a *time encoding machine (TEM)* which converts input signal amplitude information to time information of the output square wave signal. As long as this time encoding machine is not overloaded, that is, if $v(t);\ t \in \mathbb{R}$ is a finite energy band-limited signal and $|v(t)| \leq V_{max} < 1$, then the TEM is stable and has an *one to one function* for conversion from amplitude to time information [7]. Afterward, this time information must be quantized and digitized.

In order to perform more calculation on the data using traditional DSP systems, the amplitude information of the original signal must be recoverable from digitized time information (see Figure 2-1). To reconstruct the original signal in digital domain, a *time decoding machine (TDM)* has to be employed.

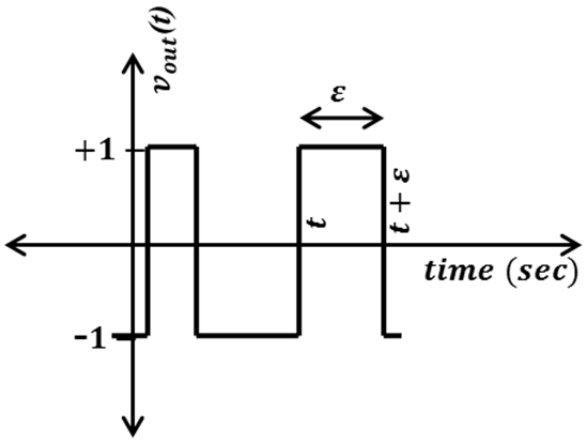


Figure 2-23: Timing frame of the output square wave signal

A detailed descriptive analysis on the recovery problem from a TEM is done in [6, 7, 18]. Based on calculations done in [7] the amplitude information of the original

signal can be perfectly recovered if the time interval between any two consecutive triggering edges of the output square wave is bounded by the *Nyquist period*. That is, in Figure 2-23, if

$$\forall t \in \mathbb{R};\ \varepsilon \leq \frac{1}{F_{Nyq}} \tag{2-25}$$

then, the encoded amplitude information can be recovered perfectly. The output square wave of the ASDM, sampled at a sampling frequency higher than the inverse of the minimum time interval between triggering edges, can be presented in digital domain without any aliasing.

A typical way to reconstruct the signal is to filter the output signal using a digital low pass filter. A decimation filter in particular helps to deemphasize the high frequency components of the output spectrum and retain the original signal by reducing the effective number of samples. Since the filtering method is linear while the ASDM loop is nonlinear, the main problem with this method is the number of non-harmonic components that appear in the band of interest. To remove these components, the filter order must be high or the base band must be narrow enough. Otherwise, the OCR must be considered very high resulting in more power consumption. Thus, a nonlinear reconstruction method is more preferable than a filtering method.

To reconstruct the original signal a vector-based reconstruction method is developed in [6]. In this method, a pseudo-inverse matrix based on time intervals

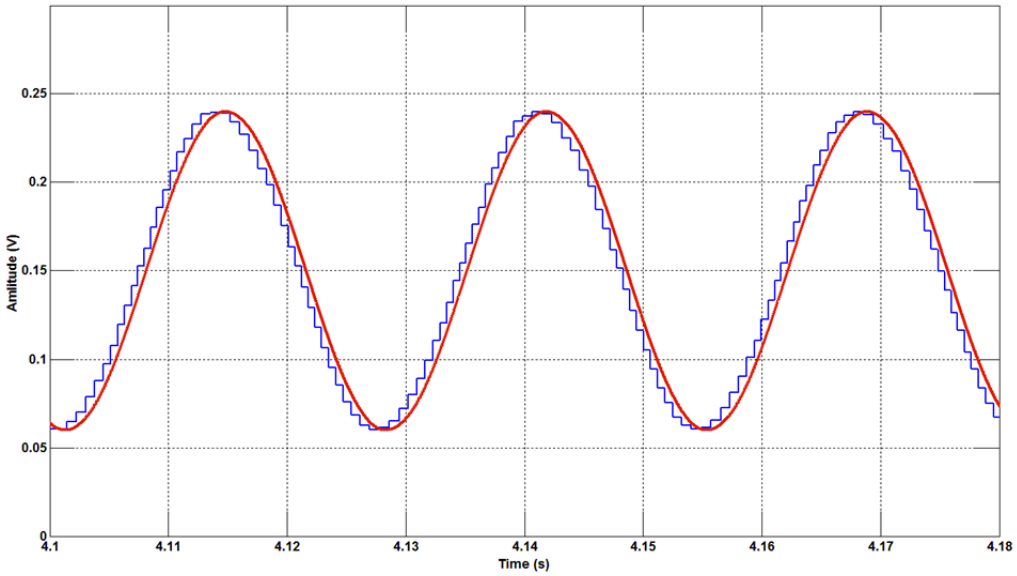
between consecutive triggering edges of the output signal is constructed and applied iteratively to the original signal. As the number of iterations increases the result converges to the reconstructed input signal. This method perfectly reconstructs the signal but in a trade-off with speed and resources.

A simple method to reconstruct the signal is developed based on (1-1) and (1-2) in [19]. With a slight change in this method the original signal can be reconstructed as:

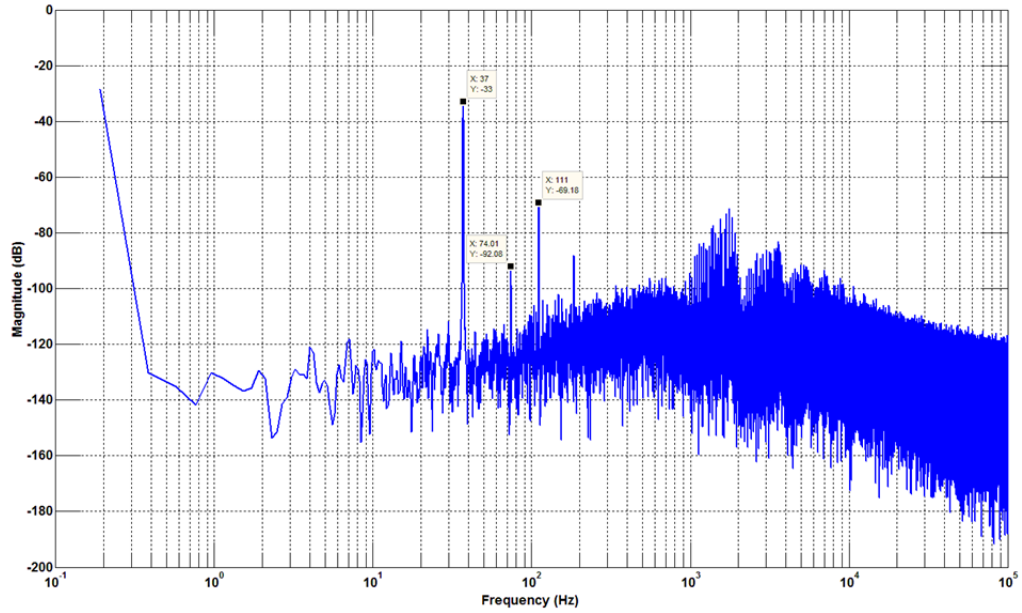
$$v_{rec}(t) = \frac{\alpha\lfloor t \rfloor - \beta\lfloor t \rfloor}{\alpha\lfloor t \rfloor + \beta\lfloor t \rfloor} \tag{2-26}$$

where $\alpha\lfloor t \rfloor + \beta\lfloor t \rfloor = T\lfloor t \rfloor$ and $\alpha\lfloor t \mid t_n \leq t < t_{n+1} \rfloor = \alpha(t_n)$. This method is applied to the output of a semiconductor-level ASDM regularly sampled at 2MS/sec. The circuit parameters in this experiment are same as Table 2-3 except for the input frequency which is 37Hz. The reconstructed staircase signal is plotted in Figure 2-24(a). In this method, as is implied in (2-26), the value of the reconstructed amplitude for the time interval $t_n \leq t < t_{n+1}$ between two consecutive rise and fall edges of the square wave signal is calculated based on the pulse width and period of the former period. Thus, memory blocks used in this reconstruction method shifts the reconstructed signal to the left.

The output spectrum of the reconstructed signal is also depicted in Figure 2-24(b). As mentioned before, since the ASDM is constructed of single-ended components, a number of harmonics can be distinguished out of the noise floor.



(a)



(b)

Figure 2-24: Simple signal reconstruction
(a) reconstructed signal (staircase) vs. original signal
(b) spectrum of the reconstructed signal (rectangular window)

The benefit of this method is its simplicity in implementation and speed. Speed and precision are traded off in this reconstruction method.

Chapter 3

Variants of Asynchronous Sigma-Delta Modulator

3.1. Introduction

As discussed in chapter 2, ASDMs improve the resolution of data converters by utilizing the improved time resolution achievable with shrinking CMOS technologies. Our research proves that the amplitude-to-time conversion process is somehow distorted because of many error sources in real ASDM loops.

Inspired of the mature CT-SDM technology, different approaches are developed to solve these issues in ASDMs. However, these approaches need to be investigated to make them applicable for the ASDM. Among these approaches, *multi-level asynchronous sigma-delta modulators (ML-ASDM)* and *band-pass asynchronous sigma-delta modulators (BP-ASDM)* are discussed in this chapter.

Generally, multi-level conversion is used to increase the dynamic range. Any extra bit added to the quantizer results in a $6dB$ improvement in the resolution. However, simulation results show that this assumption is not valid in ML-ASDM architecture. This approach is intuitively discussed in section 3.2.

On the other hand, to increase the speed of the ASDM while preserving the dynamic range, a narrow-band band-pass filter can be implemented instead of the

low-pass filter used in ASDMs. By limiting the bandwidth, noise metrics improve and higher frequency conversion can be achieved. Using this bandwidth-speed relationship, ASDMs for higher frequency applications can be developed. Section 03.3 intuitively analyzes BP-ASDM architecture and possible issues with it.

3.2.Multi-Level Asynchronous Sigma-Delta Modulator

Core part of asynchronous sigma-delta ADCs is a *Bi-Level ASDMs (BL-ASDMs)* which serves as an amplitude to time converter. Our research shows that the amplitude-to-time conversion process is somehow distorted because of many error sources in real BL-ASDM loops. Inspired from the mature continuous-time sigma-delta modulators, we explored the option of adding multiple levels into the level crossing comparator inside the loop akin to multi-bit quantizer in CT-SDMs. We coin the term Multi-Level Asynchronous Sigma-Delta Modulation (ML-ASDM) for such architecture.

We expect that increasing the number of levels will achieve better resolution and increased dynamic range for ADCs. Ideally, doubling the number of levels, *n*, results in $6dB$ increase in the output SNDR [20] in case of CT-SDMs. However, our simulation results show that this result is not observed in ML-ASDM architecture.

To setup an n-level ASDM, $n-1$ comparators are needed. Without loss of generality, we will consider the case of $n=4$; thus three comparators are needed. The schematic of such a ML-ASDM is depicted in

Figure 3-1 in which the three output levels are combined together based on activity-select method developed in [19]. In *n*-level ASDMs the output of each comparator will switch between $V_{OL}=\frac{V_{IL}}{n-1}$ and $V_{OH}=\frac{V_{IH}}{n-1}$, where V_{IH} and V_{IL} are defined respectively as input high and low trigger levels of the comparator, and V_{OH} and V_{OL} are defined respectively as its output high and low levels.

Parameter		Symbol	Value
Input frequency		f_{in}	$1KHz$
Bandwidth of interest		BW	$10KHz$
Input offset		V_{ofs}	$0V$
Dynamic range		DR	$2V$
Modulation depth		MD	80%
Maximum input amplitude		A_{max}	$1V$
Integrator coefficient		$1/k$	$\frac{1}{RC} = \frac{1}{(20pF \times 10M\Omega)} = 5KRad/s$
Sampling rate		F_s	$8\,MSample/s$
Number of FFT samples		N	$2^{24}\ Sample/s$
1st Comparator	Hysteresis value	h_{-1}	$5mV$
	Comparator high input level	V_{IH-1}	$+5mV$
	Comparator low input level	V_{IL-1}	$-5mV$
	Comparator offset	V_{ref-1}	$-5mV$
	Comparator high output level	V_{OH-1}	$+\frac{DR}{2} = +1V$
	Comparator low output level	V_{OL-1}	$-\frac{DR}{2} = -1V$
2nd Comparator	Hysteresis value	h_0	$5mV$
	Comparator high input level	V_{IH0}	$+5mV$
	Comparator low input level	V_{IL0}	$-5mV$
	Comparator offset	V_{ref0}	$0V$
	Comparator high output level	V_{OH0}	$+\frac{DR}{2} = +1V$
	Comparator low output level	V_{OL0}	$-\frac{DR}{2} = -1V$
3rd Comparator	Hysteresis value	h_{+1}	$5mV$
	Comparator high input level	V_{IH+1}	$+5mV$
	Comparator low input level	V_{IL+1}	$-5mV$
	Comparator offset	V_{ref+1}	$+5mV$
	Comparator high output level	V_{OH+1}	$+\frac{DR}{2} = +1V$
	Comparator low output level	V_{OL+1}	$-\frac{DR}{2} = -1V$
Input noise power		σ_N^2	$-60dB$
Input signal		$v_{in}(t)$	$A_{max} \times MD \times \sin(2\pi f_{in} t) + Noise$

Table 3-1: Simulation parameters assumed for ML-ASDM circuits

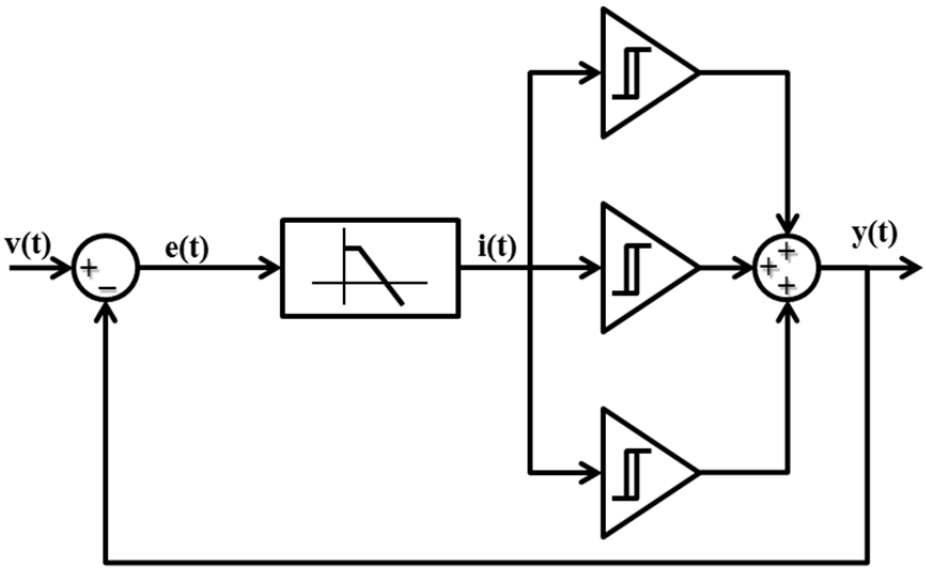


Figure 3-1: Schematic of a 4-level ASDM

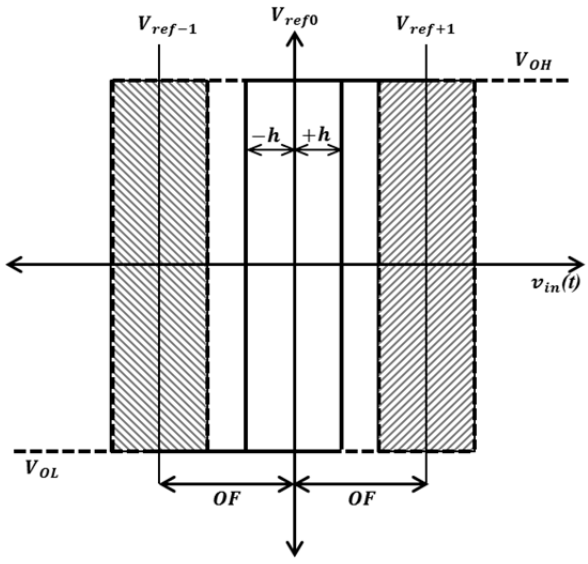
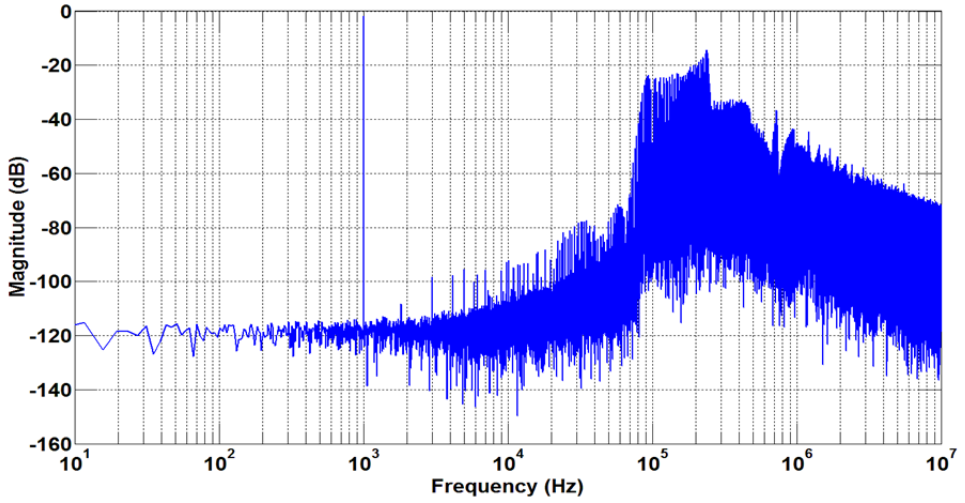


Figure 3-2: Hysteresis plot of three comparators in 4-level ASDM

A difficulty in designing ML-ASDMs is how to set the reference voltage of each comparator. Approximately, they can be set to $m \times V_{FS}/n$ where m is a non-negative integer from *0* to *n-1* [20]. In Figure 3-2, depicting the hysteresis plot of comparators and their respective reference voltage in a 4-level ASDM, changing the *overlap factor (OF)* can control the activity of the side comparators. Our studies on the 4L-ASDM



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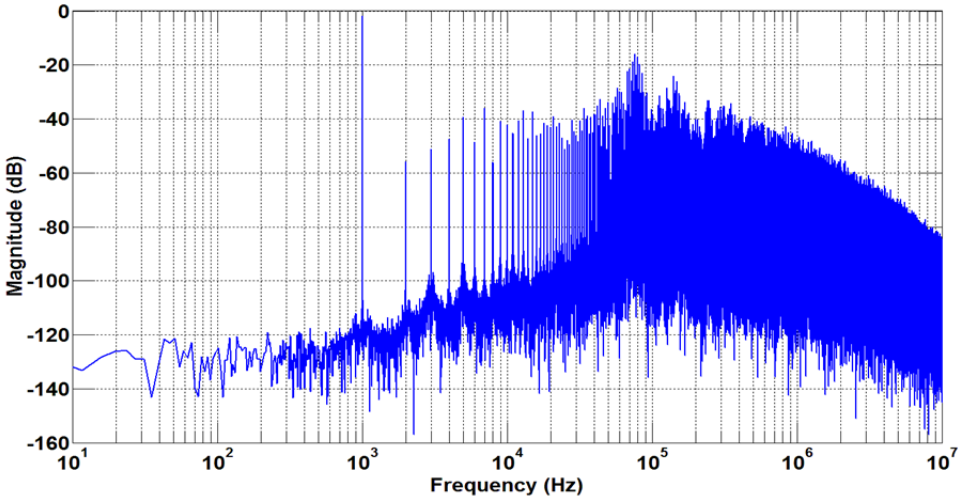

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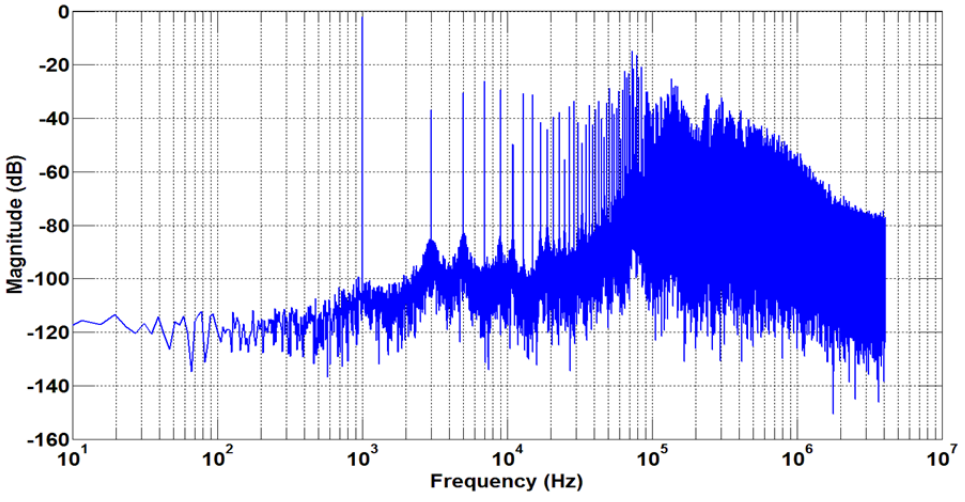


(c)

Figure 3-3: Output spectrum (rectangular window)of three different overlap values in a 4-level ASDM, (a) OF=0, (b) OF=2h, (c) OF=V_{FS}/4

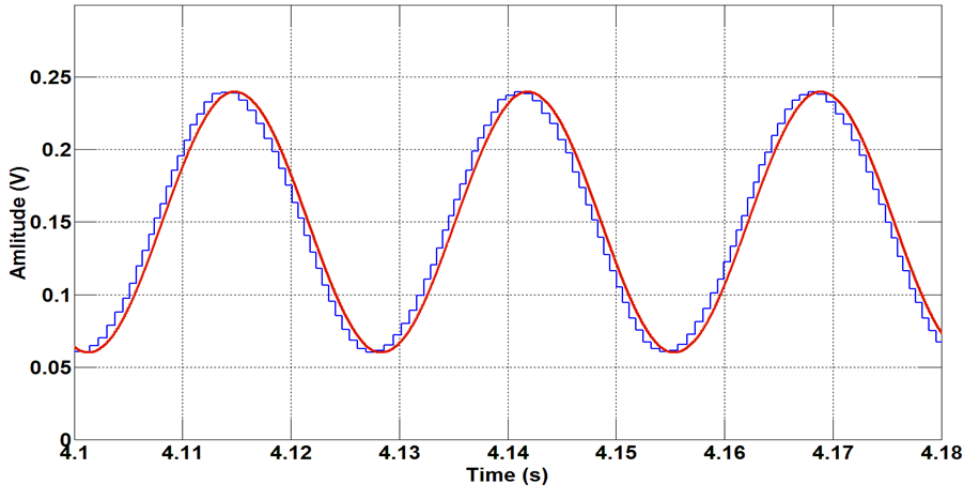
Offset level	SFDR (dB) @10KHz BW	SNDR (dB) @10KHz BW	SNR (dB) @10KHz BW	Figure #
0	86.2	67.5	67.5	Figure 3-3(a)
2h	28.2	26.7	18.6	Figure 3-3(b)
FS/4	19.5	18.6	18.6	Figure 3-3(c)

Table 3-2: Comparators' offset level change test in ML-ASDM

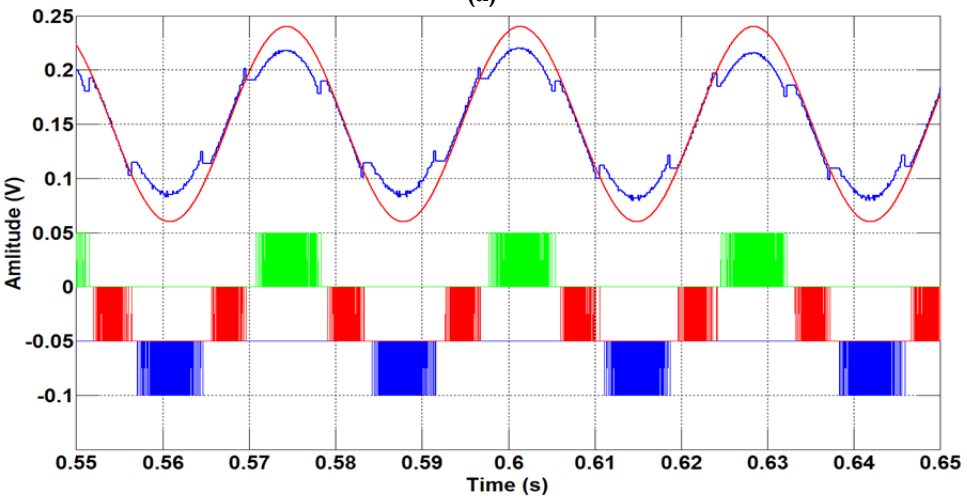
show that increasing the difference between reference levels of comparators distorts the output signal as shown in Figure 3-3. Circuit parameters in these simulations are tabulated in Table 3-1. The performance metrics of the ML-ASDM with different offset factors are tabulated in Table 3-2. The best SNDR is achieved when reference levels of all comparators completely overlap (OF=0); i.e. in its best case performance of an ML-ASDM shrinks to a BL-ASDM (see Figure 3-3). This is explained qualitatively below.

The reconstructed signals in Figure 3-4 illustrate that the output signal of a BL-ASDM can be perfectly reconstructed, but ML-ASDMs consist of dead-zones, which causes the reconstructed output of signal of the ML-ASDM to be distorted.

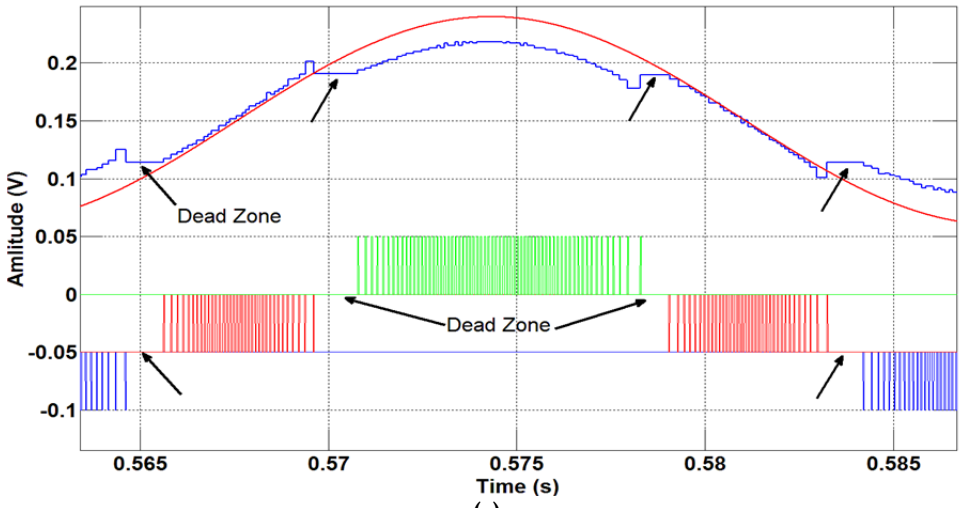
Dead-zones are caused while transitioning from one comparator to another with increasing integrator (low pass filter) output. Consider a case where the increasing output of the integrator (line $d1$ in Figure 3-5) has touched the $+h$ hysteresis edge of the bottom comparator. At this time, the output level of this comparator, V_{OH-1} is triggered which in turn generates a feedback such that output of the integrator $I(t)$ decreases. The output of the integrator $I(t)$ follows the line $d2$ in Figure 3-5. Please note along the trajectory *d1*, there is a time when there is no switching activity from both the bottom and middle comparator leading to an apparent dead zone. Let's



(a)



(b)



(c)

Figure 3-4: Reconstructing output signal of ASDMs
(a) reconstructed signal of a BL-ASDM, (b) reconstructed signal of a 4L-ASDM, (c) reconstructed signal of a 4L-ASDM with dead-zones

consider when $I(t)$ reaches the high hysteresis level of the middle comparator, $+h$, the feedback signal $(V_{OH-1} + V_{OH0})$ is generated which causes the integrator to reverse course following trajectory $d3$. The dead-zone similarly appears during transition between the middle and top comparator. This analysis suggests that inherent hysteresis in multi-level comparators results in dead-zones, which introduces nonlinearities degrading SNDR.

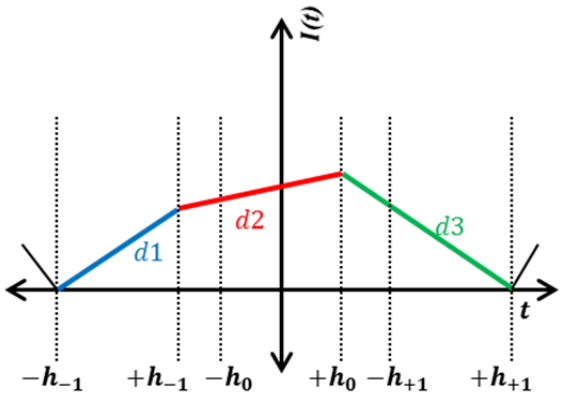


Figure 3-5: A case study on the integrator output in (blue line d1, red line d2, and green line d3)

In conclusion, the results show that a ML-ASDM not only doesn't improve the SNDR by a factor of $6dB$ in a definite bandwidth, but it also introduces harmonics and degrades the SNDR.

3.3. Band-Pass Asynchronous Sigma-Delta Modulator

In this thesis, we propose a different scheme of asynchronous sigma-delta modulators, a *band-pass ASDM (BP-ASDM)*. Referring to Figure 2-4, in place of a low-pass filter in the sigma-delta loop a Band-Pass filter can be used. This filter only passes those frequency components of the error signal bounded to frequency range of the filter. To design this filter, traditional analog filter design skills are helpful. In all simulations in this section a second-order Butterworth filter is used.

Parameter	Symbol	Value
Input frequency	f_{in}	$1GHz$
Bandwidth of the filter	BW	$200KHz$
Center frequency of the filter	f_{cen}	$1GHz$
Filter type	-	second-order Butterworth
Input offset	V_{ofs}	$0V$
Dynamic range	DR	$2V$
Modulation depth	MD	80%
Maximum input amplitude	A_{max}	$1V$
Integrator coefficient	$1/k$	$\frac{1}{RC} = \frac{1}{(20pF \times 10M\Omega)} = 5KRad/s$
Sampling rate	F_s	$8\,MSample/s$
Number of FFT samples	N	$2^{24}\ Sample/s$
Hysteresis value	h	$5mV$
Comparator high input level	V_{IH}	$+5mV$
Comparator low input level	V_{IL}	$-5mV$
Comparator offset	V_{ref}	$0V$
Comparator high output level	V_{OH}	$+\frac{DR}{2} = +1V$
Comparator low output level	V_{OL}	$-\frac{DR}{2} = -1V$
Input noise power	σ_N^2	$-60dB$
Input signal	$v_{in}(t)$	$A_{max} \times MD \times \sin(2\pi f_{in} t) + Noise$

Table 3-3: Simulation parameters assumed for BP-ASDM

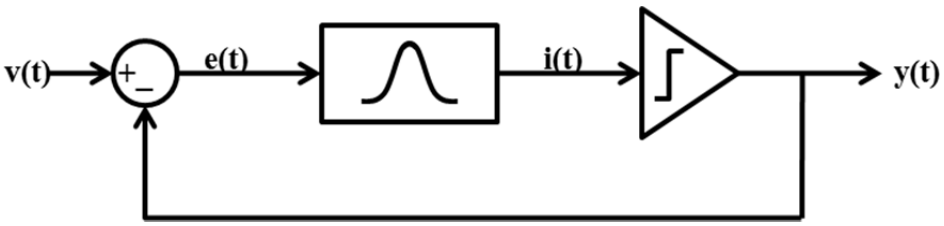
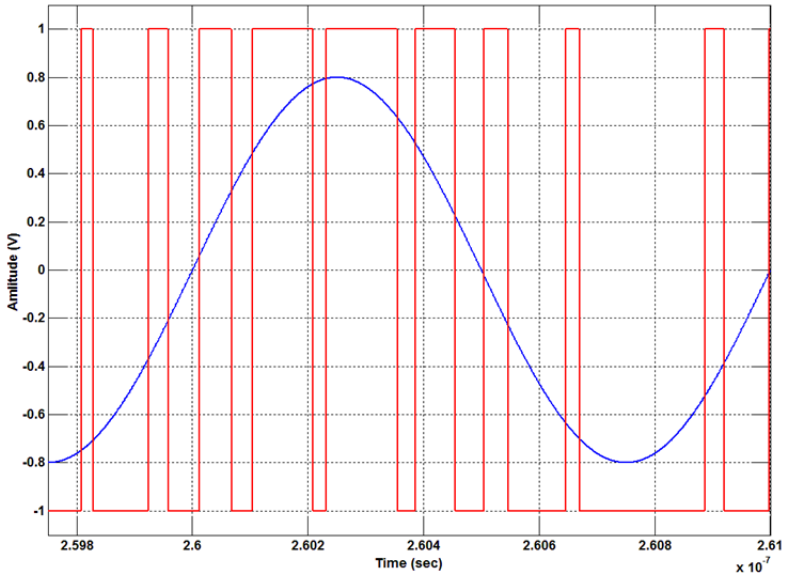
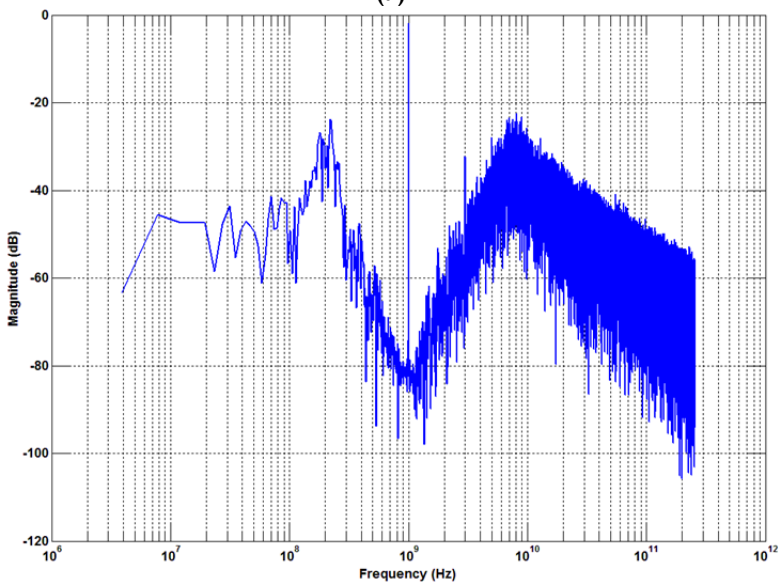


Figure 3-6: General Architecture of a Band-Pass ASDM



(a)



(b)

Figure 3-7: Output of an ideal Band-Pass ASDM (behavioral model) in response to a 1GHz input signal at 80%MD (a) Transient Response, (b) Frequency Response

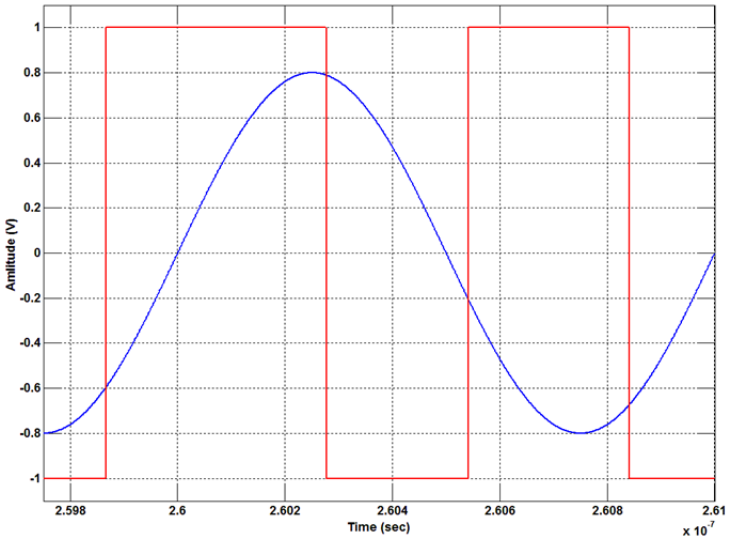
In band-pass filter design, at least two poles and one zero are needed. Thus, if the system is designed with non-minimum phase, the phase shift needed to satisfy

Barkhausen criteria is satisfied just with implementing the filter. This means that the loop oscillates even in the absence of the hysteresis phenomenon and the hysteresis comparator can thus be replaced by a simple comparator. However, presence of hysteresis comparators helps to prevent unwanted triggers due to noise sources. The architecture of the BP-ASDM is presented in Figure 3-6.

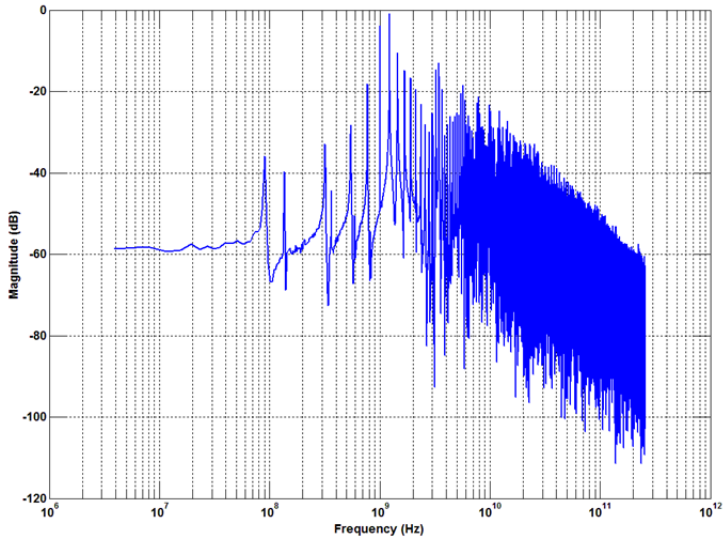
A behavioral model of the BP-ASDM is simulated and the results are shown in Figure 3-7. The circuit parameters are listed in Table 3-3.

In this thesis, such BP-ASDMs are targeted for mid-band radio-frequency applications. Thus, the test frequency in these experiments is selected high enough to consider all complexities of low frequency design accompanied with this type of modulators and converters.

As can be seen from Figure 3-7(a), the output signal is very dense; the time intervals between two consecutive output transitions can be on the order of femto seconds for band-pass filters with center frequency of $1GHz$. This conveys that high frequency BP-ASDMs are vulnerable to distortion caused by any delay in the loop, especially the propagation delay of the comparator. Figure 3-8 shows output results of the same BP-ASDM as above except for the comparator with a propagation delay model as in equation (2-22). A linear delay of $10fs$ and a time constant of $50fs$ are applied as τ_d and τ_c, respectively. These results show that even a small amount of delay results in a lot of distortion added to signal which destroys the original signal.



(a)



(b)

Figure 3-8: Output of a band-pass ASDM (behavioral model) with delayed comparator in response to a 1GHz input signal at 80%MD (a) transient response, (b) frequency response

Therefore, to employ this type of ASDM in high frequency *data converters*, the circuit delay and the time quantization resolution must be carefully considered.

Chapter 4

Conclusion

4.1. Introduction

A wide range of applications of analog to digital converters forces designers to design ADCs with improved performance. Continuously shrinking CMOS fabrication technology helps designers to achieve higher performance from standard designs. However, affecting maximum achievable dynamic range of the ADCs, this down scaling, also degrades the resolution. Thus, designing high resolution ADCs in the amplitude domain is complex and difficult. Transferring amplitude information to time information is a possible solution. Decreasing CMOS process size yields increasing time resolution which in turn improves the dynamic range of ADCs.

In the present report, a comprehensive analysis of the different error sources in asynchronous sigma-delta modulators and their effect on the performance of the whole system is presented. These errors are categorized into input-dependent and input-independent subsets.

In [3] a descriptive frequency domain analysis of ASDMs based on the harmonic Fourier transform is done and in [6] a time domain analysis based on frame theory is performed. However, neither of these analyses combines both time and frequency domain analysis to intuitively present the concept of ASDMs.

Two ASDM structures that can solve problems in conventional ASDMs are investigated. The pros and cons of these structures against the simple ASDM are discussed intuitively. Our studies show that implementing multi-level ASDM will not result in improvement in the resolution of the ASDM. However utilizing a band-pass filter instead of low-pass filter in the ASDM increases the work frequency while improving the resolution at the same time.

The presented report helps to intuitively understand asynchronous sigma-delta modulators and their variants, understand the error sources and their effects, and provides good insight into design steps of a high-performance ASDM.

4.2. Future Works

The focus of this thesis was on the modulator core and its error sources In addition to the Modulator, a time-to-digital converter is also a main part of ASDM-based ADCs. The quantization noise introduced in this stage is the most important error source. Thus, a qualitative analysis on ASDM-matched TDCs and their error sources affecting the output signal is needed.

Moreover, as a new representation of ASDMs, more investigation on band-pass ASDM structure needs to be conducted in future. A detailed and descriptive analysis of error sources and their solution should be performed for this structure.

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