A Radiation Hardened Mutually Compensated Mobility and Threshold Voltage Reference Approach

A thesis submitted by

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Abstract:

Microelectronics that leave the earth's magnetosphere are exposed to the natural radiation environment and are subject to effects not experienced by terrestrial microelectronics. Device characteristic degradation including off state leakage current, reduced transconductance, and reduced threshold voltage are all potential consequences of being exposed to the natural radiation environment. It would benefit the designer to make these devices radiation hardened. Voltage references are used to provide accurate and stable voltages over a wide range of temperatures and they are crucial to analog integrated circuits (ICs). A radiation hardened by design (RHBD) mutually compensated mobility and threshold voltage reference was designed and tested. Mobility and threshold voltage decrease with increasing temperature. The technique of mutual compensation of mobility and threshold voltage cancels these effects for a given temperature and establishes a zero temperature coefficient (ZTC) for a diode connected MOS. It was found that linearly combining the output voltages of a diode connected NMOS and PMOS that implement this technique achieve a thermally stable voltage reference superior to either the NMOS or PMOS alone.

Acknowledgements:

I would like to take this time to formally thank my adviser at Draper Labs, Rob Bousquet. I could always go by Rob's office and ask him just about anything and he would have an answer to it. He was an excellent mentor to me that would echo concepts learned in class, introduce me to topics not mentioned in academia, and simply talk about the mundane to blow off steam. There is no way that this work could have come to fruition without him. I would also like to thank my thesis adviser at Tufts, Professor Sameer Sonkusale. Sameer provided me with the foundation for analog IC design and I will always be grateful for that. His enthusiasm for the subject was always apparent and easily rubbed off on anyone willing to learn. I'd also like to thank John Lachapelle, Rob, and Sameer for dealing with all of the hurdles balancing work at school and Draper.

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1.0 Introduction

Analog circuits play an important role in electronics including amplifiers, comparators, voltage references, analog to digital converters (ADCs), and digital to analog converters (DACs). Analog IC design comes with many challenges that designers must face. A more esoteric issue is making electronics less susceptible to the effects caused by the natural radiation environment. Electronics that leave the safety of the earth's magnetic field are subjected to high energy particles that can alter device behavior. Some of these effects include reduced transconductance, shifted threshold voltage, and an increase in off-state leakage current. It is important that analog or digital circuits, subjected to the natural radiation environment, are designed such that these deleterious effects do not affect circuit functionality.

There are technologies (processes), as well as circuit topologies and layout techniques (design) that make microelectronics less susceptible to these effects. While some foundries have radiation-hardened technologies, it would be best if design techniques could be used to make circuits radiation-hardened. If designers could implement design techniques regardless of foundry or process it would remove the need to rely on exotic radiation-hardened processes. Radiation effects and how to mitigate their effects on microelectronics will be investigated, as well as the implementation of these well-known techniques. This work focused on using radiation hardening by design techniques on a mutually compensated mobility and threshold voltage reference using a standard-bulk CMOS process.

2.0 Radiation Effects and Mitigation Schemes in CMOS

2.1 Radiation Effects on CMOS

Complementary Metal Oxide Semiconductor (CMOS) technologies have been the dominant technology in integrated circuit (IC) design over the past decades. Design issues exist with shrinking technology nodes. A more esoteric issue for IC designers is making circuits less susceptible to the effects of ionizing radiation. Outside of the earth's magnetosphere there are high energy particles that can cause damage to electronics. Terrestrial electronics are protected by the earth's magnetic field and are not subjected to the amount of high energy particles experienced in space. Two common categories of radiation damage are Total Ionizing Dose (TID) and Single Event Effects (SEEs). TID is caused by solar and trapped particles (protons and electrons) and their subsequent interaction with the field oxide and/or gate oxide (if applicable). They affect bulk CMOS by introducing trapped charged particles at the gate/channel interface and in the gate dielectric [1] [4]. The radiation-induced damage leaves interface and oxide states with net trapped interface charge, N_{IT}, and net trapped oxide charge, N_{OT}, respectively [12]. These accumulated trapped charges cause device degradation and will be explained in more detail in Section 2.1.1. SEEs are caused by single high energy particles (protons and heavy ions) that strike the semiconductor material in a seemingly random manner and can introduce unwanted currents within a device [14]. The damage incurred from SEEs will be discussed in greater detail in Section 2.1.2. The negative effects of TID and SEE can be mitigated through radiation hardened by design (RHBD) techniques.

There are existing technologies that are less susceptible to ionizing radiation [11], but it would benefit designers to use layout techniques and circuit topologies that reduce the susceptibility of

devices to ionizing radiation regardless of which technology is used. TID affects device characteristics such as off-state drain current, threshold voltage, and both subthreshold and linear transconductance; the effects from TID can be mitigated using layout techniques such as enclosed layout/geometry transistors (ELTs) or edgeless transistors. Devices affected by SEEs can be desensitized using layout techniques and circuit topologies. TID and SEE can degrade device performance and must be taken into account for use in systems that are exposed to the natural radiation environment.

All space electronics are susceptible to the natural radiation environment. The natural radiation environment is filled with high energy particles including protons, electrons, heavy ions, and photons that can cause damage to electronics [1] a detailed image of sources of radiation damage in space can be seen in Figure 1 [32].

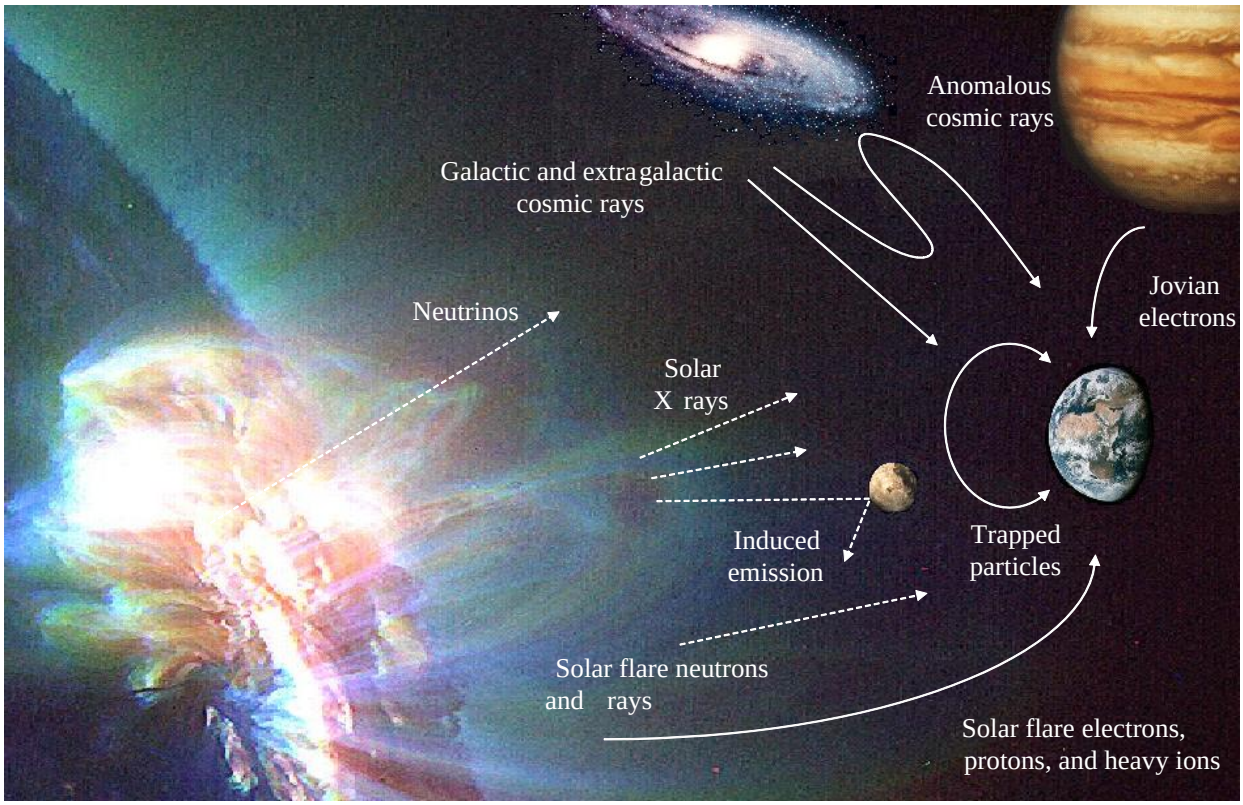


Figure 1: ***The Natural Radiation Environment and Potential Sources of Radiation Damage [32].***

Terrestrial electronics are shielded by the earth's magnetic field and do not experience the flux of these particles found in the natural radiation environment. Whether accumulating charge over time (TID) or in a single strike (SEE), when particles come into contact with semiconductor material it can affect device performance.

2.1.1 Total Ionizing Dose (TID)

The definition of TID is the amount of energy left behind by high energy particles and photons that produce electron hole pairs (ehps). TID is typically measured in rads (radiation absorbed dose), 1 rad = 100 ergs/ 1 gram (material) [3][4], and the SI unit is the Grey (Gy) 100 rads = 1Gy (J/kg). When a particle (proton, heavy ion, electron, or even photon) with sufficient energy comes into contact with a target material like SiO_2 it can produce ehps. The number of ehps produced within the oxide is directly proportional to energy transferred to the target material. The energy lost per unit length during the interaction of the high energy particle or "stopping power" is typically measured in MeV/cm.

Once the incident particle has created ehps, it is widely accepted that there is a prompt recombination of a fraction of the ehps. The recombination rate of the ehps is directly proportional to the electric field in the oxide. The remaining electrons tunnel out of the gate oxide due to their high mobility, while the slower holes remain and are the leading cause of TID damage this is illustrated in Figure 2, [3]. The leftover holes affect the oxide in two different areas. Neutral oxygen vacancies where positive charges adhere and form traps are commonly known as E' centers; these defects are in the gate oxide and near the Si/SiO_2 interface.

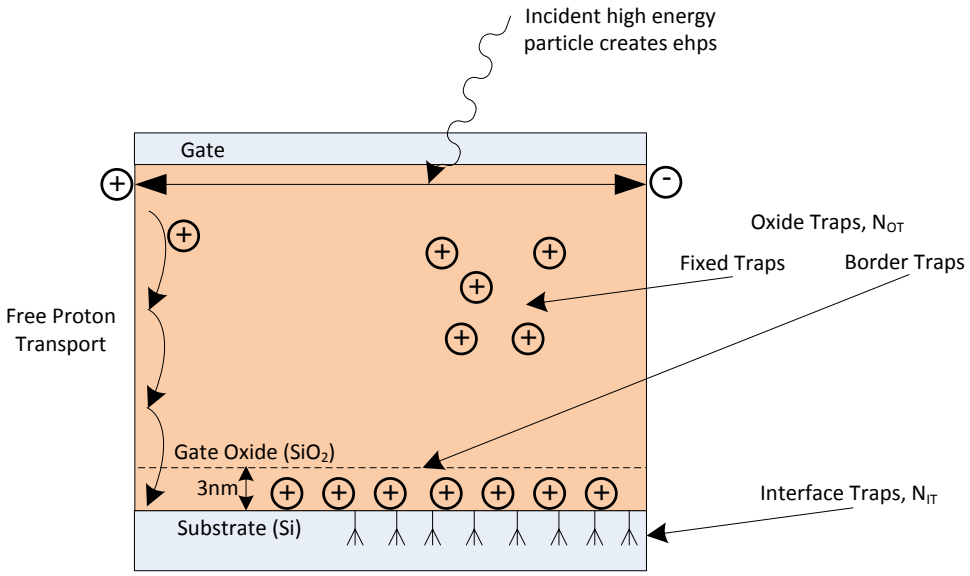


Figure 2: ***Process that leads to TID damage [3].***

TID damage is broken up into two categories, the first are traps occurring >3nm from the Si/SiO_2 interface, these are known as fixed oxide traps. Fixed oxide traps, N_{OT}, are bias independent and can be annealed under certain bias conditions and high temperatures [3]. Fixed oxide traps lead to a negative shift of threshold voltage for both NMOS and PMOS devices shown in Figure 3, [3]. This well documented DC issue is problematic for both analog and digital circuitry and can be expressed in Eq. (1) [3], where ΔV_{OT} expresses the shift in threshold voltage due to fixed oxide charge.

$$\Delta V_{OT} = \frac{t_{ox}}{\varepsilon_{ox}\varepsilon_o} q\Delta N_{OT} \qquad (1)$$

The other type of damage that occurs in the oxide is referred to as switching states. These switching states, also known as border traps or E' centers, occur within 3nm of the interface. E' centers are broken up into two sub categories, E_δ and E_γ, each having different energy levels and vary in location [3]; they both lead to trapped charge in the gate oxide. E_δ centers are thought to trap and reemit

positive charge while E_γ are thought to capture and reemit electrons forming shallow dipole structures near the interface [4].

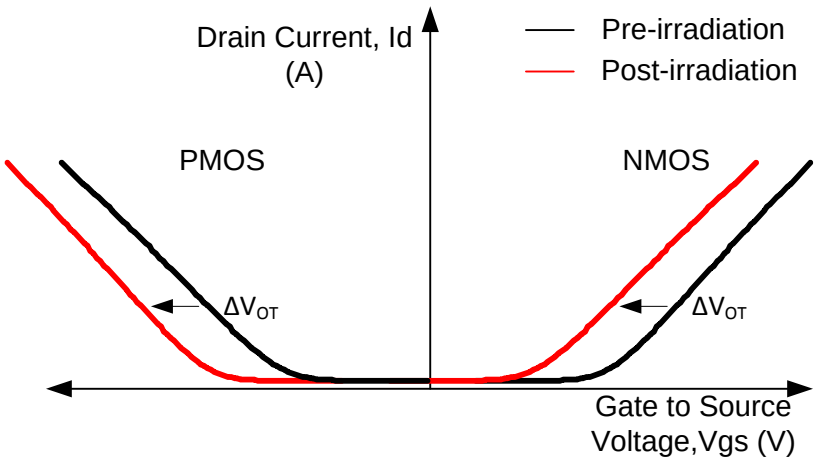


Figure 3: ***Negative Threshold Voltage Shift in NMOS and PMOS due to Fixed Oxide Traps [3].***

The final type of ionizing damage caused by TID is known as interface traps. Interface traps, N_{IT}, are created mostly by protons and can affect the mobility and recombination rates of the carriers at the semiconductor surface. Interface traps are caused from defects called P_b centers and occur directly at the Si/SiO_2 interface. Interface traps and switching states (border traps) have similar DC effects in CMOS. Unlike fixed oxide traps, the DC effects of border and interface traps are bias dependent. Affecting both NMOS and PMOS devices, the most noticeable effect is a decreased slope of the I_D v. V_{GS} curve in the subthreshold and linear regions termed by some as an increase in "subthreshold swing" [3],[5]. Instead of having a sharp rise from the subthreshold region into the linear region and then becoming saturated the FET transitions more gradually from subthreshold to linear and finally saturation. Ionizing damage caused by TID can also affect AC parameters such as noise. The effects of radiation on 1/f or flicker noise have been investigated ([5] and [29]) and it is believed defects found near the Si/SiO_2 interface increase the flicker noise in MOS devices.

As the dimensions of the gate oxide thickness, t_{OX}, become smaller TID becomes less problematic because the DC threshold variation (ΔV_{th}) is directly proportional to t_{OX} raised to some power. The power that t_{OX} is raised to is still in contest with sources. Some contend that ΔV_{th} is proportional to t_{OX}^2 [3], t_{OX}^3 [5], and others t_{OX}^4 [31]. However, it is important to note that the aforementioned ionizing radiation is not limited to gate oxide of semiconductor devices. Shallow trench isolation (STI) is a field oxide used to isolate devices in CMOS; the field oxide is much thicker (300nm-450nm) than gate oxides [15]. In modern technologies, the issues of TID are from the parasitic transistors that form between diffusion regions and the field oxide (see Figure 4 [3]). The negative shift in threshold voltage and increase in subthreshold swing can translate to an increased off-state leakage current (and consequently more static power dissipation). Increased static power dissipation is a downside for both analog and digital circuits (primarily digital), and the negative shift in the threshold voltage can lead to undesired biases and operating points in analog circuitry.

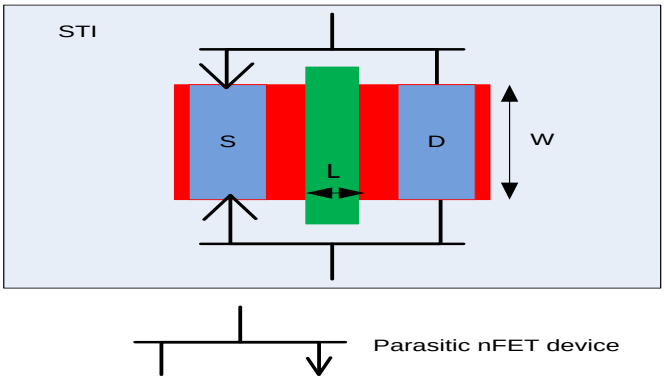


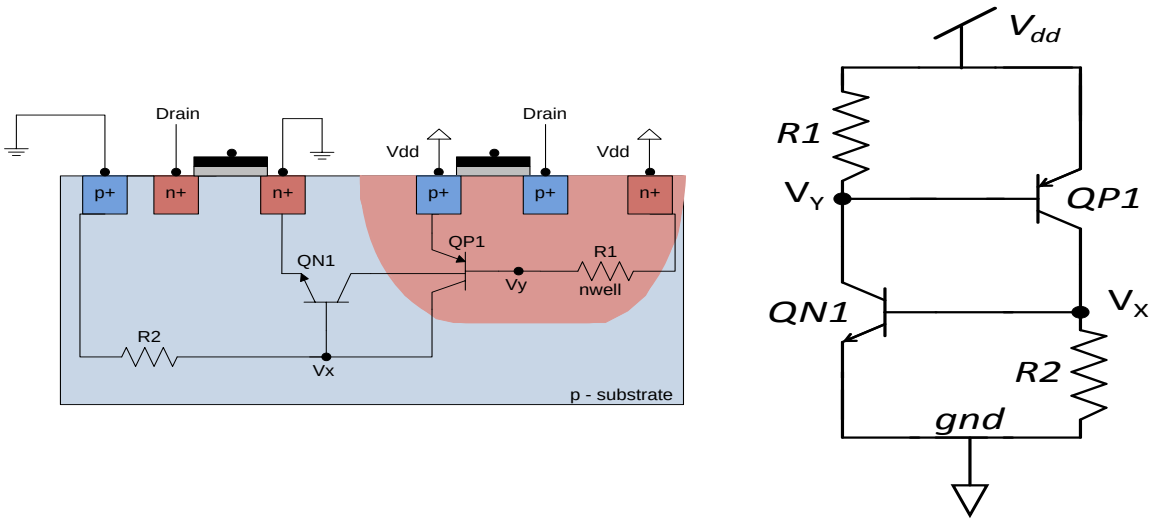
Figure 4: ***Parasitic NMOS devices formed with STI [3].***

2.1.2 Single Event Effects (SEE)

There is another type of ionizing radiation issue for IC designers to address. A single event (SE) or single event phenomenon (SEP) is the interaction of a single ionizing particle (heavy ion, proton, or secondary particle caused by neutron) that comes into contact with a semiconductor material. A SE that causes a response in the circuit is known as a SEE. SEEs are random and can affect any part of the semiconductor material; the effects on the circuit can range from harmless blips to irreparable damage. A useful metric when discussing radiation damage is linear energy transfer (LET). LET is derived from the energy of the incident particle normalized by the target material's density and is usually measured in $MeVcm^2/mg$. SEEs can affect both digital and analog circuitry.

SEEs can be broken up into two broad categories hard and soft errors [13]. These errors can affect single devices that can alter circuit and even system functionality. A soft error is one that can be corrected by reprogramming and is not devastating to performance. A hard error affects functionality and can cause permanent damage. Digital circuitry can be affected by a single event upset (SEU). A SEU is when a high energy particle causes a bit flip, which can lead to changes in memory or states. With digital circuitry becoming denser in modern ICs, it is also possible for a SE to affect multiple bits commonly referred to as a multiple bit upset (MBU).

SEEs can result in excess charge collection in sensitive nodes of semiconductor devices which can lead to unwanted current called single event transients (SETs). A SET can cause a glitch which can lead to an error that propagates through the circuit which can lead to a SEU. Another SEE hazardous to both analog and digital circuitry is single event latchup (SEL). Latchup is when parasitic npns and pnps formed within the p-substrate and n-well (refer to Figure 5 [15]) "turn on" and become "latched-up" causing an increase in drain/source current and static power dissipation [15].



(a) (b)

Figure 5: ***(a) Parasitic npn and pnp which can lead to positive feedback and latchup, and (b) equivalent circuit [14].***

SEL occurs when significant current is injected into the substrate and causes a parasitic transistor to latch up. If node V_X is injected with high amount of charge such that $V_X > V_{BE}$ QN1 will turn on and begin sinking current. At this point V_Y will begin to decrease and if it drops such that $V_Y < V_{DD} - |V_{BE}|$ then QP1 will turn on; while QP1 sources current, V_X will rise. This produces a positive feedback loop. If this occurs in the substrate it may affect circuit performance, and may lead to sustained latchup and device burnout if the forward current gains of QN1 and QP1 are high enough.

2.2 Radiation Hardened by Design Techniques

While some of the effects of TID can anneal over time and some SEEs can be harmless to overall system behavior, there are some effects that cannot be ignored. An increase in off-state leakage current, decrease in threshold voltage, decrease in transconductance, increase in subthreshold swing, and unwanted current in semiconductor material are all side effects of ionizing radiation and threaten device/circuit performance. With the aforementioned problems that can arise from either TID or SEE, implementing design techniques or technology processes are crucial to device through system performance for electronics exposed to the natural radiation environment.

There are some standard CMOS processes that provide decreased susceptibility to ionizing radiation effectively making devices and thus circuits radiation hardened (rad-hard or RH). A few of the RH approaches include triple wells to prevent SEL and thinner STI oxides are also used. It would benefit the design engineer to practice circuit topologies and layout techniques that make circuits RHBD and remove the dependency on a manufacturing process. There is a great deal of literature about layout techniques and circuit topologies aimed at mitigating ionizing radiation effects on CMOS [4]-[10] and [16]. What is clear from the literature is that circuit topologies and layout techniques are used primarily to prevent SEE, while only layout techniques are used to mitigate TID. While these techniques reduce the susceptibility to TID and SEE they inevitably consume more die area. Some of the circuit topology techniques, used for SEE prevention, consume more power as well.

2.2.1 Design Techniques for the Mitigation of SEE

Since SEEs are caused by the introduction of charge in semiconductor regions (including the substrate) they can introduce unwanted current into devices and affect circuit behavior. The brute force

method to mitigate SEEs is to increase the bias currents in the device or circuit such that the unwanted current is significantly less than the bias current and makes no appreciable difference. While this method works, it may not be suited for low power applications. There are two other broad categories to mitigate SEEs: the first is circuit topology techniques and the second is layout techniques. One clever circuit topology used in RHBD is geared towards steering current away from the actual circuit during a SE. The technique designed to steer current away from critical nodes during a SE is called sensitive node active charge cancellation (SNACC) [6]. A layout technique that mitigates SEEs implements charge sharing.

Differential Charge Cancellation (DCC)

Differential Charge Cancellation (DCC) combines the benefits of using differential inputs with the layout technique known as common-centroid. When designing circuits to be RH against SEEs it is important to note the most critical node in the circuit. That is, at which node in the circuit will a SEE cause the most damage. While this node depends on the circuit and design, we will focus on a differential pair input.

The benefits of using differential inputs (as opposed to using single ended) are well known [12], [15] and [20]. The use of differential inputs is preferred because of its high dynamic output range and its rejection of noise. Differential inputs remove any common perturbations (noise), referenced to the input terminals, fed to the output; assuming that the common-mode rejection ratio (CMRR) is high [12]. For a single ended amplifier, an input signal plus unwanted noise will appear at the output as an amplified version of both the signal and the unwanted noise. In the differential case, the unwanted noise will be common to both input terminals and the differential output will only see the amplified

differential input signals. The differential amplifier only amplifies the difference in the input signals so a common source of noise will be cancelled out during the difference of the two outputs see Figure 6.

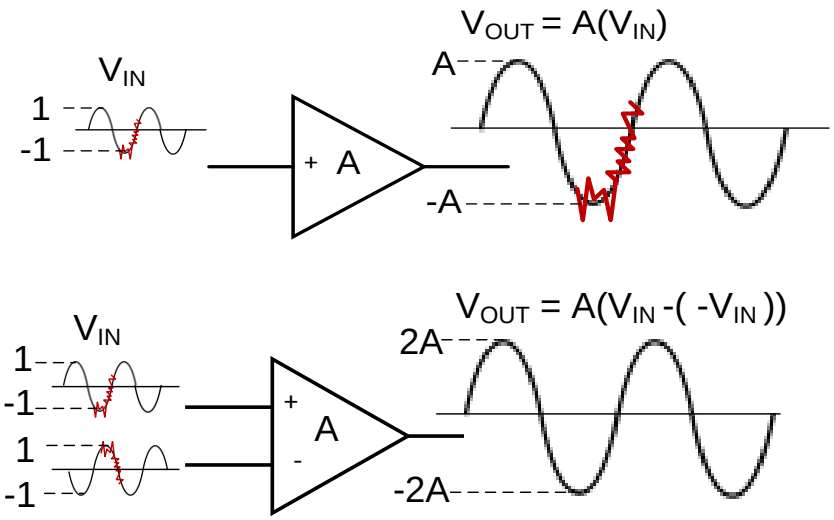
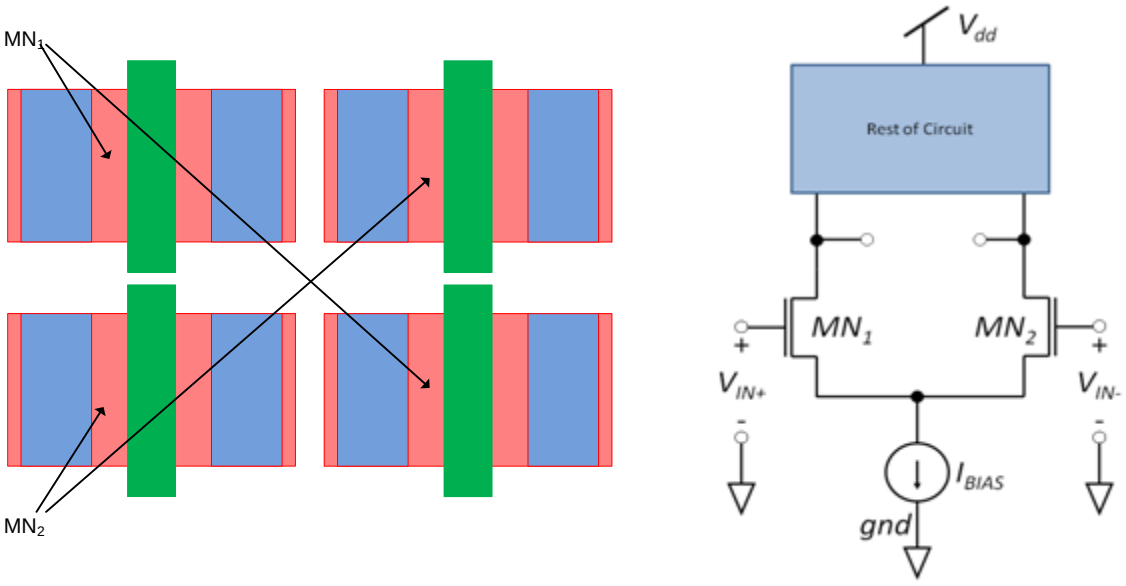


Figure 6: ***Benefits of Using Differential Signals***

In a differential pair, the two input transistors are made to be the same size; this is crucial to circuit operation. When fabricated for layout, however, the devices are subject to mismatch due to the gradients along the x and y-axis. To avoid this potential mismatch the transistors are laid out in a common-centroid configuration [15]. Common centroid splits up the differential pair transistors into multiple parallel combinations placed diagonally across from each other, see Figure 7.

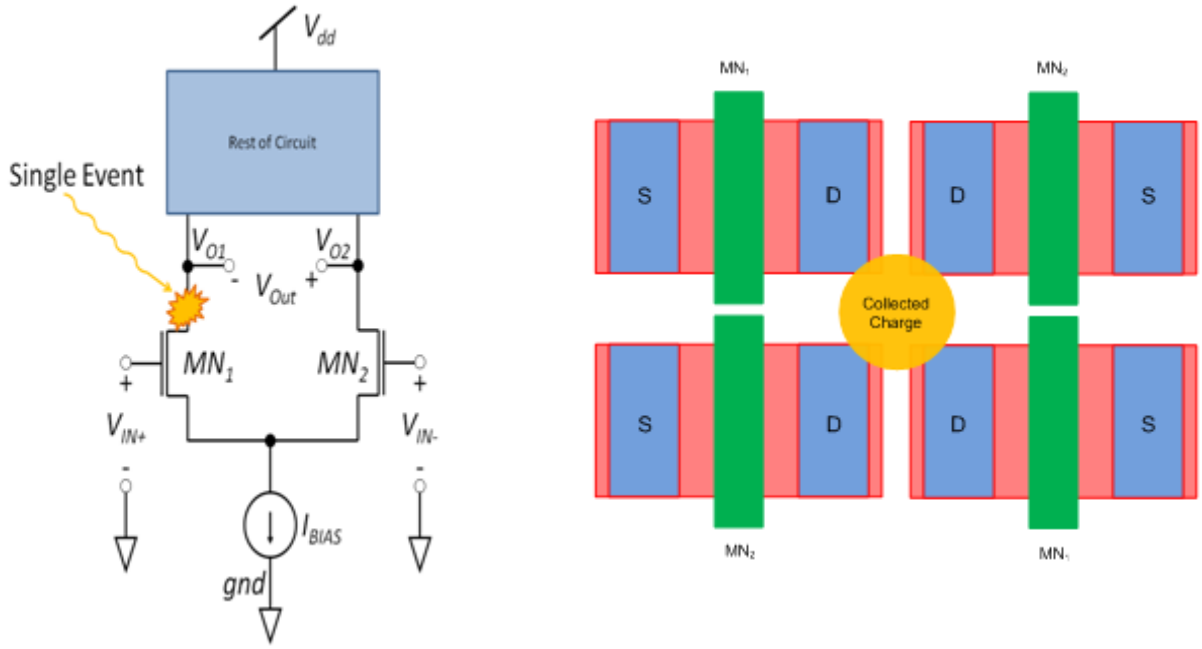


(a) (b)

Figure 7: (a) ***Common Centroid Configuration of Differential Pair and (b) Circuit***

Intertwining the input pair takes out the effects of the gradient to the first-order. DCC is in a sense very similar to the common-centroid layout technique; DCC utilizes transistors laid out in a similar fashion but to a different end.

Common-centroid utilizes layout configurations to ensure optimally matched devices. Common-centroid is not limited to common source topology, but will be depicted this way to illustrate the concept. The use of a differential pair eliminates the effects of unwanted noise riding on the input signal as well as perturbations from the ground on their shared source terminal, but it does not protect against perturbations on the drain. Consider the circuit in Figure 8 (a), if there was a SE strike that occurred on the drain of transistor MN_1 there would be a perturbation in the left branch of the differential pair which would produce a corrupted output signal. DCC brings the drains of sensitive nodes as close together as possible (permitted by design rules) see Figure 8 (b).



(a) (b)

Figure 8: ***Differential Charge Cancellation Layout Technique (a) Circuit and (b) Physical Layout***

Because feature sizes of transistors are becoming increasingly small, the amount of collected charge can affect multiple devices. The drains of sensitive devices are brought as close as possible to each other; because of the close proximity of the drains, DCC is also known as drain-proximity common centroid. Like SNACC, DCC will become more effective with decreasing device dimensions.

Sensitive Node Active Charge Cancellation (SNACC)

SNACC is a circuit topology used to mitigate SETs at sensitive nodes of analog circuits. In Figure 9, a current generator has been implemented with SNACC. The most sensitive node, node X, in this circuit is the drains shared by MN_2 and MP_2.

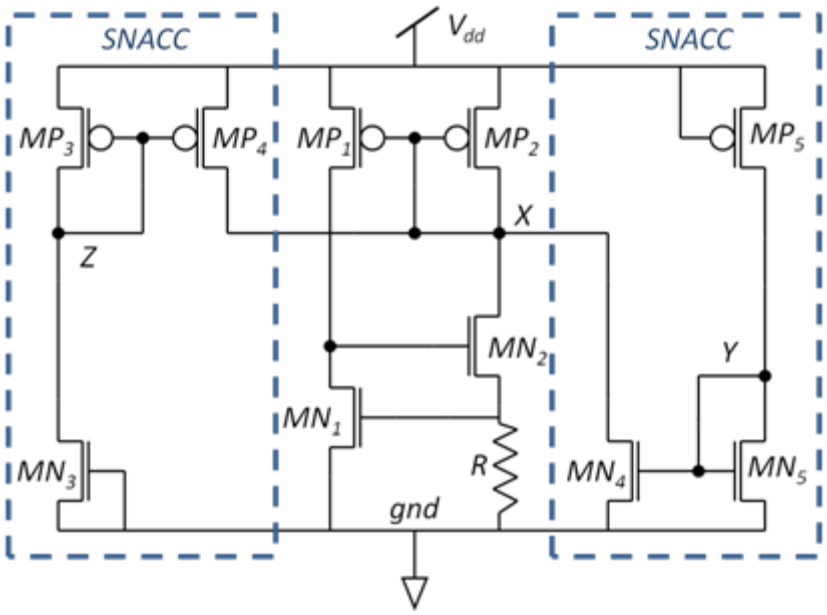


Figure 9: ***A Current Bias Generator with SNACC added to the Sensitive Node (Drain of MP2 and MN2) [6]***

To implement SNACC is it is important to layout specific transistors in an unconventional way. First, the transistors MN_3 and MP_5 are broken up into parallel combinations. One of MP_5's unit cells is placed in close proximity to MP_4 and another with MP_2. In a similar fashion, MN_3 is intertwined w MN_2 and MN_4 [6]. Due to the circuit configuration, the drain of both MP_5's unit-cells is in close proximity to the sensitive node X. In a similar fashion the drain of both MN_3's unit-cells is in close proximity to the sensitive node X near MN_2.

If a SE were to occur within MP_2 or MN_2 at node X it could give rise to a SET within the current generator. The SNACC circuitry sees the excess amount of charge from the SE and would be collected by either MN_3 or MP_5. If a SE were to occur within MN_2 or MN_4 then MN_3 would collect the charge and if a SE were to occur within MP_2 or MP_4 then MP_5 would collect the charge. The layout of one section of the SNACC topology can be, see Figure 10.

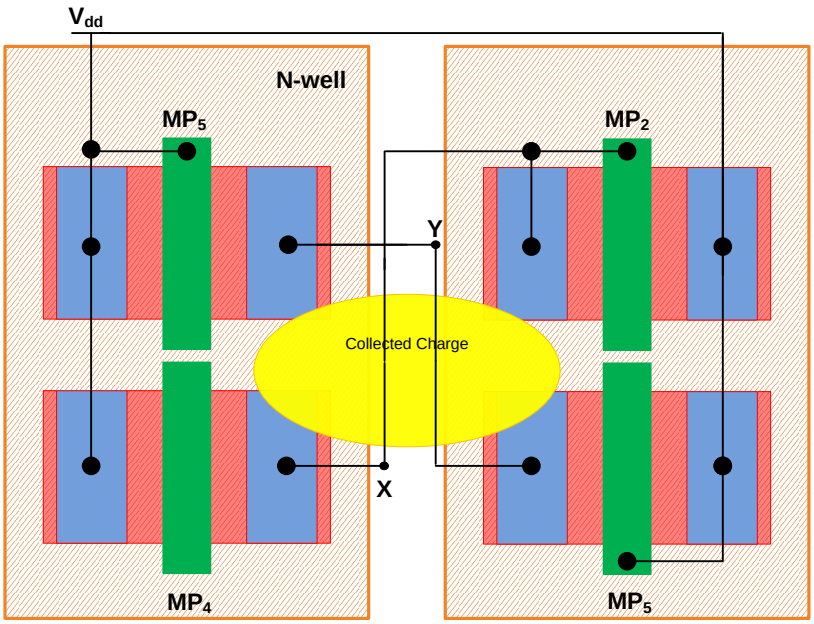


Figure 10: ***Layout Technique Utilized in SNACC Evenly Distributes the Collected Charge to Node Y***

Let us assume that a SE were to occur within the drain of MP_2 (node Y) as depicted in the figure above. An increase in charge, ΔQ, gives rise to an excess voltage at node Y, where $\Delta V_Y = \Delta Q/C$. This excess charge will be shared by the drain of MP_5 and produce a current that will sink into MN_5; ideally any excess charge seen at node X will be sunk by MN_4 because MN_4/MN_5 form a current mirror. The same conclusions can be drawn using MN_3 in place of MP_5 and MP_3/MP_4 for the current mirror MN_4/MN_5 if there is a SE within the drain of MN_2.

The source and gate are shorted for MN_3 and MP_5; they are ideally off and sink/source no current into the diode connected MP_3 or MN_5. So under normal operation little quiescent current is added to the circuit which is one benefit of this circuit topology. Adversely the SNACC circuitry does take up more die area. This technique has been shown to work and can be easily implemented at any

sensitive node. This technique will become more effective as devices become smaller and denser allowing more charge sharing to occur [6]. SNACC was implemented in an amplifier and an 8-bit DAC and was shown to reduce the average LSB error rate by one third as compared to the unhardened design [7]. SNACC is one example of using a circuit level technique to mitigate SEEs. Both a circuit topology technique and a layout technique for the mitigation of SEE have been discussed.

2.2.2 Design Techniques for the Mitigation of TID Effects

TID is less sporadic than SEs and because of this circuit topologies are generally not used to prevent TID damage. RH design techniques for TID mitigation are typically on the device level. As previously mentioned, the field oxide in STI connects the two diffusion regions of NMOS devices forming a parasitic FET. The field oxide fills in around the NMOS device including under the gate overlap (see Figure 11) and forms the parasitic FET with a parasitic gate oxide orders of magnitude larger than the actual gates oxide. This parasitic FET is the primary contributor to TID damage in NMOS devices.

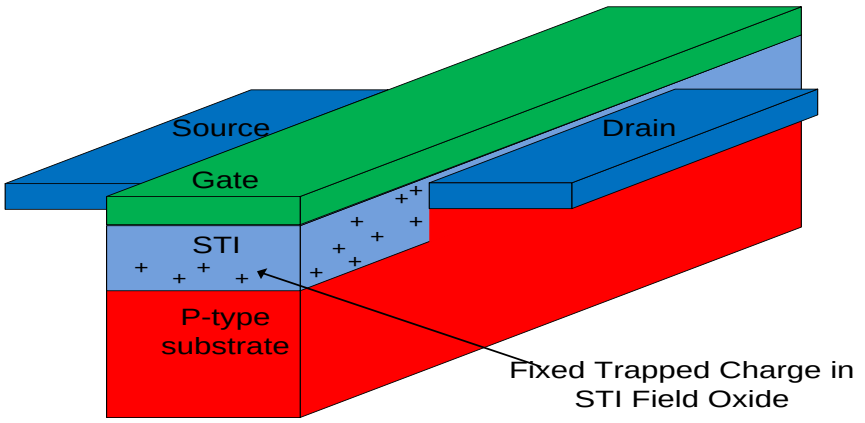


Figure 11: ***Formation of Parasitic FETs around NMOS Due to Gate Overlap and STI [24]***

The various mechanisms that make TID problematic can be obviated with edgeless transistors, otherwise known as ELTs (see Figure 12). The reduction in gate oxide thickness in newer technologies (<4.5nm in .18µm CMOS) has made the gate oxide less susceptible to TID; however, the field oxide used in STI is much thicker than the gate oxide and contributes to most problems found from TID. Through the use of ELTs one can mitigate the deleterious effects from TID.

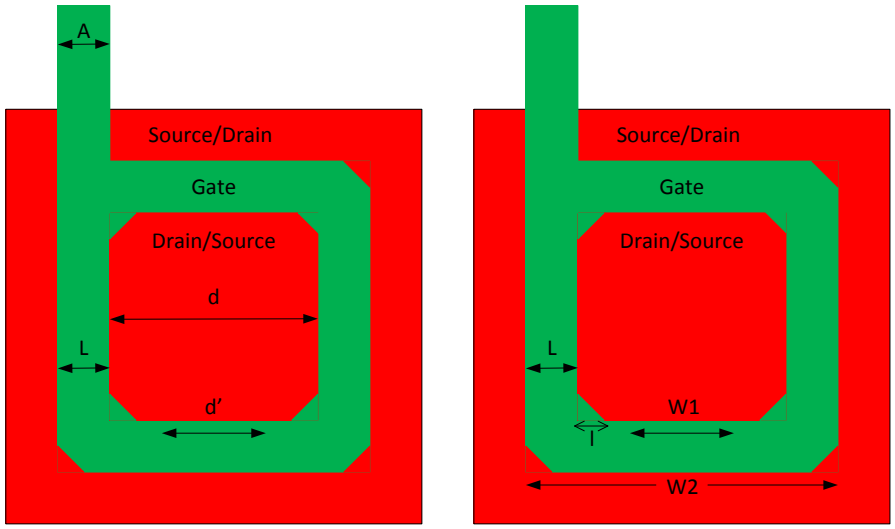


Figure 12: ***(a) Enclosed layout transistors with variables used in Eqn. 2, and (b) variables used in Eqn. 3 with n = 4.***

ELTs can be found in references [5]-[10], the effective aspect ratio is given by the following equation. Due to how this equation was derived it is only valid when $d' > 2\alpha L_{eff}$.

$$\left(\frac{W}{L}\right)_{eff} = 4\frac{2\alpha}{ln\frac{d'}{d'-2\alpha L_{eff}}} + K\frac{1-\alpha}{\frac{1}{2}ln(\frac{1}{\alpha})\sqrt{\alpha^2+2\alpha+5)}} + 3\frac{\frac{d-d'}{2}}{L_{eff}} \qquad (2)$$

K is a parameter related to width of the elongated section of polycrystalline silicon and is given by K = 8 – A/L. The variable α (approximately .05) is a parameter relating the border of the transistor

represented by the first and second term and L_{eff} is the effective channel length of the device. This equation breaks the ELTs poly region into three different "gates" and this is why there are three terms in Eq.(2). Eq. (2) is derived from the three transistor model used to break up the annular gate into sections more information can be found in [16]. There is another equation found in literature that states accurate modeling for devices n-sided polygon ELTs with higher channel lengths [4].

The derivation assumed the classic long-channel (gradual channel approximation) model and that the carrier mobility was uniform throughout the device [4]. The charge density along the length of the channel was found and can be seen in Eq. (3).

$$Q_d = C_{OX} 2x \tan\left(\frac{\pi}{n}\right)(V_{GS} - V_{thn} - V(x)) \tag{3}$$

The drift current is given by Eq. (4).

$$I = \mu Q_d \frac{dV(x)}{dx} \tag{4}$$

Equating both Eq. (3) and (4) and grouping like terms results in a separable differential equation. Integrating both sides results in Eq. (5).

$$\int_{w1}^{w2} \frac{I}{2x} dx = \int_0^{V_{DS}} \mu C_{OX} \tan\left(\frac{\pi}{n}\right)(V_{GS} - V_{thn} - V(x))\, dV(x) \tag{5}$$

Solving for the drain current results in Eq. (6); however this equation only represents the current in one side of the n-sided polygon. The final result can be seen in Eq. (7).

$$I = \mu C_{OX} \frac{2tan(\frac{\pi}{n})}{ln(\frac{w2}{w1})}[(V_{GS} - V_{thn})V_{DS} - \frac{V_{DS}^2}{2})] \quad (6)$$

$$I_d = nI = \mu C_{OX} 2n \frac{tan(\frac{\pi}{n})}{ln(\frac{w2}{w1})}[(V_{GS} - V_{thn})V_{DS} - \frac{V_{DS}^2}{2})] \quad (7)$$

This equation is very similar to the classic straight gate transistor; the only difference is the effective aspect ratio is now different. The effective aspect ratio for an n-sided ELT can be seen in Eq. (8).

$$\left(\frac{W}{L}\right)_{eff} = 2n \frac{tan\,(\alpha)}{ln\frac{w2}{w1}} \quad (8)$$

Where n is the number of sides of the ELT and α = π/n. Eq. (8) can also be used for polygonal shapes that are not limited to squares like Eq. (2). Both analog and digital IC design can benefit from these equations. A full derivation of Eq. (8) has been derived in full detail in [4].

Research and experimentation have been performed to observe the benefit of having enclosed drain versus enclosed source of ELTs. One clear benefit of having enclosed source of the devices is charge sharing can be implemented. Enclosed source also reduces the channel length modulation error. It was noted that due to the asymmetry of the ELT enclosed drain devices have higher output

conductance [16]. Other benefits of enclosed drain vs. enclosed source can be found [5], [10], and [16]. These papers have both simulated and experimental data and should be read for further insight.

While the previously mentioned techniques can decrease susceptibility to ionizing radiation, there are also downsides to using RHBD techniques. Some techniques used for RHBD including (ELTs, and SNACC) take up more die area. In most cases, using these techniques inherently increases power consumption. More research can be done to ensure accurate modeling of novel layout techniques and validation of existing equations that predict aspect ratios. The validity of Eq. **(2)** and **(8)** will be examined in greater detail in future work (preliminary analysis has been conducted and can be seen in the Appendix. Some questions that will hopefully be answered are which equation truly represents the effective aspect ratio of an ELT and is one equation more accurate for certain channel lengths.

Conclusion

Electronics exposed to the natural radiation environment are susceptible to device degradation from mechanisms not experienced by terrestrial electronics. Ionizing radiation can degrade DC performance in PMOS and NMOS devices and potentially irreparable damage to the device/circuit/system. Design engineers have implemented layout techniques such as ELTs to decrease the susceptibility to TID and circuit topologies to handle unwanted excess current. This section has introduced the causes and effects of ionizing radiation in modern semiconductor devices and techniques used to mitigate these effects.

3.0 Voltage References

Some of the effects of radiation damage were described in the previous section and designing analog ICs becomes more challenging when radiation effects need to be considered. The purpose of this work was to produce a RHBD voltage reference using a standard-bulk CMOS process. The following section will detail some common voltage references and then introduce the voltage reference designed for this research.

3.1 Voltage Reference Topologies

3.1.1 Zener Diode Based Regulators

Zener diodes have seen extensive use in voltage reference topology for many decades. A Zener diode behaves similarly to that of a normal diode; the IV characteristic of a Zener diode can be seen below in Figure 13.

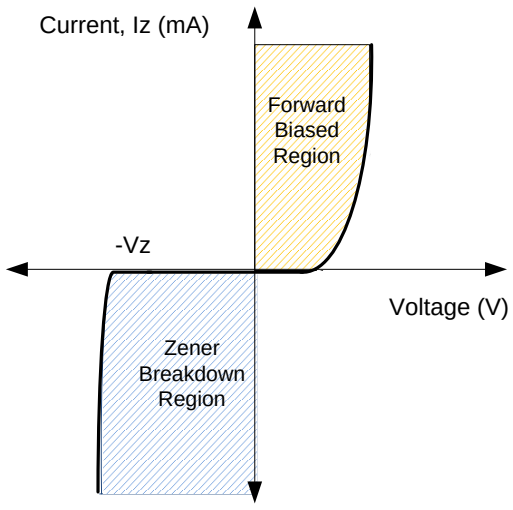


Figure 13: ***IV Characteristic of Zener Diode***

In a pn junction under reverse bias, the anode is connected to a lower potential than the cathode. In reverse bias the depletion region is widened on both sides. As a more positive voltage is connected to the cathode more electrons are attracted away from the metallurgical junction; similarly a negative voltage at the anode will attract holes away from the metallurgical junction. An increasing number of ionized donors, present at the depletion region, cause an increase in the electric field. When this field reaches a certain threshold it breaks some of the covalent bonds of the semiconductor atoms [23]. This introduces more unbound minority carriers which add to current.

A Zener diode as a reference is an example of a two-terminal shunt reference. When a supply current is provided across a resistor and the break down voltage of the Zener diode is exceeded, a stable reference is achieved. The output voltage is typically connected to a load in parallel hence the name shunt reference see Figure 14.

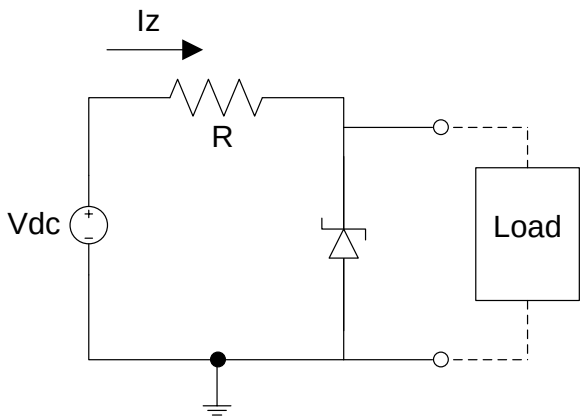


Figure 14: ***Biasing a Zener diode reference***

All diodes have a breakdown voltage; but a Zener diode has a breakdown voltage *and* still functions as a diode without much destruction caused to the device. Once the breakdown voltage is reached the Zener diode will conduct current through it and will have a fairly constant voltage drop

across it over a wide range of temperature and currents. Unlike a forward diode voltage drop which is approximately 600 mV a Zener diode's breakdown voltage occurs at odd intervals (2.7V,3.3V,5.2V ,6.2V etc.).

Zener diodes are discrete components, but there is a type of Zener that is manufactured with n and p regions on silicon. These are known as Buried Zener diodes. Buried Zener diode references are popular because they: eliminate surface noise, have a less temperature drift as compared to the Zener, prolonged stability, and excellent accuracy. A few reasons why Buried Zener references are undesirable: they require high supply voltages and they are more costly than standalone Zener diodes [23]. Another pitfall to the use of Buried Zener diodes is that they are not available in standard CMOS technologies. They also require greater supply voltage and this is undesirable for low power application. There is another option to using Zener and Buried Zener references.

3.1.2 Bandgap References

We have discussed a shunt type reference (Zener). A Bandgap references is a series type reference and is a popular choice for a voltage reference. Unlike Zener references Bandgap references are implemented using bipolar junction transistors; they can be used for low power applications and do not require a high voltage source. The output reference voltage can be varied with a Bandgap reference in contrast to discrete values in a Zener references. The cornerstone of the Bandgap reference is its ability to exhibit both an inverse and direct relationship to temperature using the characteristics of bipolar junction transistors (BJT).

A BJT can be characterized as a current controlled current source. The collector current, I_C, is given by Eq. (9).

$$I_C = I_S e^{\frac{V_{BE}}{kT/q}} \quad (9)$$

Where k is Boltzmann's constant, q is the unit of electric charge, V_{BE} is the base emitter voltage, and T is temperature. A small current into the base, I_B, of the transistor produces an amplified current, I_C. If a BJT is connected with its base and collector tied together it acts as a diode. If a diode connected transistor is supplied with a constant current it should have a constant V_{BE}; however this is not the case with changes in temperature.

With a constant current the diode-connected transistor's V_{BE} has a temperature dependency of approximately -2 (mV/°C) for a given temperature. A parameter that decreases with increasing temperature is said to be complimentary to absolute temperature (CTAT). If one added V_{BE} (CTAT) with another voltage that has the opposite temperature dependence, say α (mV/°C) where α>0, then theoretically one could construct a new voltage, V_{REF}, which would be more thermally stable over a range of temperatures.

The aforementioned variable, α, is proportional to absolute temperature (PTAT). The combination of PTAT and CTAT voltages is the cornerstone of the Bandgap reference. Consider the circuit shown below in Figure 15.

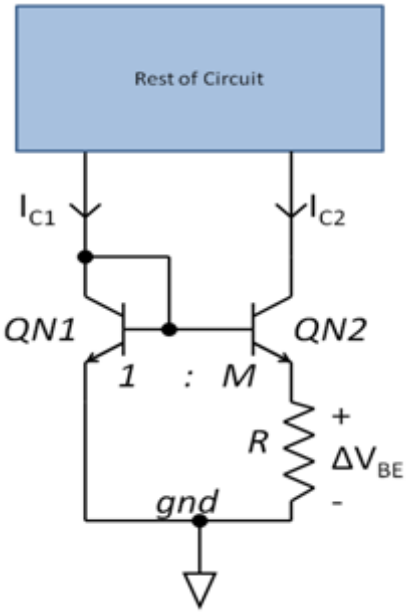


Figure 15: ***Realization of a PTAT Reference***

Doing KVL around the circuit yields equation Eq. (10).

$$\Delta V_{BE} = V_{BE1} - V_{BE2} \tag{10}$$

Using Eq. (9) and replacing the V_{BE} term Eq. (10) can be rewritten and yields Eq. (11).

$$\Delta V_{BE} = \frac{kT}{q} ln\left(\frac{I_{C1}}{I_{S1}}\right) - \frac{kT}{q} ln\left(\frac{I_{C2}}{I_{S2}}\right) \tag{11}$$

The collector currents, I_C, are made to be equal, but QN2 is much larger than QN1 by a factor M that is $I_{S2} = M \cdot I_{S1}$ then Eq. (11) can be reduced to Eq. (12).

$$\Delta V_{BE} = \frac{kT}{q} ln\left(\frac{I_{S2}}{I_{S1}}\right) = \frac{kT}{q} ln(M) \tag{12}$$

Using Eq. (12) and Ohm's Law we find that the collector current can be described by Eq. (13).

$$I_C = \frac{1}{R}\frac{kT}{q} ln(M) \tag{13}$$

We can see from Eq. (13) that it is possible to form a voltage/current that is PTAT using BJTs. Now the parameter $\alpha = \frac{k}{q}\ln(M)$ must be made to compensate for the CTAT behavior of V_{BE}.

The issue at hand is how to combine the CTAT and PTAT voltages into a stable output voltage V_{REF}. There are many ways to accomplish this [15] and [20] , one can be seen in Figure 16.

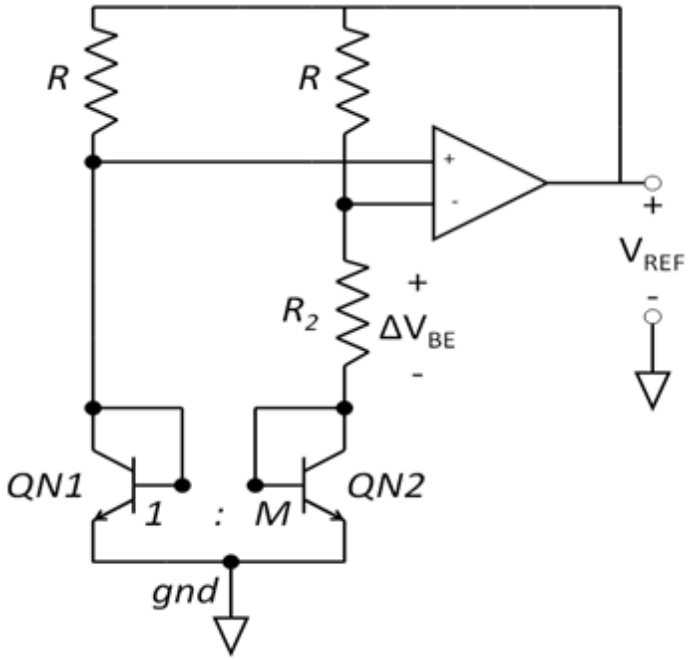


Figure 16: ***Realization of Bandgap Reference with an Operational Amplifier***

Performing KVL around the loop we can find that the V_{REF}, see Eq. (14).

$$V_{REF} = V_{BE2} + \Delta V_{BE}(1 + \frac{R}{R_2}) \tag{14}$$

Note that both V_{BE} and ΔV_{BE} are functions of temperature we may rewrite the equation Eq. (14) with V_{REF} as a function of temperature, see Eq (15).

$$V_{REF}(T) = V_{BE2}(T) + (1 + \frac{R}{R_2})\Delta V_{BE}(T) \quad (15)$$

As discussed previously, V_{BE} is CTAT while ΔV_{BE} is PTAT, this complimentary behavior can be exploited and provide a stable output voltage for a given temperature. Taking the derivate of both sides of Eq. (15) with respect to temperature yields Eq. (16).

$$\frac{dV_{REF}(T)}{dT} = \frac{dV_{BE2}(T)}{dT} + (1 + \frac{R}{R_2})\frac{d\Delta V_{BE}(T)}{dT} \quad (16)$$

Setting the derivate equal to zero provides insight into how the parameters M, R and R_2 must be sized to cancel out the effects of V_{BE2}, see Eq. (17).

$$\frac{dV_{REF}(T)}{dT} = 0 = -2 + (1 + \frac{R}{R_2})\frac{k}{q}ln(M) \quad (17)$$

From the Eq. (17) one can see that the resistances and sizing of QN2 can be chosen to cancel the changes of V_{BE2} over temperature. This is one example in which a thermally stable voltage reference can be designed using Bandgap reference. The derivation shown in Eq. (17) can be made go to zero for a given temperature, T_0, but in reality V_{BE} has both a linear and nonlinear component that has a small curvature over temperature. There are ways to compensate the curvature using advanced curvature compensation techniques [26] and [27].

BJT devices are susceptible to TID and SEEs just like CMOS devices but they are affected by another type of radiation omitted from the previous section (Section 2.1). Incident particles can cause both ionizing (TID) and non-ionizing damage (displacement damage). Non-ionizing particles can displace atoms in the lattice of the semiconductor material, resulting in new energy levels in the bandgap of the semiconductor. For minority carrier devices (such as BJTs) this can alter the electrical properties of the semiconductor [28]. The primary device parameters that are examined as functions of displacement damage are minority-carrier lifetime and DC current gain. Displacement damage can be caused by electrons, protons, as well as neutrons. Displacement damage was not discussed in Section 2.1 because CMOS devices are relatively unaffected by this type of radiation damage.

Displacement damage has been examined for different particles and at different energy levels for voltage references using Bandgap references and one Buried Zener reference [25]. The accuracy of the output reference voltages were evaluated for different fluences of protons (equivalent total dose) at different energy levels of incident particles. It was found that the Buried Zener reference was the least susceptible to radiation damage. Unlike the simpler Buried Zener reference, Bandgap references rely on second-order effects to produce the output voltage and displacement damage affected the accuracy of the voltage. The degradation in DC current gain is also explored [25].

3.2 Mutually Compensated Mobility/Threshold Voltage Reference

3.2.1 Motivation

This project looked into designing a voltage reference in a standard-bulk CMOS process. The Zener and Bandgap references were discussed in some detail in the previous section. While Buried Zener references have better noise performance compared to the Bandgap reference, Buried Zener diodes are unavailable in standard-bulk CMOS processes and are not suitable to low voltage applications. While the Bandgap reference remains an adequate choice as a voltage reference they are more susceptible to radiation damage compared to CMOS and Buried Zener diodes. It will be shown that there is an alternative to using Bandgap references (utilizing BJTs) and the Buried Zener reference. The alternative can be fabricated in a standard-bulk CMOS process implementing only CMOS.

It has been noted in several references that there exists a way to compensate for the degradation of mobility and threshold voltage as functions of temperature; this relationship has been investigated with NMOS devices [17], [18], and [19]. The mobility of a NMOS device, μ_n, decreases with increasing temperature and threshold voltage, V_{thn}, also decreases with increasing temperature [15]. This relationship can be exploited recognizing that while each parameter decreases with temperature, the decrease has different effects on the drain current (or gate source voltage) of a diode connected MOS device.

3.2.2 Design to Cancel Effects of Mobility and Threshold Voltage

Consider an NMOS operating in saturation (as a diode connected FET). If a constant current source I_D is supplied then there will be a constant voltage drop, V_{GS} or V_{DS}, across the device see Figure 17.

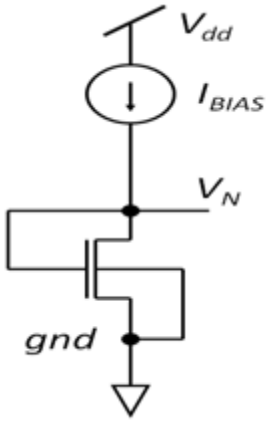


Figure 17: ***Diode Connected NMOS with a Constant Current Source***

The drain current, I_D, for a saturated NMOS is given in Eq. (18).

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{thn})^2(1 + \lambda V_{DS}) \tag{18}$$

Assuming that the channel length modulation error is small ($\lambda V_{DS} \ll 1$) Eq. (18) can be simplified. Rearranging Eq. (18) one can find a simplified expression for V_{GS} (Eq. (19)).

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox} Z}} + V_{thn} \tag{19}$$

Where Z = (W/L) is the aspect ratio. Mentioned previously both mobility and threshold voltage vary as functions of temperature. The relationship between the mobility of a NMOS and temperature can be seen in Eq. (20).

$$\mu_n(T) = \mu_{n0}\left(\frac{T}{T_0}\right)^{\alpha_\mu} \tag{20}$$

The relationship between threshold voltage and temperature can be seen in Eq. (21). Both α_μ and α_{vth} (V/°C) are negative quantities.

$$V_{thn}(T) = V_{thn0} + \alpha_{vth}(T - T_0) \tag{21}$$

A good voltage reference is thermally stable over a wide range of temperature it is important to view how the voltage changes as a function of temperature. V_{GS} can be rewritten as a function of temperature with parameters mobility and threshold (see Eq. (22)).

$$V_{GS}(T) = \frac{\chi}{\sqrt{\mu_n(T)}} + V_{thn}(T) \tag{22}$$

Where $\chi = \sqrt{\frac{2I_D}{C_{ox}Z}}$. The beneficial relationship between changes in mobility and threshold can now be seen more clearly. While both, mobility and threshold decrease as functions of temperature, they affect V_{GS} in different ways. With increasing temperature, V_{GS} will decrease due to the threshold voltage component and increase due to the changes in mobility. One can draw a parallel between the complimentary and proportional (CTAT and PTAT) behaviors found in Bandgap references. The change in V_{GS} due to: mobility is PTAT and V_{thn} is CTAT.

In a similar way that the Bandgap reference was designed, differentiating V_{GS} with respect to temperature and setting it equal to zero for a given temperature T_0 yields Eq. (23).

$$\frac{dV_{GS}(T)}{dT}\Big|_{T=T_0} = \frac{dV_{thn}(T_0)}{dT} - \frac{\chi}{2}\frac{\frac{d\mu_n(T_0)}{dT}}{\mu_n(T_0)^{3/2}} = 0 \tag{23}$$

Solving for χ yields Eq. (24).

$$\chi = 2\frac{\alpha_{vth}}{\alpha_\mu}T_0\sqrt{\mu_{n0}} \tag{24}$$

Solving for an optimum aspect ratio, Z_{OPT}, yields Eq. (25). For a given drain current, I_D, it is possible to define an output voltage whose derivative is zero at a given temperature, T_0. That is to say, the effects of mobility and threshold voltage on V_{GS} will cancel at T_0 resulting in thermally stable voltage reference.

$$Z_{OPT} = \frac{I_D\alpha_\mu^2}{2C_{ox}\alpha_{vth}^2T_0^2\mu_{n0}} \tag{25}$$

The different design and model parameters are known and can be seen in the table below.

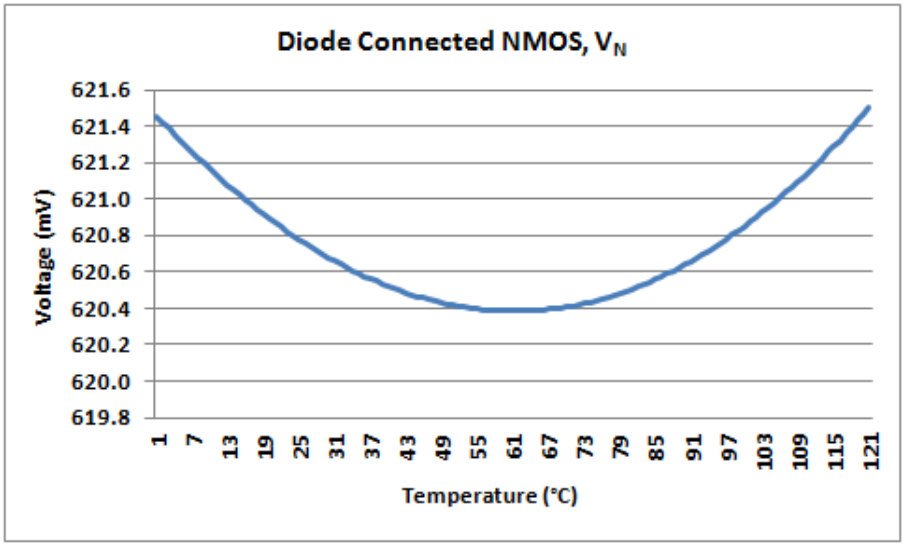
Table 1: ***Model Parameters (CMRF7SF) and Design Parameters Chosen for Optimum Aspect Ratio, Z_{OPT}***

I_D	100 (μA)
C_{OX}	7.76E-3 (F/m^2)
α_μ	-1.93
α_{vthn}	-1 (mV/°C)
μ_{no}	41.02E-3 ($m^2/(V{\cdot}s)$)

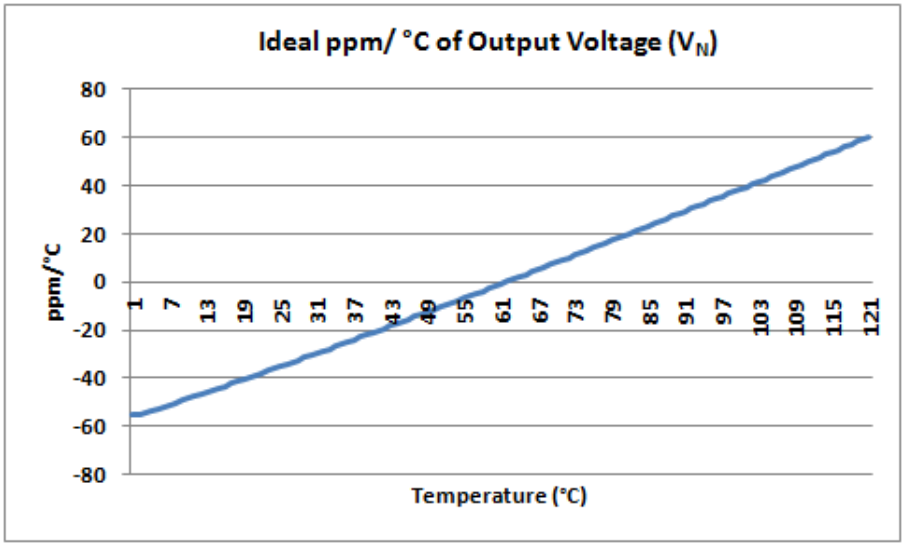
The optimum aspect ratio was found from these to be approximately Z_{OPT} = 6.6, however after simulation the value was changed to Z_{OPT} = 8.8. The NMOS devices were made up of four unit cells each had an effective aspect ratio Z = 2.2. Dividing the NMOS devices into multiples allowed common

centroid to be implemented. The channel length was chosen to be large to minimize the channel length modulation error.

Using Eq. (25) with T_0 = 60°C and Z_{OPT} = 2.2 and the values from Table 1 above, the output of a diode connected NMOS with a constant current source, as shown in Figure 17, can be seen in Figure 18.



(a)



(b)

Figure 18: ***(a) V_{GS} for Diode Connected NMOS versus Temperature and (b) V_{GS} in ppm/°C***

Looking at Figure 18 (a) the output voltage, V_N is almost parabolic and is concave up. If the current is held constant, V_{GS} must oppose the changes of mobility and threshold. In the left half of the curve V_{GS} is decreasing and in the right half V_{GS} is increasing. This is easily explained. As the threshold voltage drops V_{GS} must decrease to keep the current constant. Similarly, as the mobility decreases, V_{GS} must increase to counteract this change. The minimum of V_N is seen where the effects of mobility and threshold cancel at temperature, T_0. This thermal sweep was over a wide range of temperatures (0°C ≤ T ≤ 125°C). It will be shown later that the minimum of V_N can be changed.

Figure 18 (b) shows the accuracy V_N in ppm/°C (where ppm is parts per million) over the temperature range. This was calculated by finding the difference between two successive voltage points and normalizing the change with respect to the first voltage, dividing by the change in temperature, and multiplying by 10^6 (ppm/°C $= \left(\frac{V_x - V_{x-1}}{V_{x-1}}\right)\frac{10^6}{\Delta T}$). We can see that this is fairly symmetric about T_0. The output of a standalone NMOS is an acceptable type of shunt voltage reference by itself. Simulation does confirm theory; there is a temperature where the changes in mobility and threshold effectively cancel. This has been showcased in previous work by others [17], [18], and [19]. A method will be proposed to take the standalone NMOS and improve its accuracy by an order of magnitude. A similar analysis can be carried out for a PMOS device.

Starting in a similar fashion deriving the optimum aspect ratio for an NMOS, Z_{OPT}, we have the drain current equation for a PMOS operating in saturation Eq. (26)

$$I_{SD} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{thp})^2 \tag{26}$$

Note, the current for a PMOS flows from source to drain; it is almost identical in form to the NMOS except that V_{thp} is a negative number. Eq. (26) can be rewritten in terms of the V_{SG}; this is done because the output of the PMOS will be referenced from source to ground.

$$V_{SG} = -V_{GS} = -(\frac{\chi_P}{\sqrt{\mu_p(T)}} + V_{thp}(T)) \tag{27}$$

Where $\chi_P = \sqrt{\frac{2I_S}{C_{ox}Z}}$ and V_{thp} is negative for PMOS devices. V_{thp} decreases in magnitude (in reality it is becoming more positive) with increasing temperature. This is denoted by subtracting the changes due to temperature from the initial threshold voltage; this is consistent with the value of α_{vth} ($\alpha_{vth} < 0$) used in the NMOS analysis.

$$V_{thp}(T) = V_{thp0} - \alpha_{vth}(T - T_0) \tag{28}$$

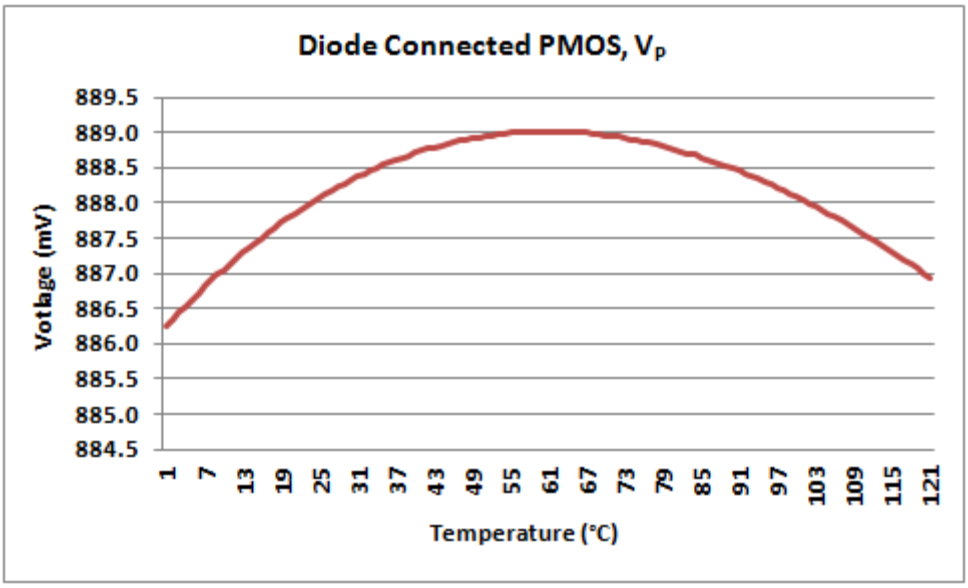
The same analysis can be performed to find at which temperature, T_{0P}, is the change in source gate voltage equal to zero. Solving for χ_P, in Eq. (29), there is sign change from the original derivation of χ; the absolute value of χ_P is shown below.

$$|\chi_P| = 2\frac{\alpha_{vth}}{\alpha_\mu}T_{0P}\sqrt{\mu_{p0}} \tag{29}$$

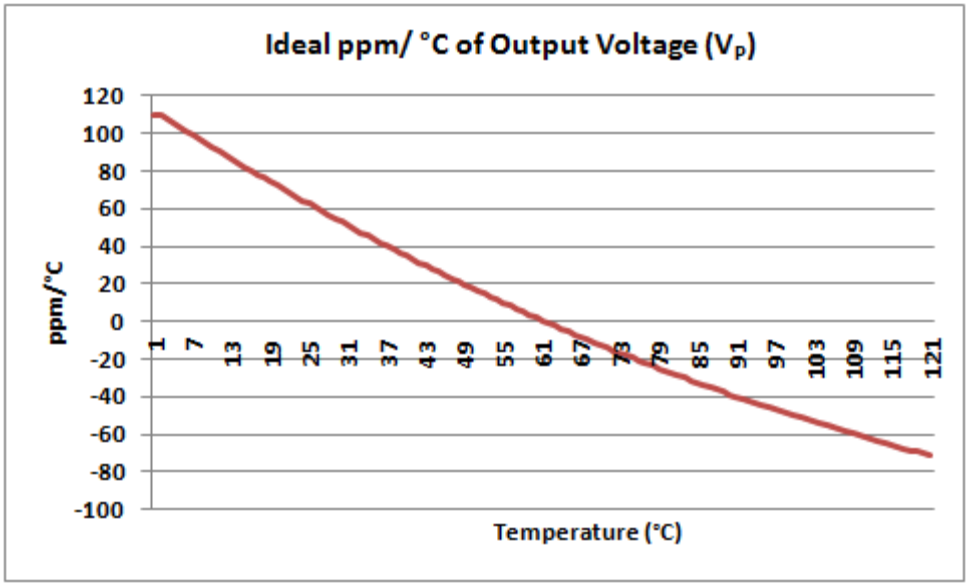
The value of Z_{OPT} for the PMOS can be seen in Eq. (30) and is very similar to that of the NMOS.

$$Z_{OPTP} = \frac{I_S\alpha_\mu^2}{2C_{ox}\alpha_{vth}^2T_0^2\mu_{p0}} \tag{30}$$

The results are fairly alike with one difference. Supplied by a constant current, the output of a diode connected PMOS, V_P, has a temperature, T_0, at which the effects of mobility and threshold voltage cancel it is also fairly parabolic versus temperature, see Figure 19.



(a)



(b)

Figure 19: ***(a) V_{SG} for Diode Connected PMOS versus Temperature and (b) V_{SG} in ppm/°C***

From Figure 19 (b), it can be seen that ppm/°C plot is fairly linear like that seen in the NMOS; however its slope is opposite in magnitude. The plot of V_N (Figure 18 (a)) is initially CTAT, crosses its minimum, and then becomes PTAT. The plot of V_P (Figure 19(a)) is initially PTAT, crosses its maximum, and then becomes CTAT. The two output voltages complement each other (V_N is concave up and V_P is concave down). While done only in post-processing the two output voltages, V_N and V_P, can be combined linearly to produce a new thermally stable output voltage, V_{REF}. V_{REF} has a higher accuracy than either the diode connected NMOS or PMOS by themselves. An example of how to linearly combine the two output voltages can be seen in Figure 20. It was not implemented for this project; all linearly combinations were performed post-processing.

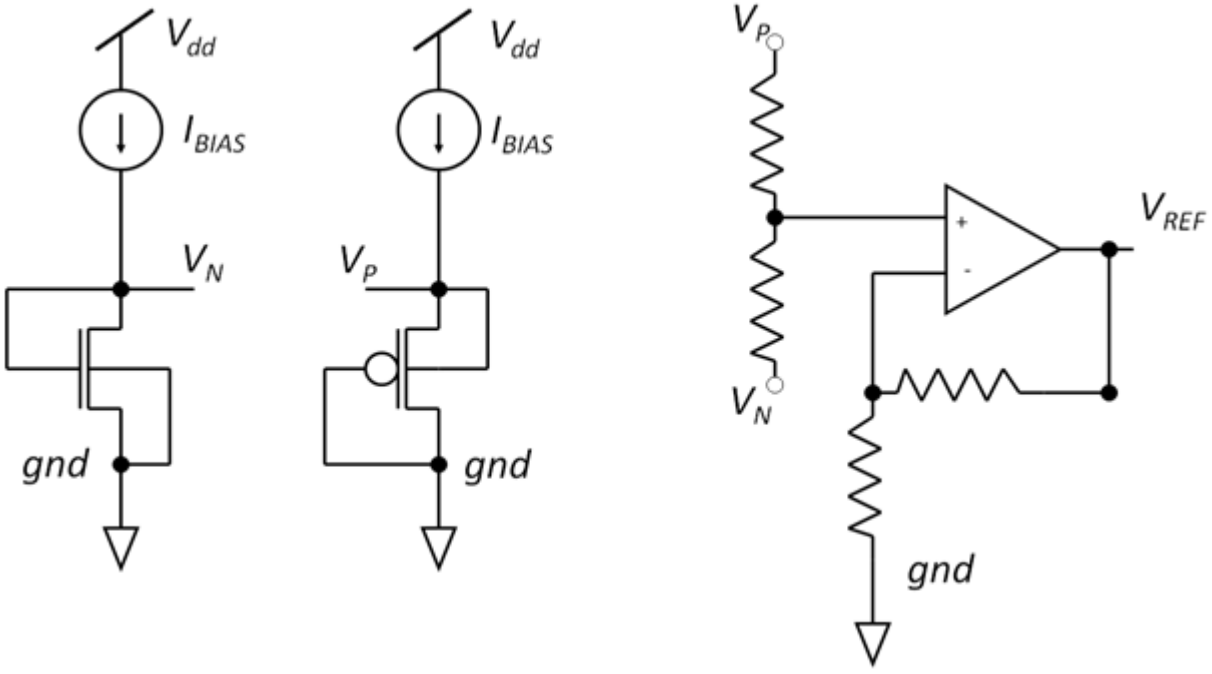
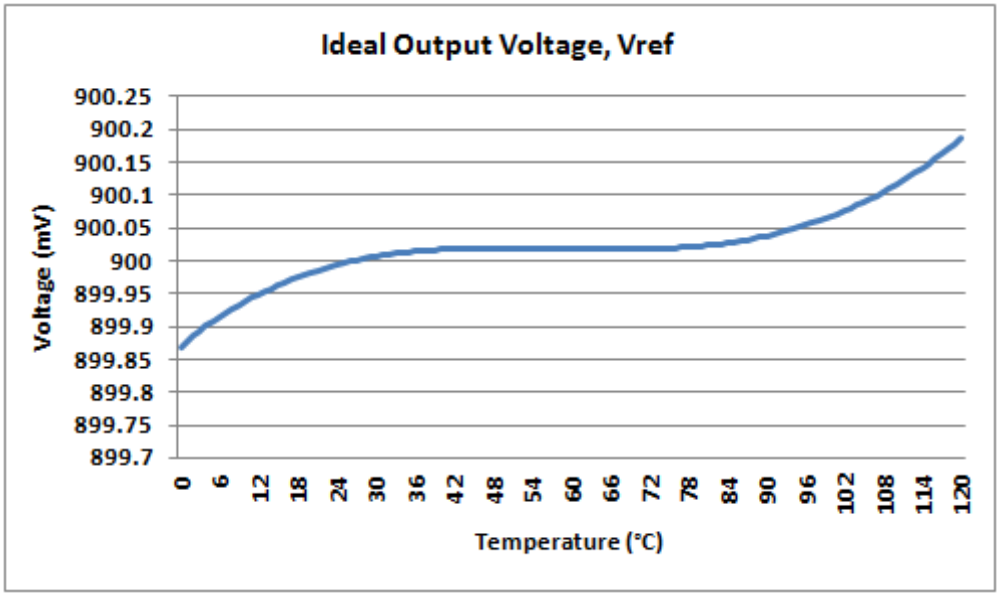
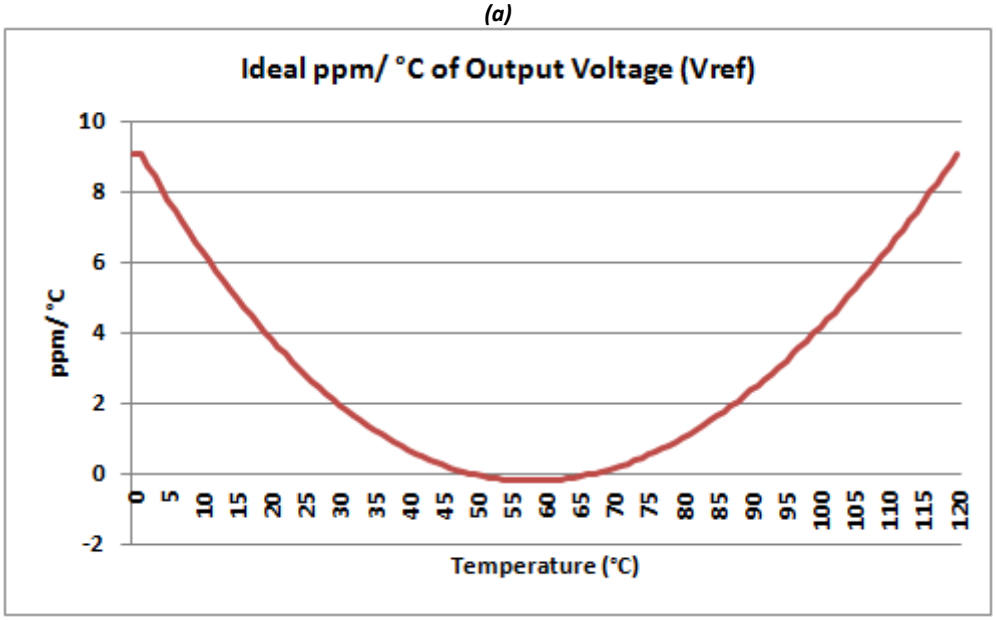


Figure 20: ***Technique to Linear Combine of V_N and V_P***

Due to the complementary nature of the thermal profiles' of the NMOS and PMOS devices the output voltage V_{REF} has a lower deviation from its mean around T_0 and across the temperature range. V_{REF} also has a lower ppm/°C behavior than either of its two components alone. The output of the linearly combined voltages, V_N and V_P can be seen in Figure 21.



(a)



(b)

Figure 21*: (a) V_{REF} versus Temperature and (b) V_{REF} in ppm/°C*

While the cancellation of mobility and threshold voltage for a diode connected MOS has been well documented ([16]-[19]), this work implemented individually tunable NMOS and PMOS mutually compensated mobility and threshold voltage technique using external bias resistances. The following section will describe the voltage reference circuit used to produce the output voltage V_N and V_P. The complimentary thermal behavior of a PMOS and NMOS will form the foundation for a thermally stable voltage reference.

3.2.3 Realization of a Mutually Compensated Mobility/Threshold Voltage Reference

A mutually compensated mobility/threshold voltage reference was designed from the different thermal profiles of a NMOS and PMOS field-effect transistors can be seen in Figure 22. The circuit is symmetrical from left to right with the exception that the output stages are a NMOS and a PMOS. The output voltages V_N and V_P are the two components needed to produce a stable voltage V_{REF}. The device sizes for NMOS and PMOS devices can be seen in Table 2.

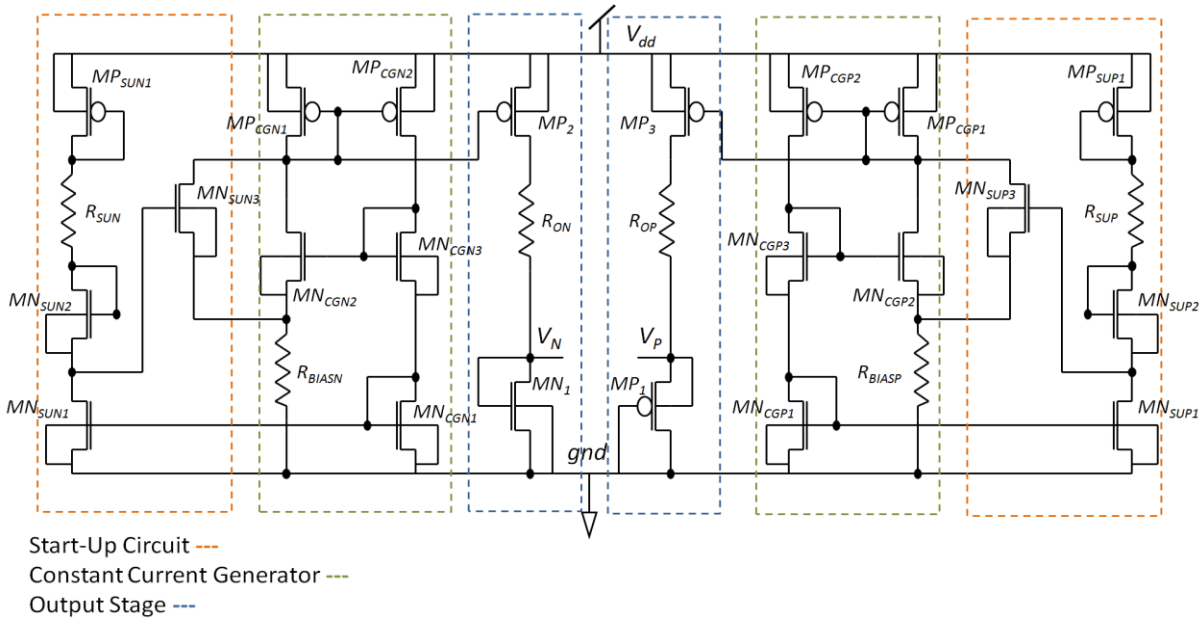


Figure 22: ***Proposed Voltage Reference***

Table 2: ***Aspect Ratios and Multipliers for MOS Devices used in Reference Design***

Device Name	Aspect Ratio (multiplier)
MN_{SUN1}, MN_{SUN2}, MN_{SUN3}, MN_{SUP1}, MN_{SUP2}, MN_{SUP3}	26.4/12.0 (m =1)
MP_{SUN1}, MP_{SUP1}, MP_2, MP_3	29.0/10.0 (m = 10)
MN_{CGN1}, MN_{CGN2}, MN_{CGN3}, MN_{CGP1}, MN_{CGP2}, MN_{CGP3}, MN_1	26.4/12.0 (m =4)
MP_{CGN1}, MP_{CGN2}, MP_{CGP1}, MP_{CGP2}	29.0/10.0 (m = 40)
MP_1	21.36/10.0 (m =8)

As shown in Section 3.2.2, a constant current source is needed to implement mobility/threshold voltage cancellation at a given temperature. An ideal current source was needed to supply to the diode connected NMOS and PMOS. A constant current generator was designed see Figure 23.

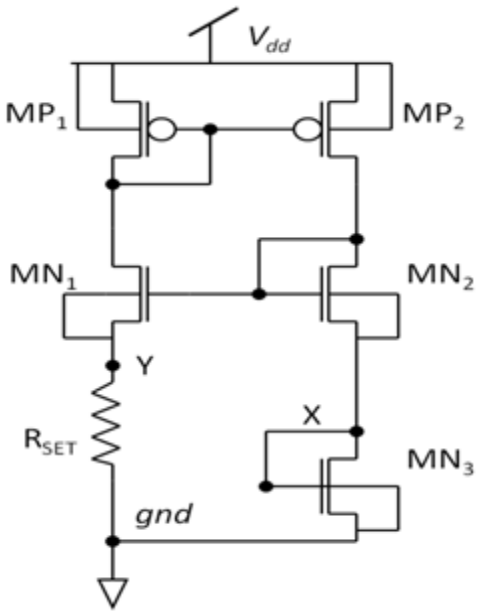


Figure 23: ***Current Generator for Mutually Compensated Voltage Reference***

Performing KVL around the bottom of the device we arrive at Eq. (31)

$$I_D R_{SET} + V_{GS1} = V_{GS2} + V_{GS3} \tag{31}$$

As mentioned in Section 3.3, $MN_{1\text{-}3}$ were sized to be the same size as the output NMOS. Noting that $V_{GS1} = V_{GS2} = V_{GS3}$ and using Eq. (31), one can see that the voltage drop across R_{SET} should be the same as V_{GS1}. Using Eq. (22) one can rewrite Eq. (31) in the form shown in Eq. (32)

$$I_D = \frac{V_{GS1}}{R_{SET}} = \frac{1}{R_{SET}}\left(\frac{\chi}{\sqrt{\mu_n(T)}} + V_{thn}(T)\right) \tag{32}$$

The resistor, R_{SET}, was not fabricated on the integrated circuit. This was partially due to the academic nature of the work, but primarily it was due to process variations and poor temperature coefficients of on-chip resistors. It was advantageous to use an external resistor so that the bias current could be

tweaked. By varying the R_{SET} one could vary the drain current and change at which temperature the effects of mobility and threshold cancel. The minimum and maximum of the two output voltages could be tuned so that they fell within a few degrees of each other. Having access to this node provided more control during debug and thermal calibration. A Startup Circuit was used to ensure that the correct operating point was attained (see Section 3.3). The currents generated in each branch are mirrored into the PMOS in the output stage (refer to Figure 22) which sources the "ideal" current into the diode connected NMOS and PMOS.

This section has described in detail the means to construct a thermally stable voltage reference with two techniques. The reference implements mobility and threshold voltage cancellation to achieve two output voltages (NMOS and PMOS) with zero temperature coefficients (ZTCs). Each branch's ZTC is tunable with the use of an external resistor. Furthermore, it was shown that these output voltages could be linearly combined to produce a voltage reference that is more thermally stable than either of the outputs alone. Now that it has been shown that this technique is possible an important issue must be brought up concerning voltage references and their desired operating point.

3.3 Startup Circuits

A reference must produce an accurate current or voltage. A current generator's purpose is to produce a desired current which will be provided to other branches of the IC; this is desirable in IC design because it is best not to rely on external references. A current generator has two operating points, the desired operating point and the unwanted operating point in which no branch currents are produced in the circuit (zero-state) [21]. The problem of a current generator falling into the undesired operating point is known as the "start-up" problem.

Startup circuits are required to ensure that a current generator is in the desired operating point. A few startup circuits are shown below in Figure 24.

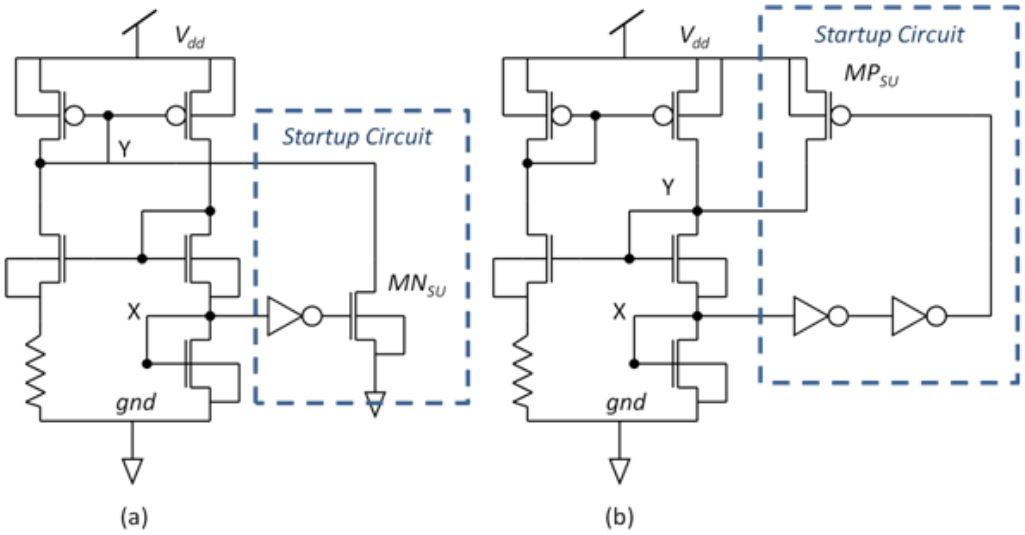


Figure 24: ***Current generator with Startup Circuits Shown***

The purpose of a startup circuit is generally the same: if the supply voltage is on and there is no current flowing in the generator, the startup circuit will disturb the unwanted state and cause the devices to turn on. Consider the circuit shown in Figure 24 (a) and assume the startup circuit is drawing no current (MN_{SU} is off), if there is no current flowing in the current generator then the voltage at node X, V_X, is low

and the voltage at node Y, V_Y, is high. V_X is sensed by an inverter, whose output is fed into NM_{SU}. When V_X is low the gate of MN_{SU} will be high, MN_{SU} will begin sinking current and V_Y will be pulled low. When V_Y is pulled low the current generator will gradually turn on until it reaches its desired operating point. Subsequently, V_X will be pulled high turning off MN_{SU}.

Another example of a startup circuit can be seen in Figure 24 (b). Though it uses more transistors then the previous example its function is the same. If the generator is operating in its zero-state then V_X and V_Y will be low. V_X is sensed by two inverters in series (buffer) and fed to the gate of MP_{SU}. If V_X is low, then MP_{SU} will turn on and begin sourcing current into the current generator; V_Y will be pulled high. After this, the current generator will be in its desired operating point, V_X and V_Y will be high and MP_{SU} will turn off.

The Startup circuit implemented in the mutually compensated mobility/threshold voltage reference is shown in Figure 25.

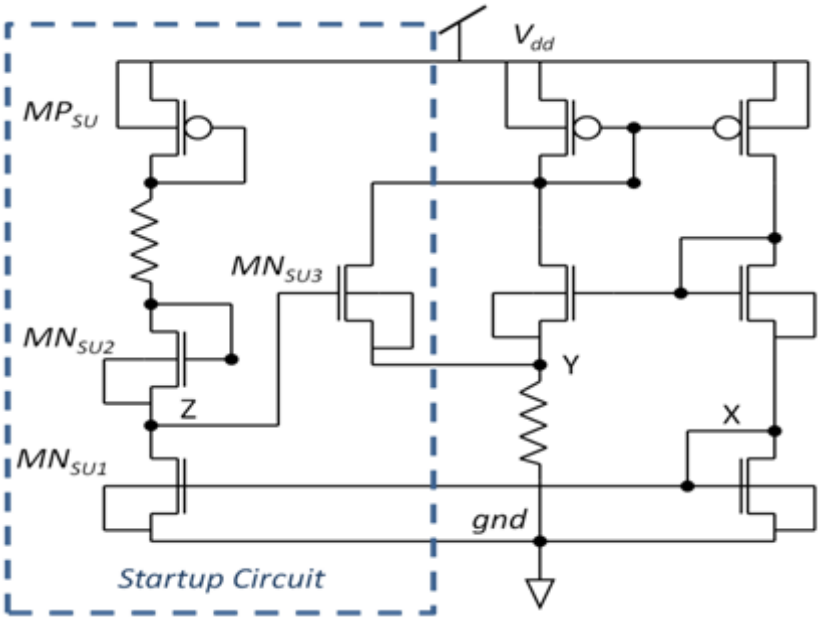


Figure 25: ***Current Generator with Startup Circuit used in Voltage Reference Design***

The principles are the same as before; when the current generator is operating in its zero-state voltage V_X and V_Y are both low. The transistors in the current generator were sized such that the voltage drop across the resistor, V_Y would be the same as the gate-source voltage, $V_{GS} = V_X$, of the NMOS devices. In the zero-state, V_X will be low, MN_{SU1} will be off, and V_Z will be pulled high. When $(V_Z - V_Y) > V_{THN}$ MN_{SU3} will turn on and begin to source current into node Y, raising V_Y. The current generator will turn on gradually and V_X and V_Y will become high; subsequently MN_{SU1} will turn on and pull V_Z low. When $(V_Z - V_Y) < V_{THN}$ MN_{SU3} will turn off.

Ideally once the current generator is operating properly the startup circuit should turn off and draw little to no current. Unlike the previous examples shown in Figure 24, the startup circuit shown in Figure 25 will always draw some current. While this is a drawback, it was an acceptable loss because this start-up circuit guaranteed that MN_{SU3} was completely off (when the generator was in its desired operating point); MN_{SU3} supplied no current into the current generator. It was important that all current generated in the voltage reference was produced solely by the current generator and not MN_{SU3}.

4.0 Fabrication and Packaging

The fabrication process used for the design of a RHBD mutually compensated mobility and threshold voltage reference was IBM's .18 micron CMOS 7RF. CMRF7SF has six metal layers (M1, M2, M3, M4, MT, and ML) with supply voltages of 1.8V core and 3.3 V I/O. Gate oxide thickness, t_{OX}, is approximately 4.5 nm, NMOS threshold voltage of approximately 355 mV, and this process also has triple well devices. This process is not radiation hardened by process; it is a standard-bulk CMOS process.

One of the goals of this work was to show that it is possible to design a voltage reference that was less susceptible to radiation damage without the aid of a RH process. The following section will talk about the fabrication of the two variations of voltage references. It will also go into detail about the design of ELT in this process and comparisons between SG and ELT devices. Considerations for packaging the IC, which make it less susceptible to radiation damage, will also be discussed.

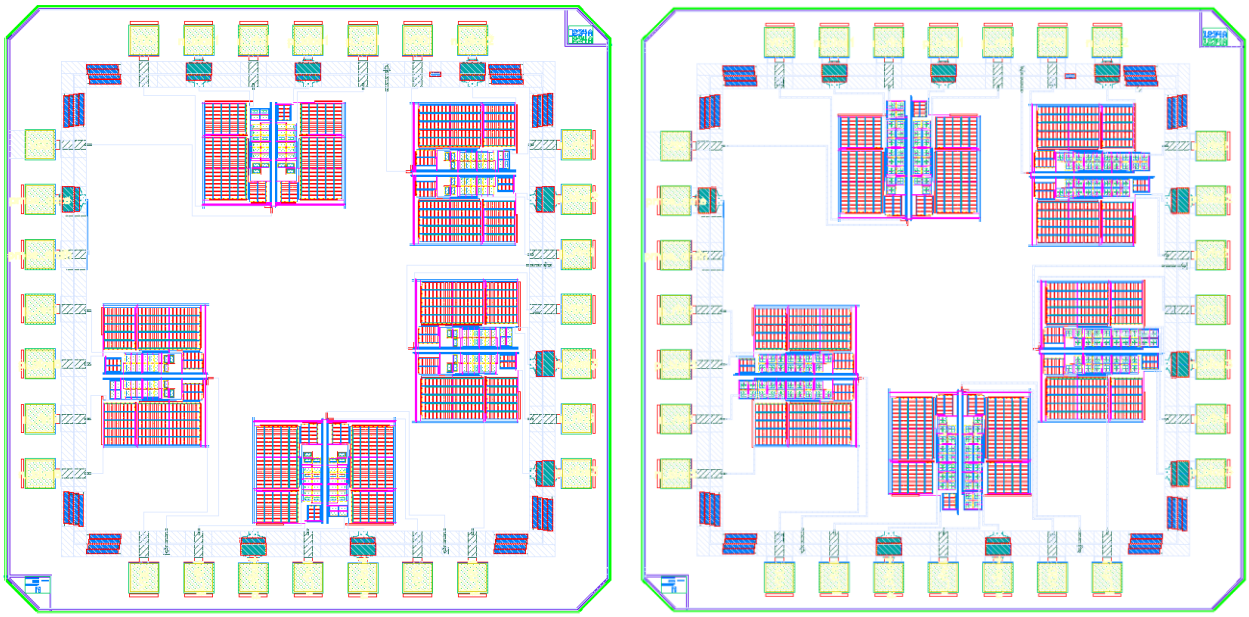
4.1 Design Fabrication in IBM CMRF7SF

There were two variations of voltage references. One was designed with all straight-gate (SG) devices (both PMOS and NMOS devices) and the other replaced the SG NMOS devices with ELT devices. The PMOS devices were all laid out in common-centroid configuration. All of the NMOS devices, including all ELT devices, were laid out using triple well devices. Using triple well NMOS devices eliminates the body effect and is thought to prevent SEL. The body effect is expressed by the term γ and is typically between 0.3 and 0.4 ($V^{1/2}$) [15] and can be seen in Eq. (33).

$$V_{TH} = V_{th0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}) \quad (33)$$

Typically the bulk and source terminals are tied together and connected to ground. However in a cascode configuration an NMOS's source is above ground and cannot be tied to the bulk directly; here the body effect will come into play. When there is a voltage difference between the source and the bulk, V_{SB}, the threshold will vary. A triple well NMOS device includes a standard NMOS that sits in its own p-well and allows the bulk to be tied directly to the source $V_{SB} = 0$ and $V_{TH} = V_{TH0}$.

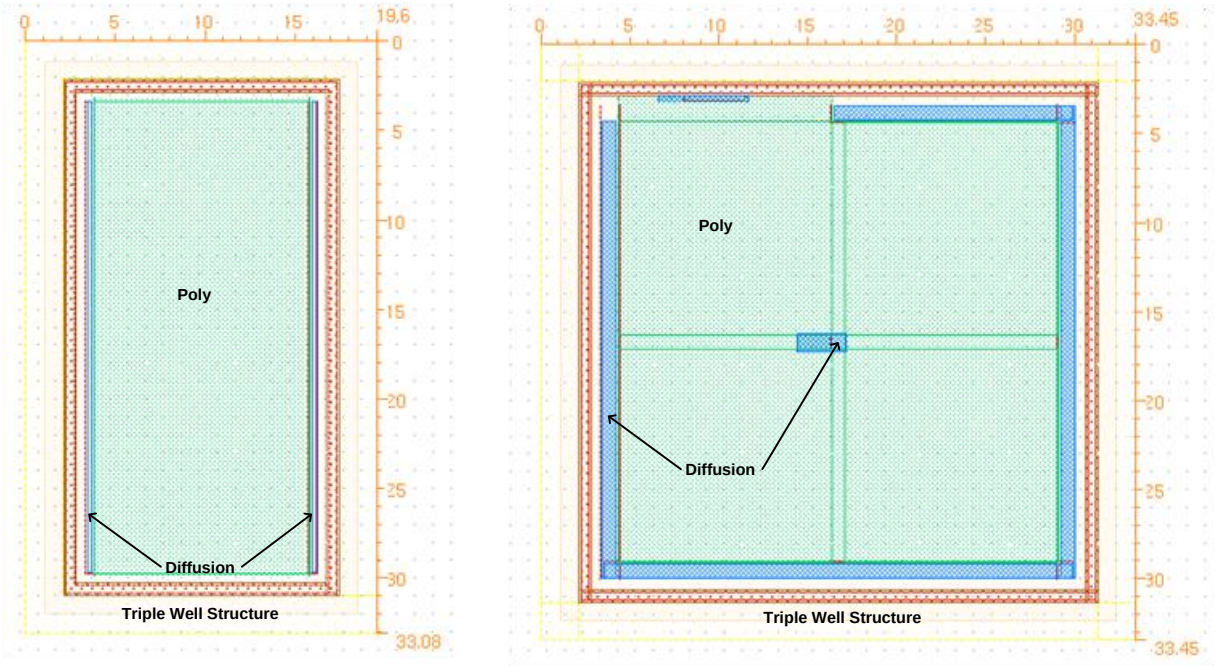
There were two types of ICs made: one with all SG voltage references and one with all ELT voltage references. On each IC there are five voltage references and each share a common supply and ground (V_{dd} and V_{ss}). A die image for the SG and ELT reference can be seen in Figure 26.



(a) (b)

Figure 26: ***Die Image for (a) SG IC and (b) ELT IC***

Since CMRF7SF, is an unhardened process, there were no standard cells for ELTs. Triple well ELTs were laid out manually for the RH voltage reference. Comparing Figure 26 (a) and (b) it can be seen that the ELT reference is slightly larger overall. The triple well ELT and SG devices are shown side by side in Figure 27; the ELT device was sized using Eq. (8) to have the same aspect ratio as the SG. The effective aspect ratios for the SG, Z_{SG}, and ELT, Z_{ELT} were designed to be equal $Z_{OPT} = 2.2$.



(a) (b)

Figure 27: ***Layout for Z_{OPT} of (a) SG and (b) ELT (dimensions in µm)***

It is clear from Figure 27, that the ELT consumes more die area than the standard SG. A more exact comparison between devices can be seen in Table 3.

Table 3: ***A Comparison of the Die Area for SG and ELT Device for RH Voltage Reference***

Area for SG NMOS for Z_{OPT} (μm^2)	Area for ELT NMOS for Z_{OPT} (μm^2)
648.37	1,118.90

The ELT device is almost twice as large as its SG counterpart. There is a complex relationship between device dimensions and aspect ratios for ELTs. An analysis was performed comparing the area tradeoff for different channel lengths and aspect ratios.

The die area consumed by a SG device can be approximated with Eq. (34).

$$Area_{SG} = (L + 2x_{min})W = (L + 2x_{min})Z * L \tag{34}$$

Where x_{min} is the length of the diffusion area, L is the channel length, and W is the width of the device. The effective aspect ratio $(\frac{W}{L})_{eff} = Z$, W was written in terms of Z and L so the equation written could be in terms of desired aspect ratio and channel length. Using Eq. (8) one can derive expressions for W_1 and W_2 in terms of L and Z for a device with four sides (n=4).

$$W_1 = \frac{2(L + l)}{e^{8/Z} - 1} \approx \frac{2L}{e^{8/Z} - 1} \tag{35}$$

$$W_2 = W_1 + 2(L + l) \approx W_1 + 2L \tag{36}$$

Where is L is the channel length, l is a small length used to create a triangle of in layout (to pass DRC) its length is defined by the designer, and in this design l << L. The die area consumed by an ELT can be approximated by Eq. (37).

$$Area_{ELT} = (W_2 + 2x_{min})^2 \approx \left(2L\left(\frac{1}{e^{8/Z} - 1} + 1\right) + 2x_{min}\right)^2 \qquad (37)$$

The dominant term in the expression for ELT area is the exponential in the denominator, except for low values of Z in which case the exponential term is negligible. It can be inferred from the equation that the area of an ELT will approach infinity as Z becomes large. A parametric analysis was carried out examining the ratio of the area of the ELT and area of the SG as a function of channel length for various aspect ratios, the results can be seen in Figure 28.

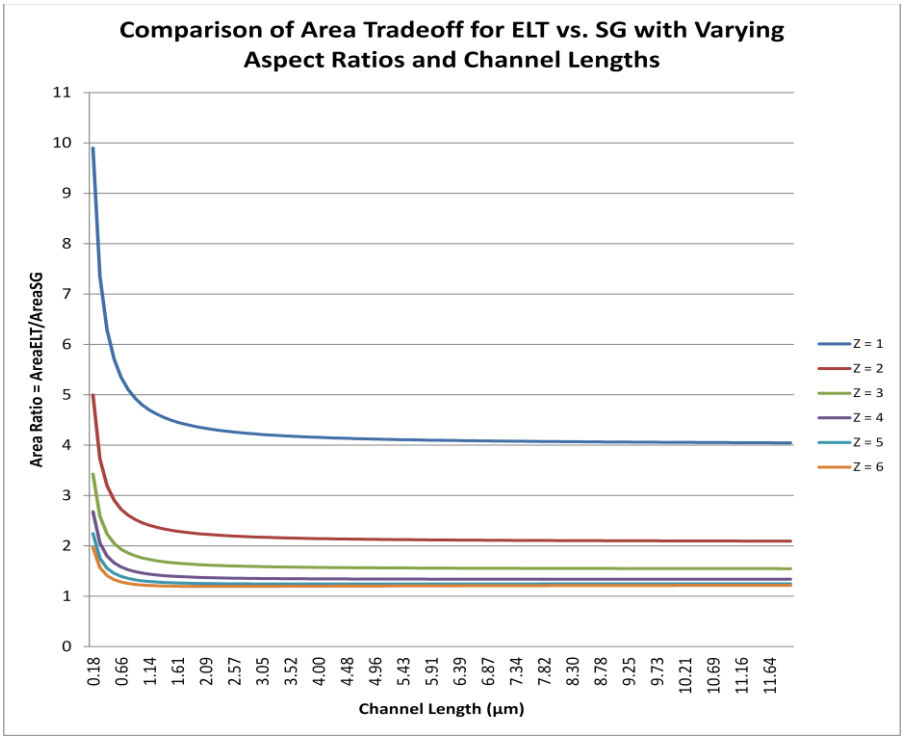


Figure 28: ***Die Area Comparison for ELT vs. SG Device***

It can be seen that for relatively small values of Z that the ratio of ELT area to SG area approaches a value asymptotically. With the assumption that Z is sufficiently small (such that $\frac{1}{e^{8/Z}-1} \ll 1$) Eq. (37) and x_{min} << L, a ratio can be approximated as L becomes large (L>> x_{min}) by Eq. (38).

$$\lim_{L\to\infty} \frac{Area_{ELT}}{Area_{SG}} = \frac{4(L^2 + 2Lx_{min})}{Z(L^2 + 2Lx_{min})} \approx \frac{4}{Z} \tag{38}$$

This behavior is valid for small values of Z because the exponential term in Eq. (37) becomes negligible; however at larger values of Z the exponential term becomes quasi-infinite and dominates the expression for the area of the ELT. The relationship shown in Eq. (38) is a good quick rule of thumb for approximating die area increase for ELTs with moderate channel lengths and low aspect ratios.

In the design of the RH voltage reference a Z_{OPT} and channel length, L, were derived to meet the specifications mentioned in Section 3.2.2. The dimensions of the ELTs were designed to meet the same Z_{OPT} and L. Though less common in literature, Eq. (8) was chosen for the design of RH voltage reference aspect ratio, because at the time of design there was an unwarranted belief that Eq. (2) was invalid for larger channel lengths. Both equations (2) and (8) have three dimensions that dominate the effective aspect ratio of the device, the two inner dimensions and L. The two inner dimensions W_1 and W_2 (d' and d from Eq. (2)) can be expressed in terms of each other, so in reality the effective aspect ratio can be expressed with only two dimensions. Since Z_{OPT} and L are specified W_1 (or d') can be easily found. A ratio of the two equations plotted to see how well the two aspect ratios matched each other (Z_{eq2} and Z_{eq3} respectively). A parametric analysis was performed over varying W_1 = d' and L, this analysis can be seen in Figure 29.

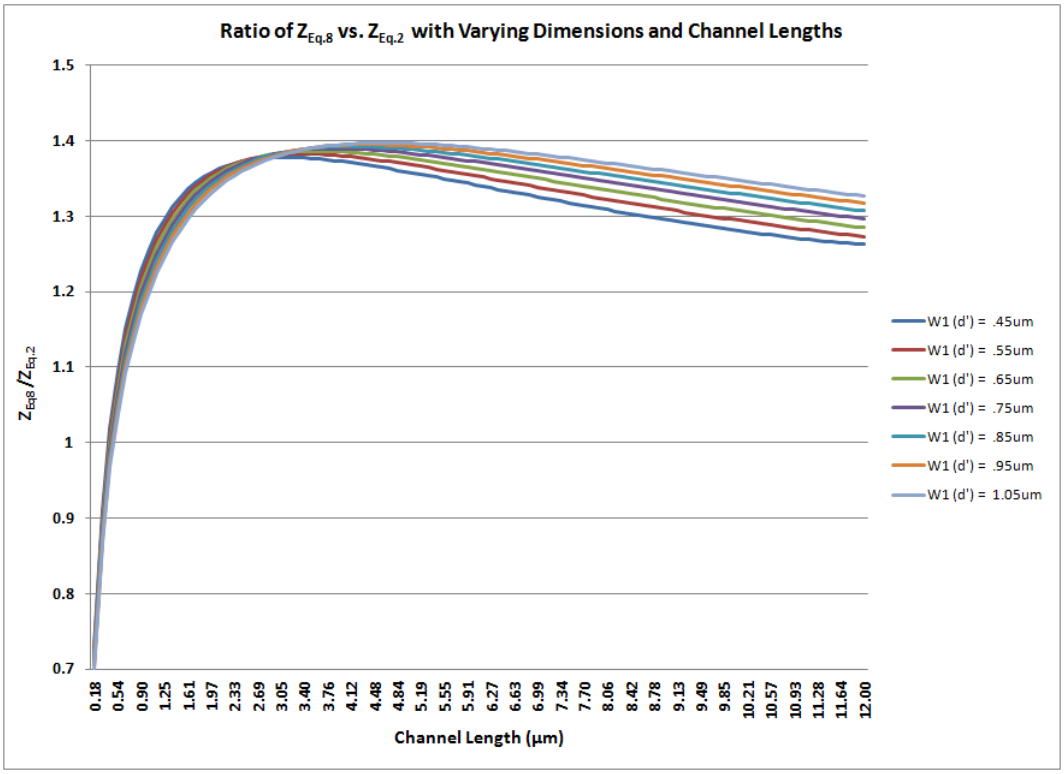


Figure 29: ***Inspection of the Similarity of Two Equations for Effective Aspect Ratio of ELTs***

From the curves it is clear that the two equations do not exactly match up and there is a maximum deviation between the two effective aspect ratios of ± 40 %. A comparison of the effective aspect ratios for ELTs will be explored in greater detail in the future. By attaining the IV curves for standalone ELT devices with varying channel lengths one will be able to extract the effective aspect ratio; this will be compared to the two equations found in literature (preliminary analysis can be seen in the Appendix).

4.2 Packaging

Once the SG and ELT references passed design rule check and layout versus schematic (DRC and LVS) they were placed within a bond ring. The last step in the IC fabrication design for the design engineer is choosing the package that will house the IC. A package can be chosen that satisfies the design specifications (device dimensions and pin count). Typically, the type of material used for the package is of little consequence to the designer; however, this is not the case in applications where radiation exposure is of concern.

TID was discussed in detail in Section 2.0, dose enhancement can also occur at the interfaces of different materials (i.e. metal contact and Silicon). Problematic dose enhancement can be found at two areas on an IC, the chip metallization and the inside material of the package's lid [22]. There are a few types of packages/lids used in IC fabrication including, ceramic, nickel, and gold. There are also several types of metallization techniques. Materials that are more prone to high dose enhancement have a high atomic number, Z, there is a direct correlation. There is a chance to accrue more dose if one uses materials (packages/lids or metallization) that are high-Z [22]; the metallization used in the CMOS process is Aluminum which has no enhancement under the metallization. It was important to select a package/lid with a low Z for the RH voltage reference.

The SG and ELT voltage references would be subjected to total dose and there susceptibility would be compared. It was important to ensure that there was no dose enhancement due to secondary processes such as metallization or packaging, because secondary dose enhancement would corrupt the data from TID testing. Gold and "Kovar" lids are high-Z and moderate-Z materials respectively. In the presence of an x ray there will be strong to moderate dose enhancement over the entire active region of

the chip. Gamma rays cause lower dose enhancement effects than x rays because they have much higher energy [22]. Though TID testing would be using a Co_{60} source which emits gamma rays a ceramic package/lid combination was chosen to house both SG and ELT references. A ceramic lid and Aluminum metallization is the best combination to reduce dose enhancement over the entire active region of the chip.

5.0 Testing

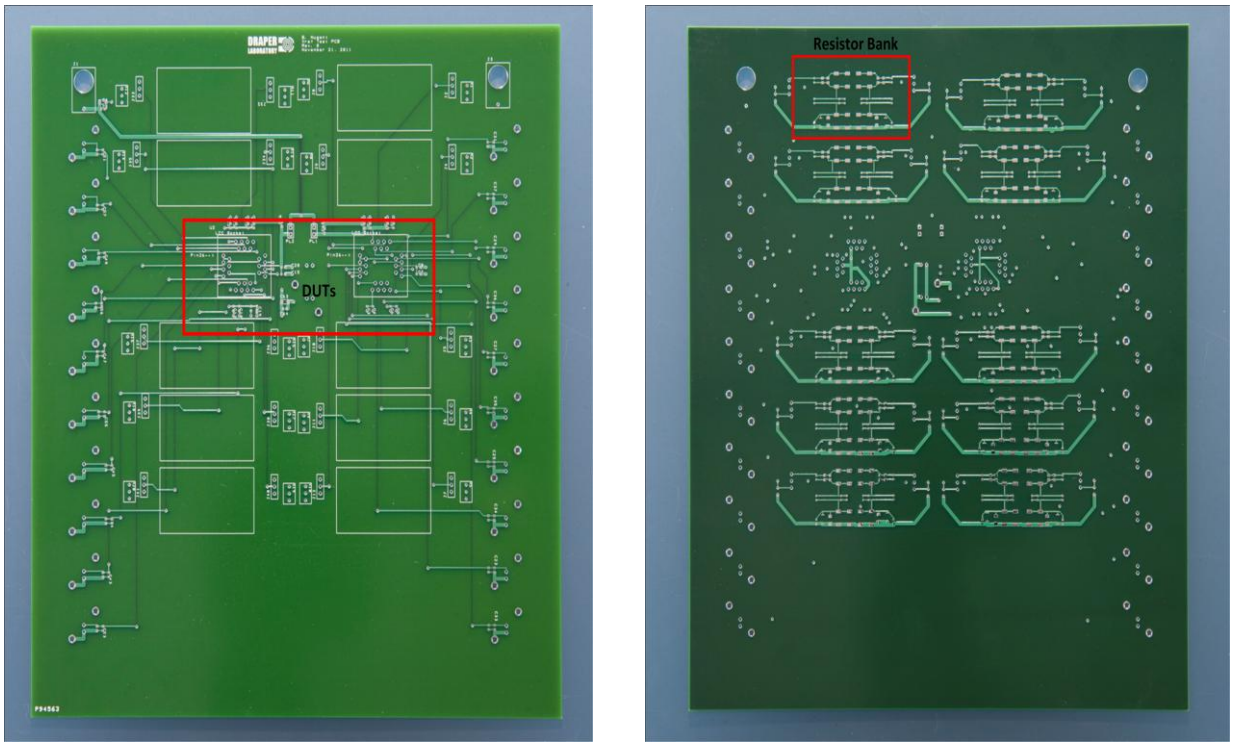
This section will explain the method, data acquisition, and experimental results for both electrical/thermal testing and TID testing. Thermal profiles of the output voltages of the NMOS and PMOS were collected and their saddle points were evaluated. It was possible to align the saddle points of the NMOS and PMOS curves for a given temperature with their individually tunable external resistances. The electrical/thermal testing would show empirically that the mutually compensated mobility and threshold voltage technique is a valid foundation for a voltage reference. Another important goal of this work was to compare the behavior of the SG and ELT devices in the references. Matching between references will also be explored. Finally, TID testing would test how RH the voltage references were. It was crucial to calibrate each reference (such that NMOS and PMOS curves were aligned) at the same temperature that they would be exposed to during TID testing. This way a comparison of SG and ELT reference performance could be examined pre/post radiation.

5.1 Electrical and Thermal Testing

5.1.1 Printed Circuit Board (PCB) Design

A PCB was designed to test the aforementioned voltage references, see Figure 30. Each PCB would hold two devices under test (DUTs). The board was designed to hold two DUTs so that a comparison could be made between ELT and SG ICs during testing. More importantly it was important to have the DUTs close together so we could say that they had uniform exposure to the same total dose

during radiation testing. The PCB was fairly simple in nature because only DC voltages and current were being measured.



(a) (b)

Figure 30: ***Picture of (a) Front and (b) Back of Unpopulated PCB Used for Electrical Thermal Testing and Radiation Testing***

Shown in Figure 31, is the concept for the PCB design. There would be supply and ground (for the entire IC) and four unique pins (V_N, V_P, R_{BIASN}, and R_{BIASP}) for each reference. The output voltages would be connected with decoupling caps for a cleaner signal and were measured using BNC connections (this is the primary reason for the PCB's large size). The power supply line also had decoupling caps. A jumper was placed in series between the supply line and each DUT so quiescent current could be measured for each DUT. The R_{BIASN} and R_{BIASP} Networks were comprised of a

potentiometer and a resistor array (with the ability to jump in one or the other). The former was used for coarse/initial bench calibration and the second was used for more accurate thermal measurements.

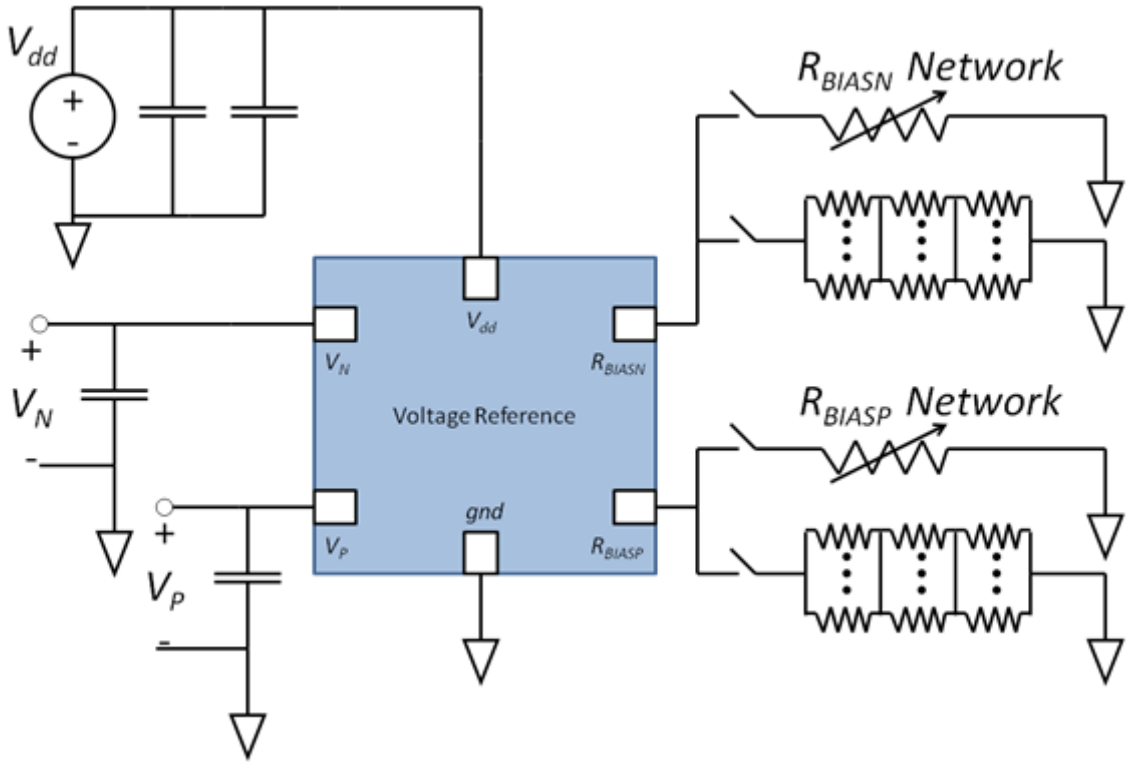


Figure 31: ***Concept of PCB Schematic for a Single Voltage Reference***

Because we were unsure which empirical resistance would produce the desired ZTC, the resistor array was designed such that many combinations of resistances could be soldered to the PCB. The resistor array was made up of three tiers, each with various footprints connected in parallel, connected in series. These discrete resistors were low ppm/°C resistors. Several resistances were ordered ranging from 10-20,000 (Ohm). From simulations, it was found that the ideal value of resistors R_{BIASN} and R_{BIASP} were 6.301 (kOhm) and 6.835 (kOhm) respectively. Due to process variations and mismatch it was anticipated that the values predicted from simulation would be off.

To obviate possible changes in resistance values a MATLAB script was written which took in all the values of the discrete resistances and provided the closest approximation to an ideal resistance allowed by the discrete values. To provide an insight into how many of each resistor should be purchased another MATLAB script was written. This script created N random resistance values centered at the ideal values of R_{BIASN} and R_{BIASP} plus or minus a few thousand Ohms. Using the first script mentioned, the values of the resistors required to approximate the random value was counted. The number of times each resistance was used was saved and tallied. These numbers provided an insight of how likely it was that a given resistance value would be required for the approximated value of R_{BIASN} or R_{BIASP}. A distribution was found and multiplied by how many resistor arrays required (plus some overstock), and this number was the total low ppm/°C resistors ordered.

A thermistor was also included on the PCB directly between the two DUTs. The thermistor was used to monitor the temperature on the device. A constant current was sunk into the thermistor and the equivalent resistance was found by using Ohm's Law. The temperature seen by the thermistor was derived using Eq. (39) from the device's datasheet; it is an extended version of the Steinhart and Hart interpolation laws.

$$T(R) = \left(A_1 + B_1 \ln \frac{R}{R_{ref}} + C_1 \ln^2 \frac{R}{R_{ref}} + D_1 \ln^3 \frac{R}{R_{ref}} \right)^{-1} \tag{39}$$

Where A_1, B_1, C_1, D_1 are constants found on the datasheet, R_{ref} is the resistance of the thermistor at 25 °C, and R is the resistance measured. The Steinhart and Hart interpolation's of temperature for a negative temperature coefficient (NTC) thermistor was calculated and could be compared with accuracy

of the thermal chamber used for electrical/thermal calibration. The thermistor was also used to detect temperature shifts during TID testing.

5.1.2 Data Acquisition

Automatic data acquisition proved invaluable for electrical/thermal testing; it laid the foundation for data acquisition for all remaining tests. MATLAB R2011b was the software used for data acquisition as well as post processing. A suite of scripts was designed from interfacing with individual instruments (Keithley 2001/2010 (DMM), Thermotron 2800 (Environmental Temperature Test Chamber), Agilent E3631A (Power Supply), and Yokogawa 7651 (Programmable DC Source)), to data storage and post processing.

The scripts used for data acquisition were broken up into a hierarchy. The scripts at the lowest level were the classes that held all the functions to communicate directly with the instruments. Most instruments had the capability to be remotely interfaced with Standard Commands for Programmable Instruments (SCPI). The functions contained in the classes were used to perform simple functions such as, create an instrument as an object, delete instruments, different settings for instruments, and perhaps most importantly read data. The classes were used in every script that controlled or interfaced with an instrument.

Though the test procedure varied from experiment to experiment, the principal actions required for the electrical/thermal calibration were the same. Initialize all instruments for test (this includes output settings, filter settings, and setting the initial temperature in the thermal chamber), and finally

acquire data from relevant instruments. This is more convoluted than it sounds and warrants an example to illustrate:

Upon declaring all variables and initializing all constants including setting the desired temperature points where the DUT will be tested. A for loop is used to increment the different temperature settings, within the for loop are sequential two while loops. The first while loop monitors the temperature in the Thermotron; and compares it to the desired temperature. The Thermotron claims to reach its set temperature much faster than as shown by the thermistor. To avoid this, a second while loop is used which reads the voltage and current off of the thermistor and converts it to the temperature in the chamber. The thermistor is believed to be the more accurate temperature measuring device due to its proximity to the DUTs. The thermistor is an improvement over the Thermotron temperature reading; however it does not provide the temperature at the die and the DUTs may not have reached their thermal equilibrium.

Once the temperature within the chamber was sufficiently close (some value ε) to the desired temperature. Many samples were taken for each measurement and averaged; this mean was called the static DC value for a given temperature, and this information was saved. The for loop continued in this fashion for the specified temperature values. While the script changed in small ways for different tests, the basic flow (see Figure 32) remained the same. This automation allowed for many hours of accurate data acquisition with the press of a button.

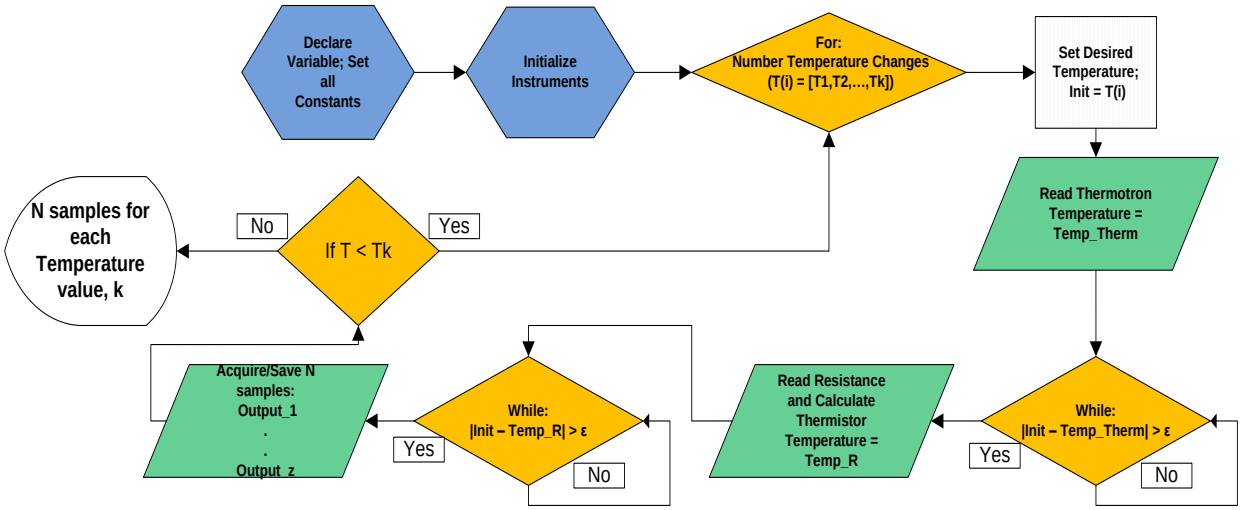


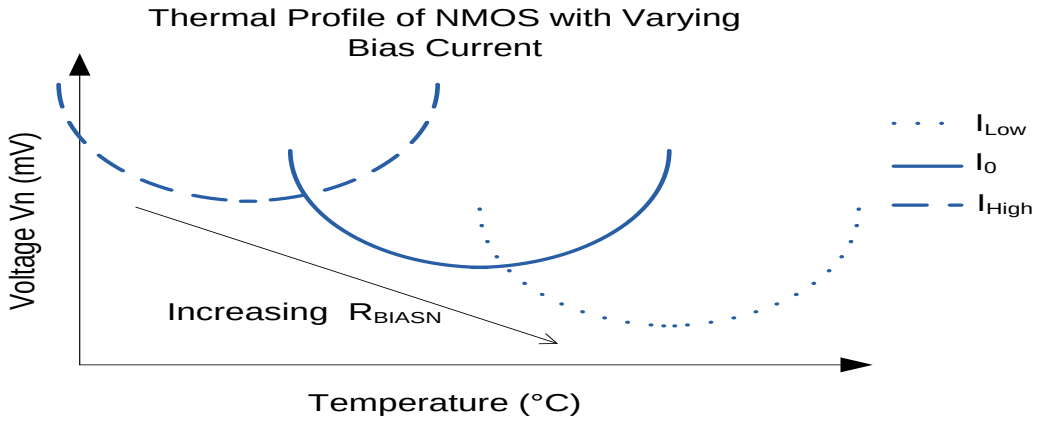
Figure 32: ***Sample MATLAB2011b Data Acquisition***

The MATLAB license used for the electrical/thermal calibration was not a standalone license. Licenses that shared impose a maximum time allowed for MATLAB to run scripts when there is no input from a user. This is most likely implemented so idle MATLAB processes return their licenses to the pool of shared licenses. The default timeout value is four hours; and this was the maximum time allowed for a single script to run. This limited the number of temperature values where data could be acquired. The, "rule of thumb" was that the Thermotron required approximately 30-40 minutes to reach equilibrium; this along with time taken to acquire data limited the number of temperature values to around four to five depending on how many outputs were measured.

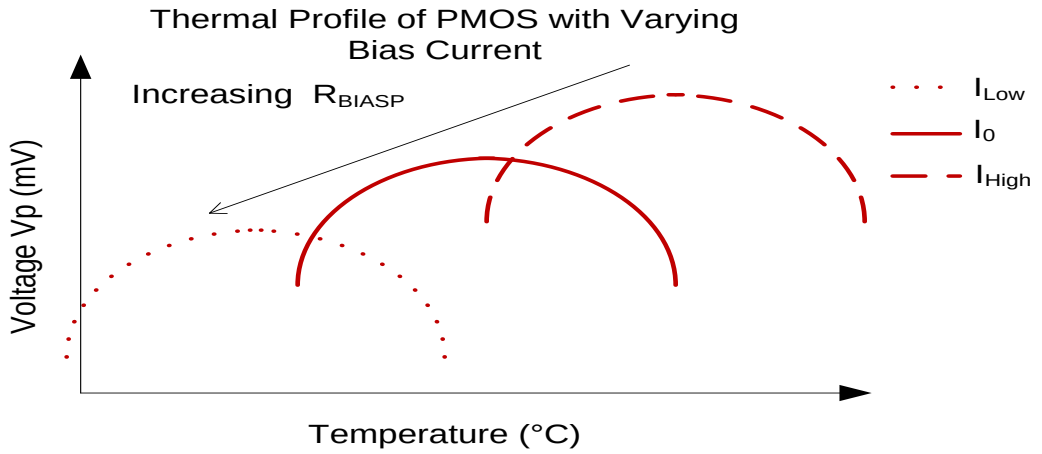
5.1.3 Calibration

It was important to calibrate each half of the reference such that the minimum and maximum were within a few degrees of each other. To achieve a more stable voltage reference the thermal

profiles of the NMOS and the PMOS had to look like mirror images of each other. This calibration was the first thing done in Electrical/Thermal Testing. Changes in the output voltages' thermal profile can be seen in Figure 33.



(a)



(b)

Figure 33: ***Thermal Profile Curves for (a) NMOS and (b) PMOS with Varying Bias Currents***

It can be seen from Figure 33 that the saddle point of the thermal profiles varies with a change in the external resistance. The external resistances, R_{BIASN} and $R_{BIASP,}$ set the bias currents that are

mirrored into the respective output stages. The currents flowing in the output stages are I_N and I_P (NMOS and PMOS respectively). An increase in R_{BIASN} (which corresponds to a decrease in I_N) shifts the saddle point location, T_{0N}, positively, and conversely a decrease in R_{BIASN} (increase in I_N) shifts T_{0N} negatively. Decreasing I_P shifts its saddle point location, T_{0P}, negatively and increasing I_P shifts T_{0P} positively. A positive or negative change in bias current produces opposite shifts of the saddle point for NMOS and PMOS diode connected devices.

Increasing the current in the both branches shifts T_{0N} and T_{0P} in opposite directions. During initial calibration it was found that both R_{BIASN} and R_{BIASP} needed to be increased from the anticipated simulated values. Increasing R_{BIASP} shifted T_{0P} to lower temperatures and increasing R_{BIASN} shifted T_{0N} to higher temperatures. This has not been resolved mathematically, but the behavior predicted by the simulator was confirmed in the electrical/thermal tests.

This relationship was used to initially calibrate and fine tune each half of the voltage reference such that their output voltages' minimum and maximum could be aligned. During the initial calibration, a DUT was placed inside the Thermotron 2800 at a given temperature T_1 for a sufficiently long time allowing the DUT to settle into their thermal equilibrium. A form of a discrete potentiometer, outside of the chamber, was used for R_{BIASN} and R_{BIASP}. Measurements would be taken for an initial resistance and then an incremental resistance would be added and another measurement would be taken. After all measurements were taken the temperature was raised by a five degree Celsius increment to T_2 and the resistance was brought back down to its initial value. Measurements were recorded as before. By varying resistors outside the Thermotron 2800 we removed any correlation between the thermal behavior of the resistance and the DUT.

5.1.4 Electrical and Thermal Test Results

The following section will be divided into two sections, the first will be preliminary findings that modified original procedures as well the initial calibration technique (discrete resistances that were off chip and outside of the Thermotron) and the second will be temperature sweeps with the low ppm/°C resistors on chip.

5.1.4.1 Preliminary Findings/Calibration

An electrical connectivity check was performed on the PCB board to ensure that there were no unwanted shorts or open connections. The values of R_{BIASN} and R_{BIASP} predicted in simulation were dialed in with the ten potentiometers required for one IC (five resistances for both NMOS and PMOS branches). Before any IC was placed within the chamber the static room temperature voltages were measured. A SG IC was tested and the voltages were nominal (which showed the circuit was functional) but not functioning in their desired operating points. Thermal sweeps would be performed with varying resistances to obtain the desired operating point for each reference.

The mutually compensated mobility/threshold voltage reference simulated to have very low ppm/°C therefore measurements required should be below 1 ppm/°C (preferably 0.5 ppm/°C). At room temperature T ≈ 24°C, an output voltage from a SG was sampled N times using a DMM interfaced with GPIB to a National Instrument Driver which was processed by MATLAB. The mean and standard deviation were monitored over varying N. N was increased until the standard deviation of the mean was on the order of single ppm/°C. Preliminary analysis of the data showed that this criterion was met when N was approximately 450. The time it takes to acquire N (where N = 450) using MATLAB is approximately

two minutes. The sample filter and the interpolation time of the DMM were also modified to improve measurements.

The next preliminary analysis was to monitor the output voltages, V_N and V_P, within the Thermotron and monitor the voltage as the Thermotron reached a new thermal equilibrium. This is not to be confused with thermal sweeps, but instead it is monitoring how long it takes for the output voltage to reach its new thermal equilibrium. First the temperature readings were measured from the Thermotron and then the approximate temperature was calculated using Eq. (39). The thermistor on the board proved invaluable for the determination of the approximate temperature at the PCB. When the temperature of the Thermotron was incremented (with the MATLAB script) it took a while for the temperature near the DUTs to reach the new programmed value. The results from this preliminary analysis can be seen in Figure 34.

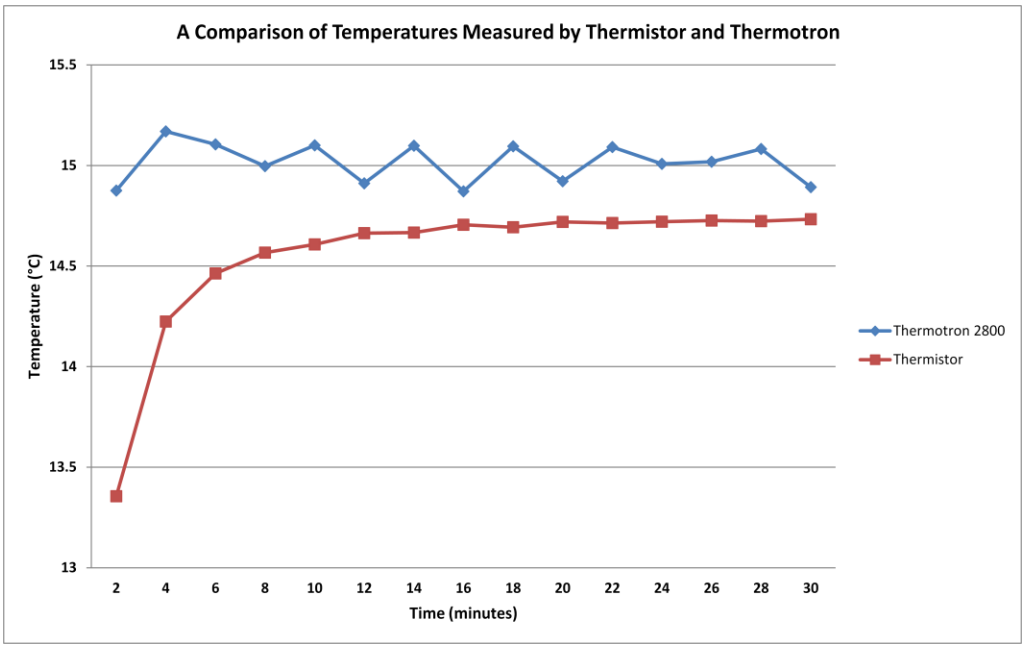
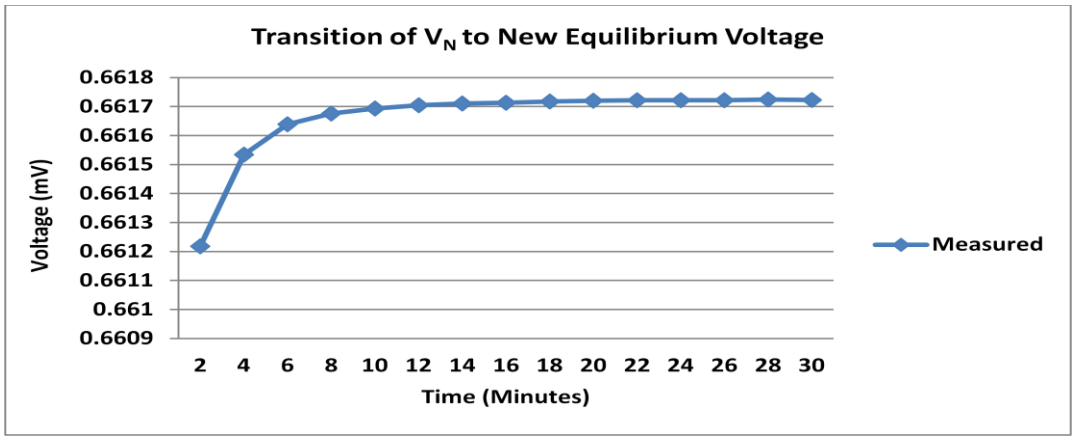
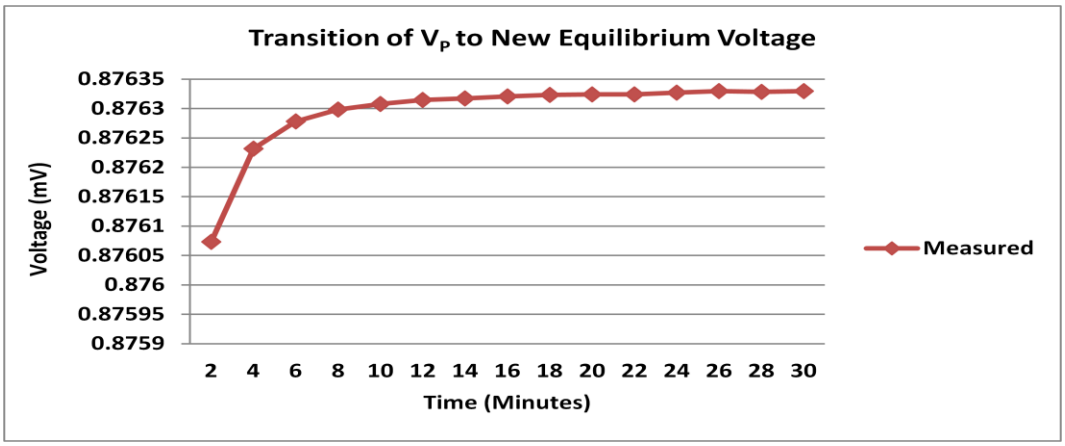


Figure 34: A Comparison of *Temperature Measured in the Thermal Chamber*

This figure shows the recorded temperature readings when the thermal chamber goes from 10 °C to 15 °C. The Thermotron measures that it has reached the desired temperature of 15 °C within two minutes; however the sensor for this is not near the PCB (and consequently the DUTs). In reality it can be seen from the curve of the thermistor, which is in close proximity to the DUTs, that the temperature approaches the desired temperature after approximately 30 minutes. The output voltages were also measured and exhibit what appears to be a "thermal tail", an analogy can be drawn to an RC time constant, see Figure 35.



(a)



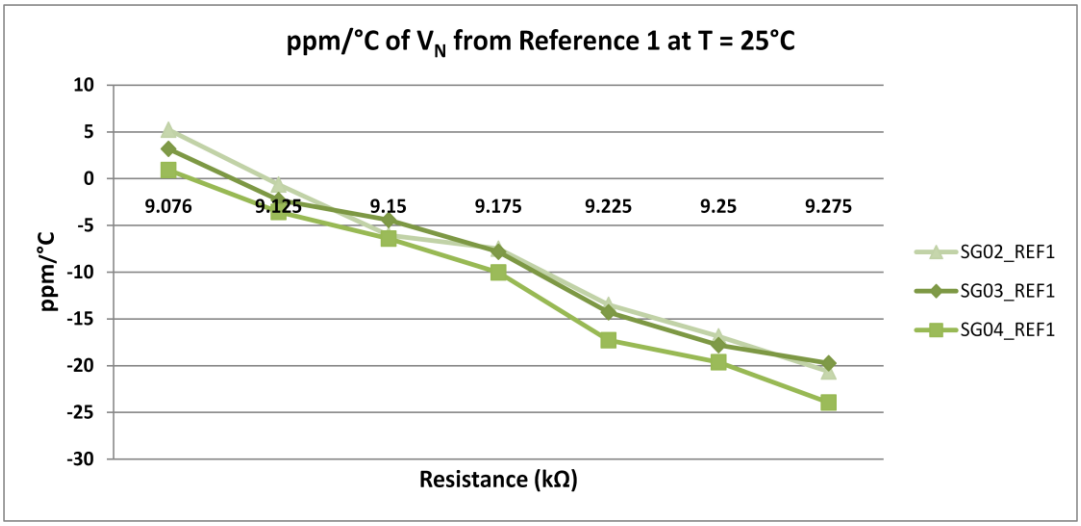
(b)

Figure 35: ***Transition of (a) V_N and (b) V_P to Their New Thermal Equilibrium Voltages***

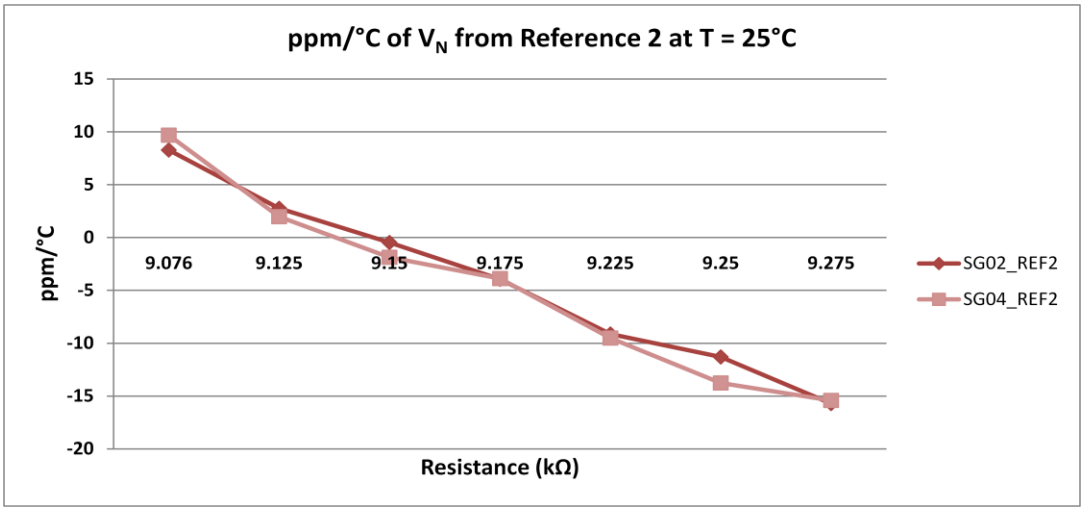
These thermal tails were seen repeatedly for different ICs, different references on individual ICs, and for different temperatures. The MATLAB scripts were changed and data would only be collected after a "hold time" that was at least 35-40 minutes (depending on the test time). Now that reliable data could be recorded the initial calibration was started for individual references.

Initially, the test method involved populating the resistor arrays with discrete low ppm/°C on the PCB and performing a thermal sweep for that set resistance. After the data were collected and analyzed the resistance was changed if the saddle point was not at room temperature (T ≈ 25°C). This process could take several hours (four hours for data acquisition and subsequent hours for modifications to the resistor array). The process was streamlined by having a discrete resistor bank outside of the chamber with several values (as mentioned in Section 5.1.3) and measuring data at only two temperatures. The two temperature points were set such that their average was approximately T ≈ 25°C. Choosing this range of temperatures provided a "window" into the ppm/ °C point at room temperature by linearly interpolating the data.

After the required hold time at the lower temperature, N samples were taken for each resistance value. This process was repeated for each output. Once all of the output voltages were recorded for all values of resistances, the temperature was increased, held for the required hold time, and data were taken in a similar fashion. The point where the ppm/°C crosses the x axis is the external bias where the ZTC will occur at room temperature. The NMOS ppm/°C curves for several references and ICs were plotted and can be seen in Figure 36, similar plots for the PMOS ppm/°C can be seen in Figure 37.



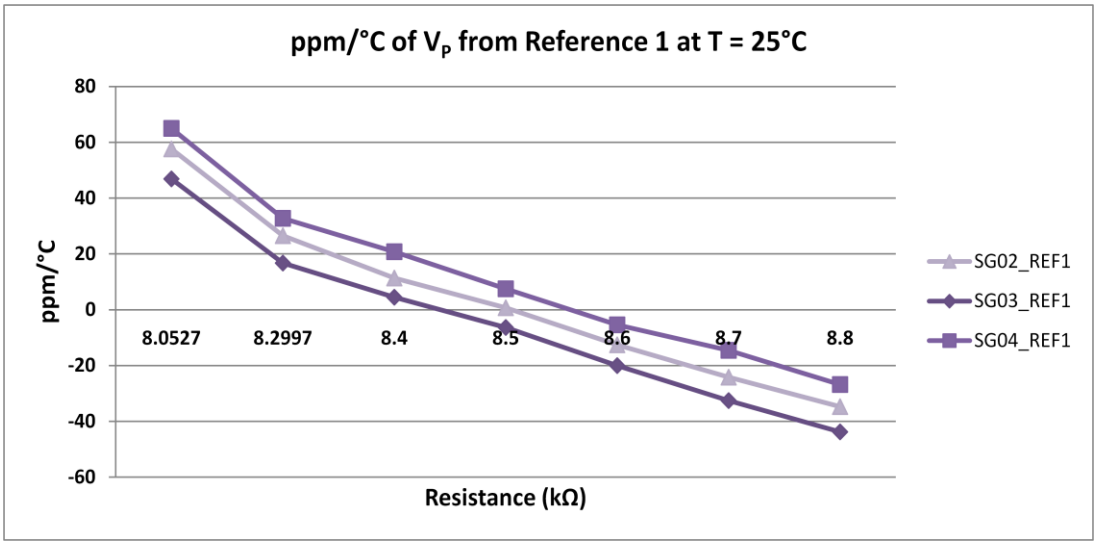
(a)



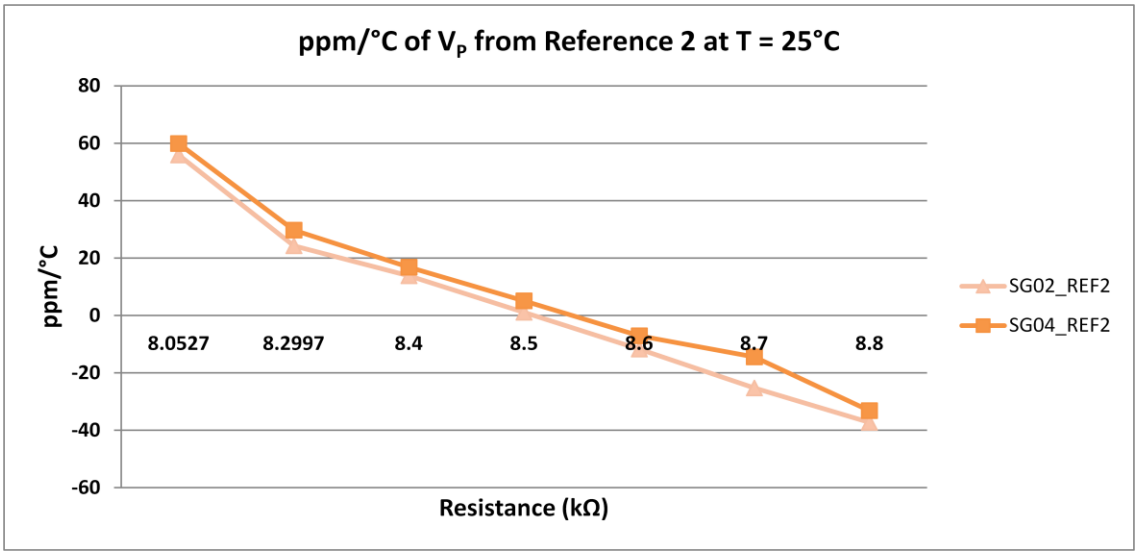
(b)

Figure 36: V_N *ppm/*°C Curves for Different ICs (a) Reference 1 and (b) Reference 2

It is important to clarify the nomenclature that will be used for the remainder of this document. Each IC has five references and there are two variations of ICs. The nomenclature used for the figures is of the form SGa_REFb and ELTa_REFb where "a" refers to the IC used, "b" refers to the reference used, and SG and ELT differentiate between the SG and the ELT variation.



(a)

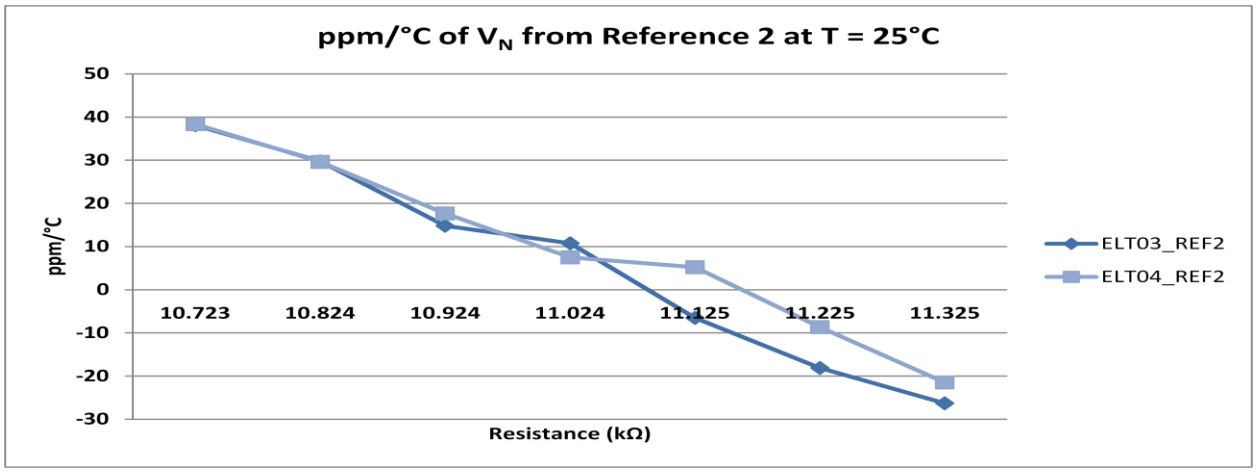


(b)

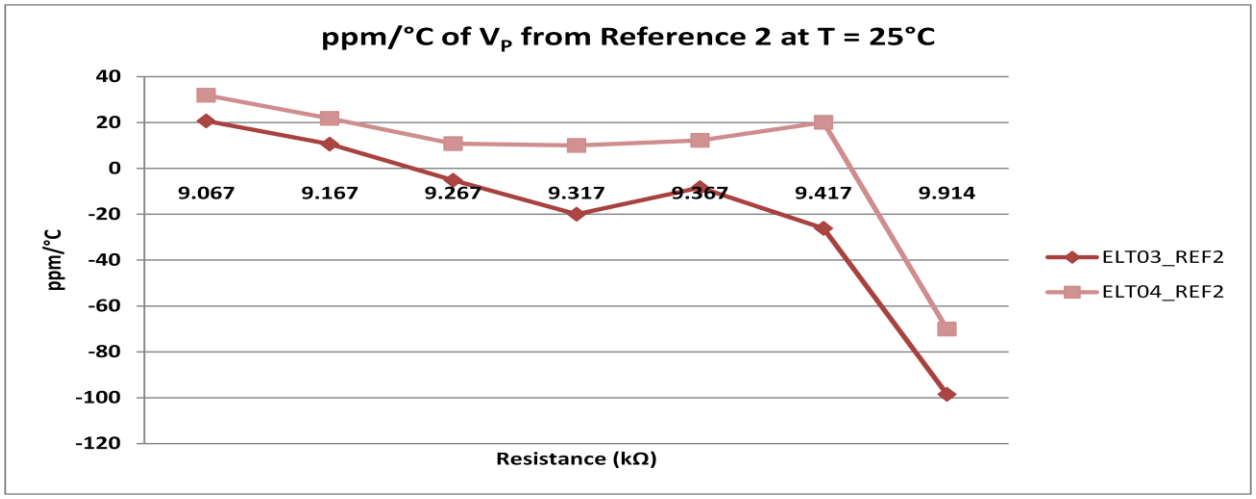
Figure 37: ***V_P ppm/°C Curves for Different ICs (a) Reference 1 and (b) Reference 2***

Ideally each reference would require approximately the same bias resistance (R_{BIASN} and R_{BIASP} respectively) for all five references on an IC; but this was not the case. The actual values for the bias

resistances were much higher than predicted by the simulator. It is clear from the plots that each reference's R_{BIASN} and R_{BIASP} are slightly different from IC to IC and reference to reference (on the same IC). The same process was done to calibrate the ELT references the results for one reference from two different ICs was collected and can be seen in Figure 38.



(a)



(b)

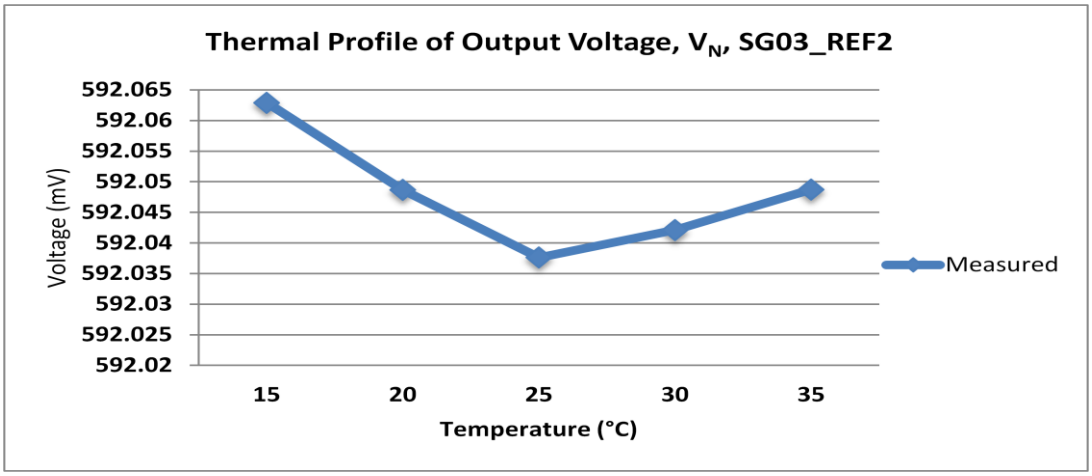
Figure 38: ***Different IC ppm/°C Curves for (a) V_N and (b) V_P***

Less data were collected during calibration for the ELT ICs due to timing constraints. From the calibration data the curves should all be decaying because the resistance is being increased; however there is an abnormality in Figure 38 (b) where for a range of resistance the PMOS ppm/°C goes up and then continues to go down. This was attributed to an error during measurement, and a linear interpolation was used to approximate the required bias resistor for the PMOS output for the ELT IC.

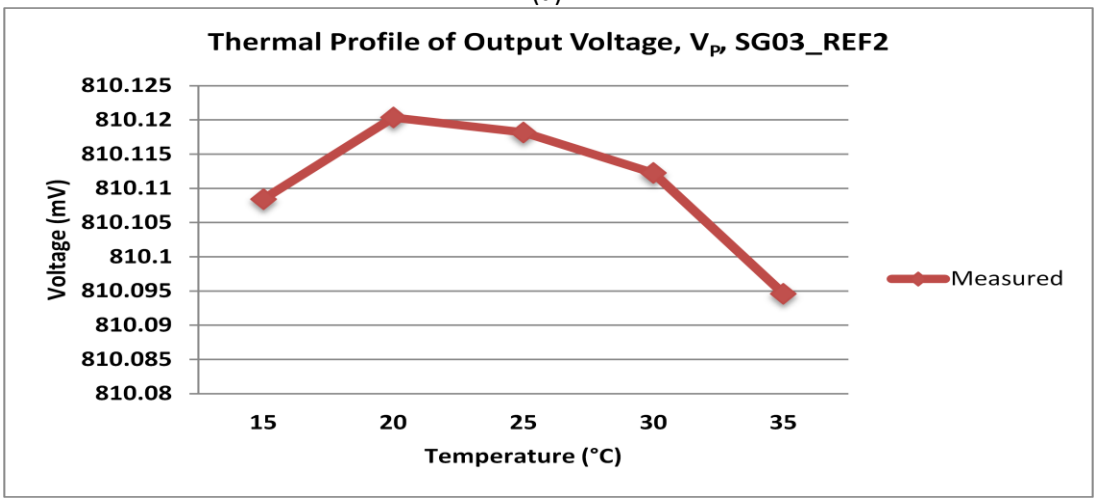
An approximate value was chosen for each reference's proper bias resistance (the point where it crossed the y-axis). This approximate value was used in the MATLAB script that gave the closest value using only the resistors with low ppm/°C in the resistor arrays. This MATLAB defined approximation was taken and each reference was populated with the resistance closest to what was observed during the previous experiment. Thermal sweeps were performed again with all components of the voltage reference on the PCB and contained within thermal chamber.

5.1.4.2 Thermal Sweeps and Post-Processing

With the references calibrated, a coarse thermal sweep could be performed. The thermal profiles for each output (V_N and V_P for SG and ELT references) were collected. Though a few more iterations were made to the bias resistances, the results will be shown for references who's V_N and V_P saddle points are within five °C of each other. The measured outputs (V_N and V_P) from SG03_REF2 as well as their ppm/°C are shown in Figure 39 and Figure 40.

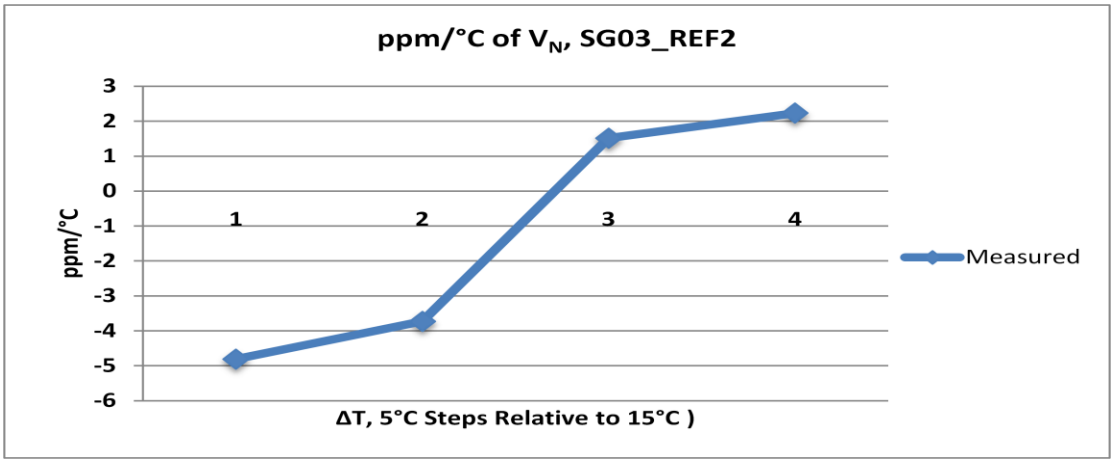


(a)

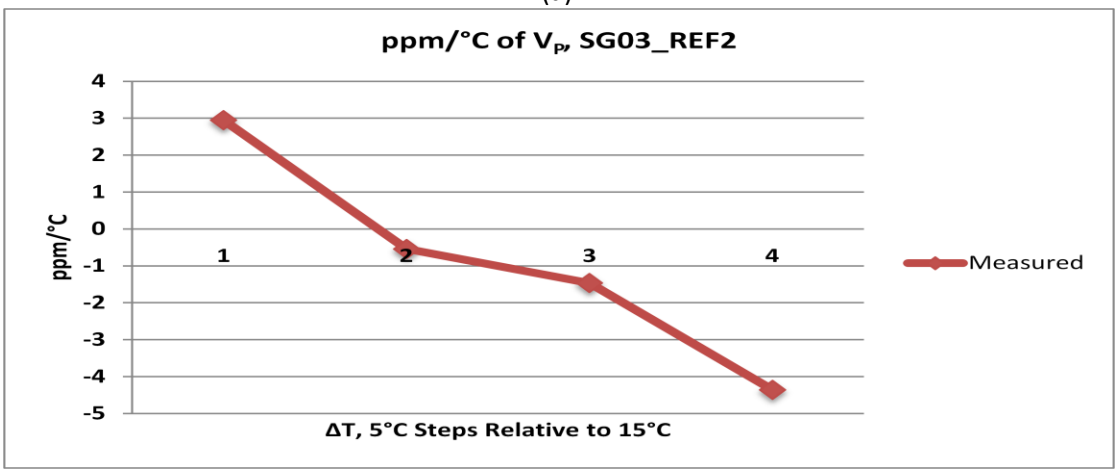


(b)

Figure 39: ***Measured Thermal Profiles from SG03_REF2 for (a) V_N and (b) V_P***



(a)



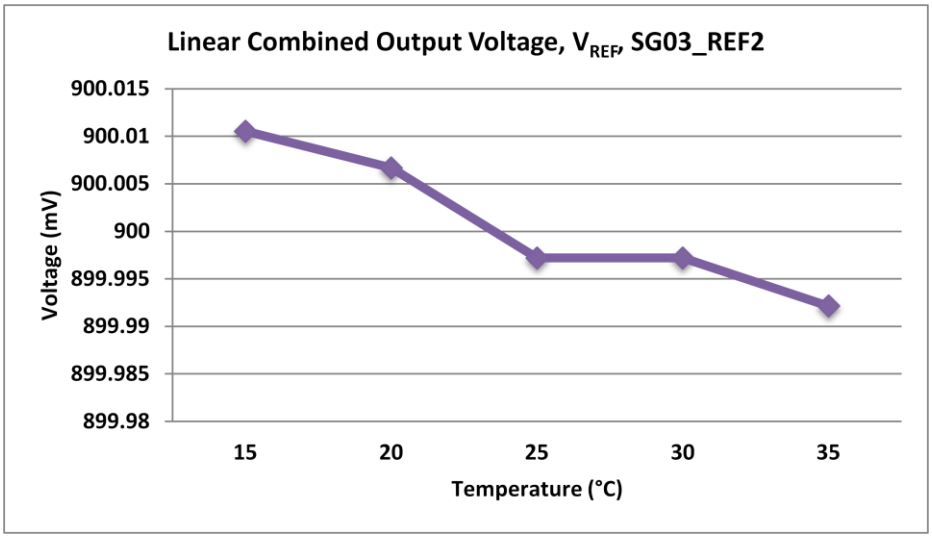
(b)

Figure 40: ***ppm/°C of Thermal Profiles from SG03_REF2 for (a) V_N and (b) V_P***

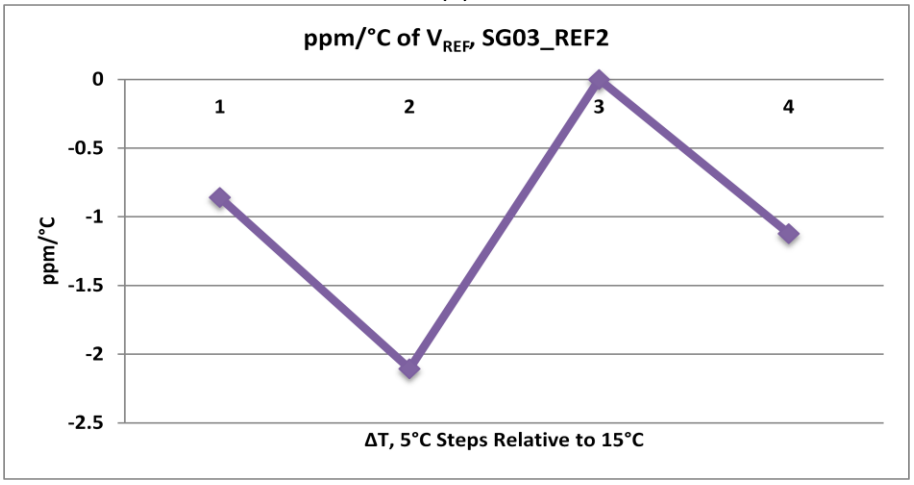
These thermal profiles show that it is possible to mutually compensate mobility and threshold voltage for both NMOS and PMOS devices (for a given I_D, Z_{OPT}, and T_0). These measured outputs were processed in MATLAB to achieve an ideal linear combination to produce V_{REF}. As alluded to in Section 3.2.2, there is a way to linearly combine V_N and V_P which can be seen in Eq. **(40)**.

$$V_{REF} = Y(V_N + XV_P) \tag{40}$$

In simulations, the variable X was chosen such that the ppm/°C of V_{REF} was around T_0 and Y was chosen until the mean of V_{REF} occurred at T_0. The definition used for the determination of X for measured results was chosen such that ppm/℃ was closest to zero at room temperature; the definition of Y remained unchanged from that used for simulations. Note that the values of X and Y can be chosen such that this criteria can be changed. The value for X and Y, for SG03_REF2, were found to be 0.715 and 0.7149 respectively. The new output voltage, V_{REF}, as well as its ppm/°C can be seen below in Figure 41.



(a)

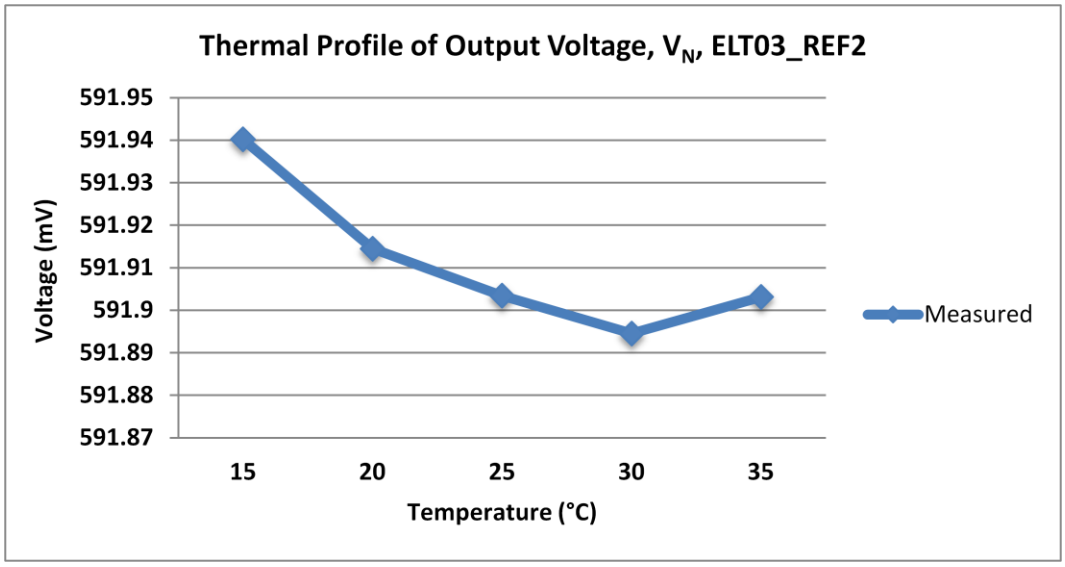


(b)

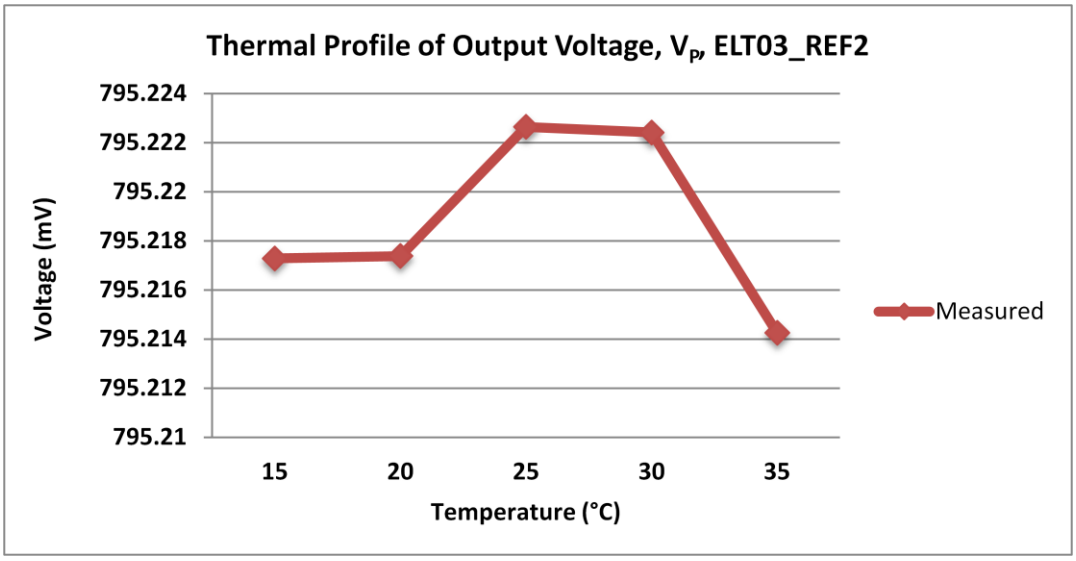
Figure 41: ***(a) Thermal Profile of Linearly Combined Output Voltage, V_{REF}, and (b) ppm/°C***

A comparison of Figure 40 and Figure 41 (b), shows that the ppm/℃ profile for V_{REF} is lower than either V_N or V_P for the same temperature range. Because the data were acquired at a few temperature points it is very coarse figure. But these figures show that it is possible to combine the complimentary behavior of a diode connected PMOS and NMOS to achieve a better more stable voltage reference.

The initial thermal sweep was also completed for various SG references as well the ELT references. Again, a few more iterations had to be made to each reference, which shows that the consistency and variability were not as good as expected from simulation. The term variability refers to the repeated thermal and electrical behavior from a single reference from IC to IC (i.e. how well does SG03_REF1 resemble SG12_REF1). The term consistency refers to how well the references matched on the same IC (i.e. how well does SG03_REF1 match SG03_REF4). A few ELT references were calibrated and the thermal sweeps for both V_N and V_P can be seen in Figure 42 and similarly the ppm/℃ can be seen in Figure 43.

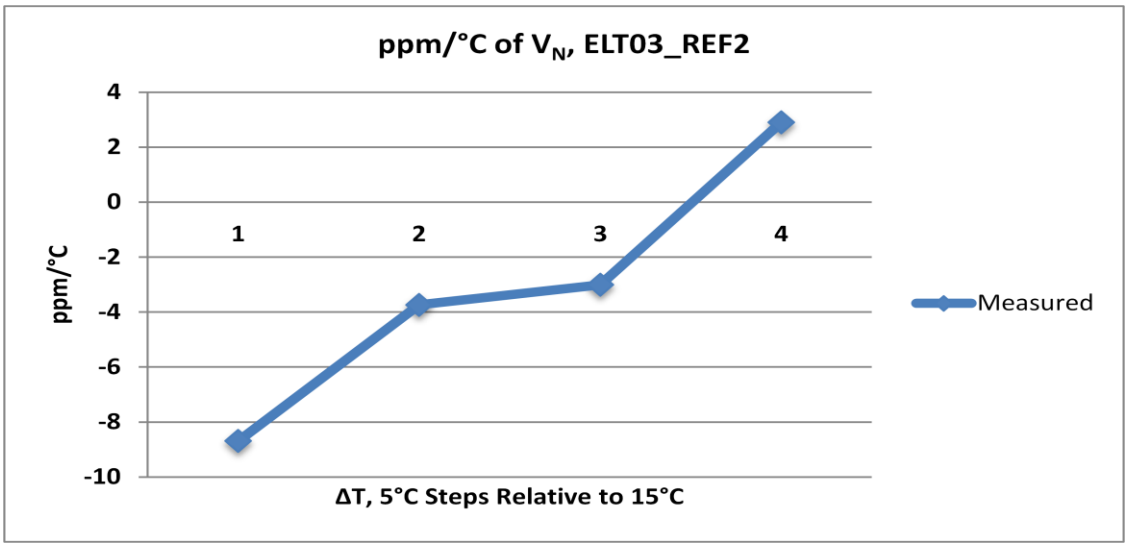


(a)

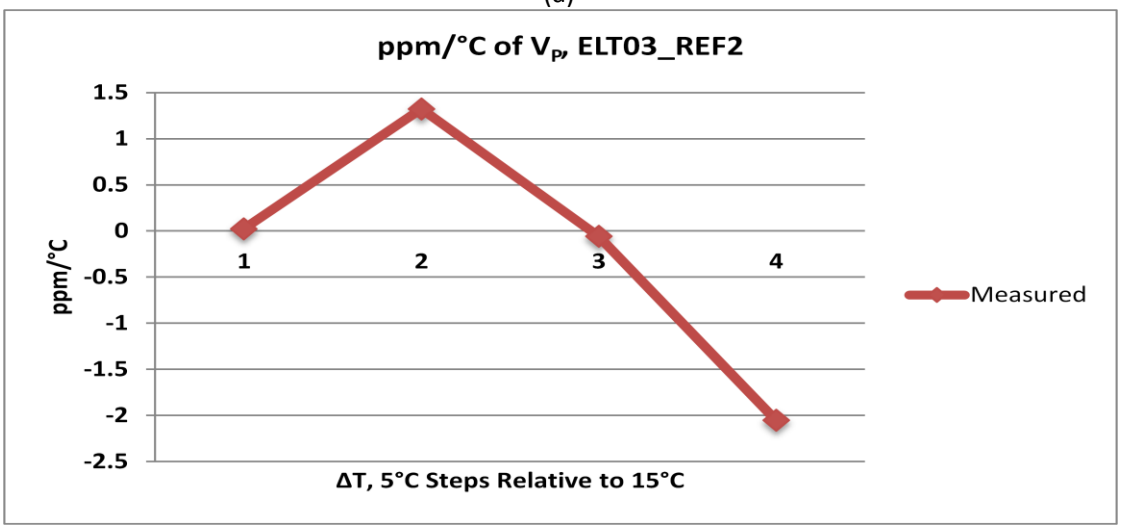


(b)

Figure 42: ***Measured Thermal Profiles from ELT03_REF2 for (a) V_N and (b) V_P***



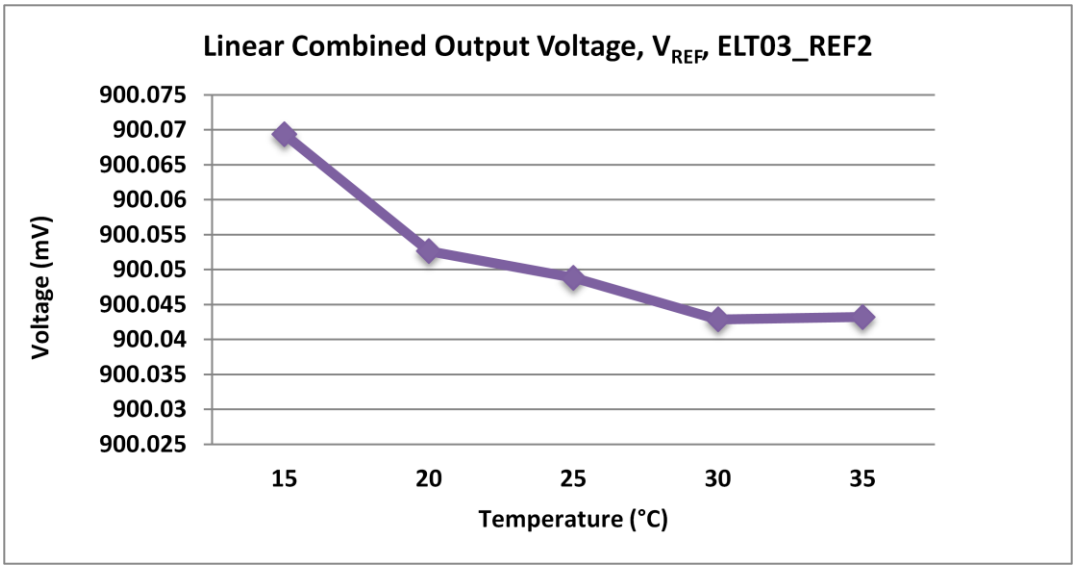
(a)



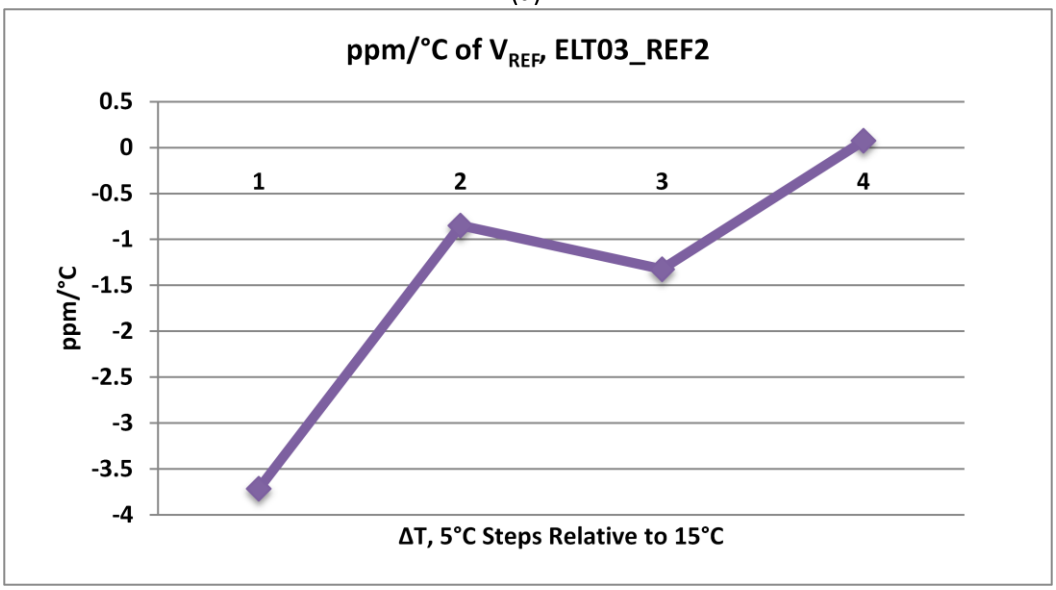
(b)

Figure 43: ***ppm/°C of Thermal Profiles from ELT03_REF2 for (a) V_N and (b) V_P***

The same criteria was used to determine X and Y for the ELT reference. The values of X and Y for ELT03_REF2 were found to be X = 0.990 and Y = 0.652. The new linearly combined ELT output voltage and ppm/°C can be seen in Figure 44.



(a)



(b)

Figure 44: ***(a) ELT Thermal Profile of Linearly Combined Output Voltage, V_{REF}, and (b) ppm/°C***

The PMOS branch of the ELT reference was not as thermally stable as its SG counterpart and those results can be seen by comparing Figure 43 and Figure 44. It is clear from the plots that it is possible to match the ppm/°C performance of a standalone output voltage but not better it as seen with

the SG reference. It is believed that this performance could be improved if there were more time for calibration and electrical/thermal testing; however there was not enough time. Now that several SG and ELT references were calibrated, their thermal profiles were acquired, and the post-processing values of X and Y were known to establish a more stable voltage reference, radiation testing could be carried out. Several ICs were tested as well as several references on each IC. There were two reasons for this: calibrating several references from different ICs gave us an idea of variations between references and several calibrated references were required for radiation testing.

The thermal profiles of the SG and ELT references measured followed the trends predicted by simulation results. The concept of mutually compensated mobility and threshold voltage as a foundation to a superior voltage reference was confirmed. The confirmation of this technique also showed that the ELTs functioned as SG transistors with some slight differences. The actual external resistor values (desired bias currents) for both SG and ELT references were greater than the values predicted with simulations. It was also observed that the ELT references' external resistance values were approximately 22% higher than the SG.

5.2 Radiation Testing

All radiation testing (TID testing) was done at the Gamma Cave located at the University of Massachusetts, Lowell, MA. TID testing would include a few stages, the first would be dosimetry measurements. Dosimeters were placed within the Gamma Cave, exposed to a Co_{60} source, and accurate measurements of dose rate were collected (where the DUTs will be located during TID testing). The dose rate was found to be 136 rad/s. The total dose could be calculated as a function of time and the DUTs could be measured at specific total dose levels. For all radiation testing two controls (SG IC and ELT IC)were monitored outside the Gamma Cave. Two pairs of calibrated SG and ELT ICs were used for the initial and final radiation sweep.

An initial radiation sweep was performed. This initial run was used to monitor at which accumulated dose the SG circuit functionality began to falter. The output voltages, V_N and V_P, were monitored for SG and ELT DUTs as well as their quiescent currents, I_{QSG} and I_{QELT}. It was expected that as TID damage began to affect the SG reference that the drop in threshold voltage would increase the drain current in the current generator and an increase in overall I_{QSG} would be present. Once the dose range was known when the SG references began to degrade the dose rate would be altered for the final radiation sweep. If the dose required to alter SG functionality was very high then the dose rate would be increased and vice versa if the SG functionality faltered at low dose.

The final radiation run was carried out in a similar way. Data were collected from the DUTs and the thermistor present in between the DUTs. The thermal characteristics close to the DUT were important in explaining any abnormalities due to large temperature swings during exposure. A MATLAB script was used to collect data and was very similar to data collection for electrical/thermal tests;

however there were slight modifications to the TID test MATLAB scripts. Firstly, instead of collecting data for a range of temperatures data were collected for range of radiation points. Secondly, for the DUTs in the gamma cave a single DMM was used to eliminate deviations from instrument to instrument. Finally, the data were collected after a user pressed enter on the laptop. This was necessary because we did not have access to an instrument in the test bed that monitored how much dose had been accumulated. The data were also collected in an infinite while loop until ended by the user.

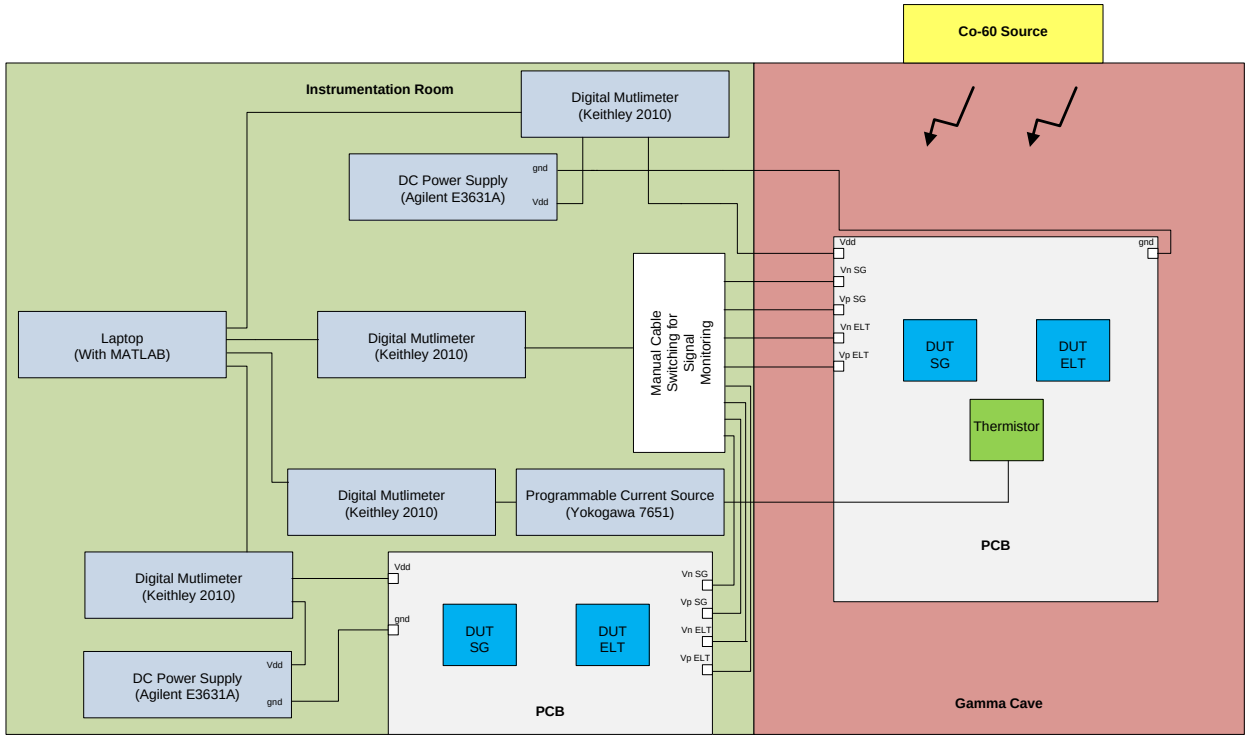


Figure 45: ***Conceptual Test Schematic for Radiation Testing***

5.2.1 TID Test Results

This initial radiation sweep took a few hours to complete. It was found that the neither the SG or ELT references experienced significant degradation when exposed to relatively low dose. Due to this finding the range of TID was increased for the final radiation sweep. Data were collected for the output voltages and were recorded; the values of X and Y used for the SG and ELT references found previously were used for both control parts and for the two DUTs respectively. The output voltage of the linearly combined V_N and V_P, V_{REF}, was calculated in MATLAB and the results can be seen in Figure 46.

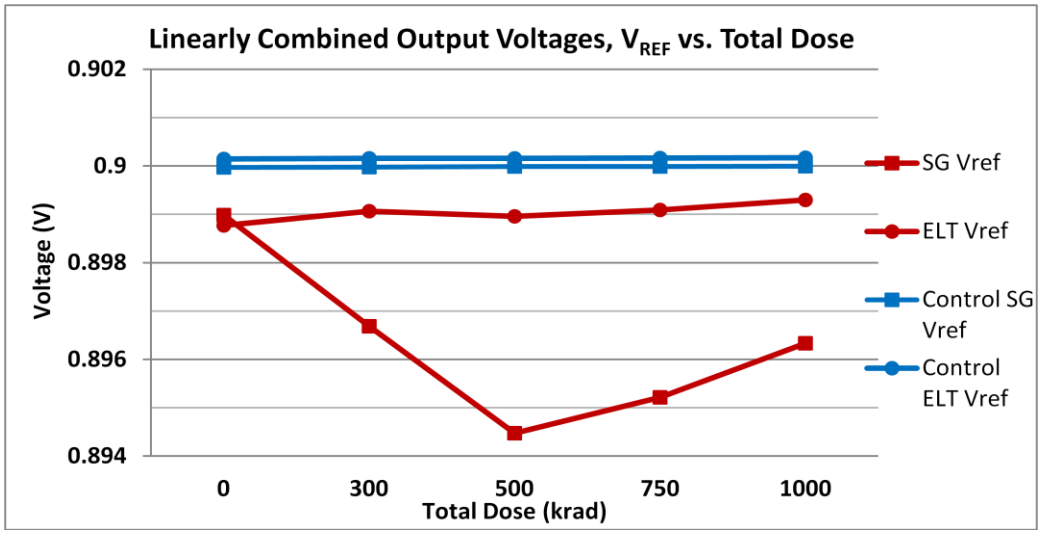


Figure 46: ***Output Voltages for Control and DUTs for Varying Total Dose***

The results from Figure 46 show that as expected the reference that used ELT NMOS devices was less susceptible to TID damage. Evaluating all references with their respective X and Y values showed the overall behavior of each reference with increasing dose. It is clear that very early on the SG DUT was susceptible to TID damage. The SG DUT was an order of magnitude off from its mean, while the ELT DUT showed little to no effect from increasing TID.

It should be noted that degradation of the SG DUT was governed by significant deviations in the quiescent current. In the initial radiation sweep there was some increase in quiescent current from the SG (more so than the ELT DUT) but not an appreciable amount. Because of this the range of radiation was increased (as mentioned previously). A significant increase in the quiescent current was not observed, but this can be explained. For each DUT, there were only two references being tested for the radiation sweep; it was noted after radiation testing that the other three references found on each DUT were not turned off. This could have been possible by using a very high external resistance for references not under test but exposed to radiation. Because the other three references were drawing current the increase in quiescent current had to be attributed to all references in operation. In future work it would be important to isolate the reference under test for each DUT so that the true increase in quiescent current due to TID can be attributed to only the reference under test.

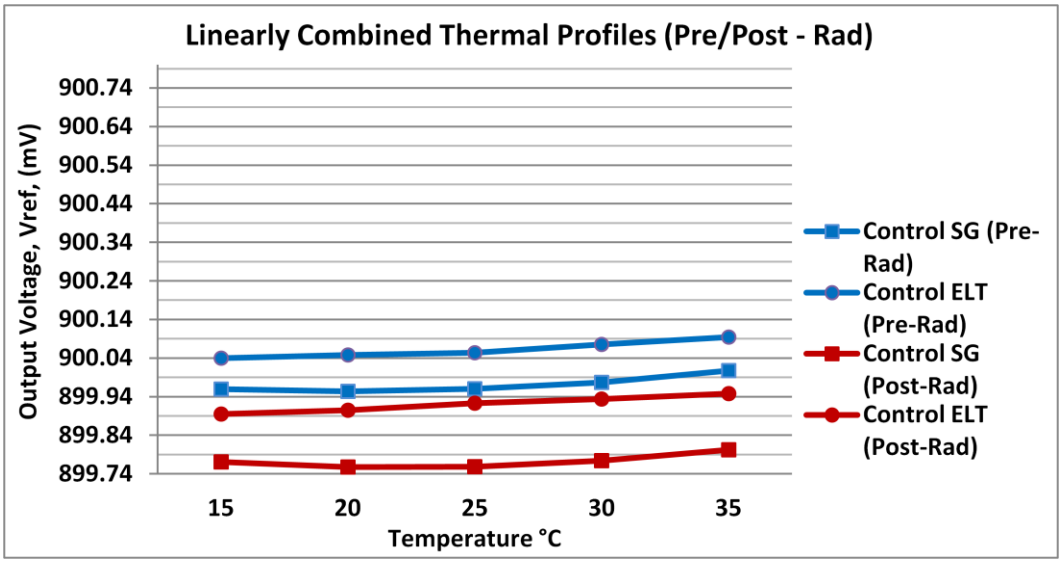
This being said it is clear from Figure 46 that the theory that an ELT NMOS greatly reduces TID damage has been confirmed. For the amount of dose introduced into the DUTs a significant shift was expected, but only mild circuit degradation was observed. This is believed to be caused by the relatively large channel length devices used in the reference design. Large channel length devices were used to eliminate channel length modulation, but this also decreases the susceptibility to TID damage. It is known that the effects of TID are complimentary to device channel length. Because large channel lengths were used, the effects of TID were less; so severe degradation was not seen in the SG DUT.

5.3 Post-Irradiation Testing

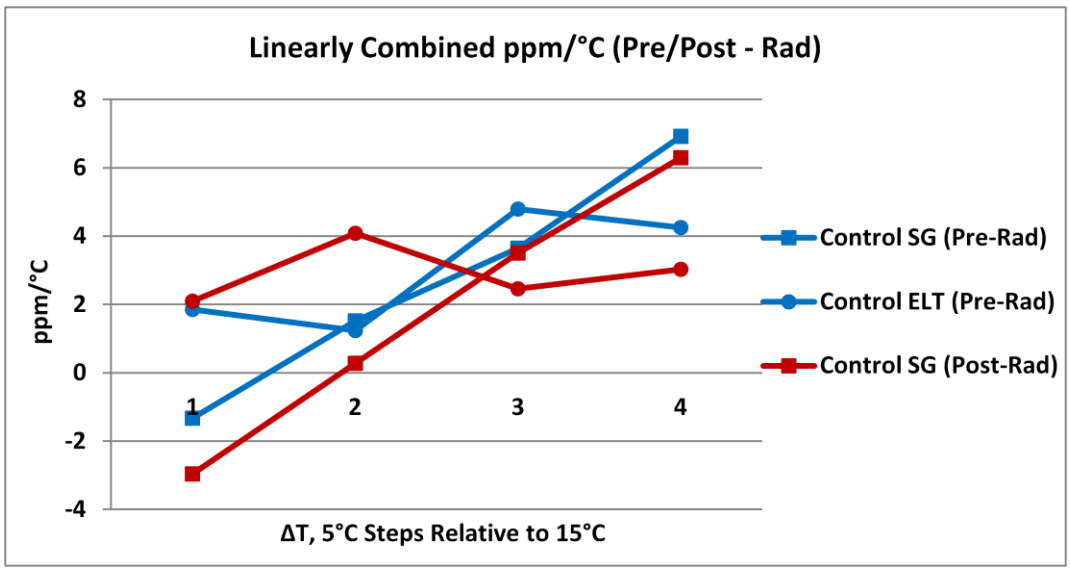
Upon completing TID testing at the test facility, post-annealing behavior for the DUTs was expected. Typically post-annealing data is collected a short time (less than 24 hours) after TID testing; however because our post-radiation testing needed to be performed at Draper Labs our post testing was performed after 72 hours. Post radiation testing involved performing the same thermal sweeps for all control references and DUTs for the same temperature range used pre irradiation. The same values of X and Y were used for each reference for post irradiation testing. This was done to normalize V_{REF} for all tests including pre irradiation and TID testing. The external resistances for all references were not altered and the same PCB used for pre irradiation testing was used to test the DUTs exposed to TID damage.

5.3.1 Post-Irradiation Test Results

The control parts used for TID testing were not exposed to any radiation and were expected to show little to no change in their pre/post irradiation thermal sweeps. The results for the post irradiation sweeps can be seen in Figure 46.



(a)



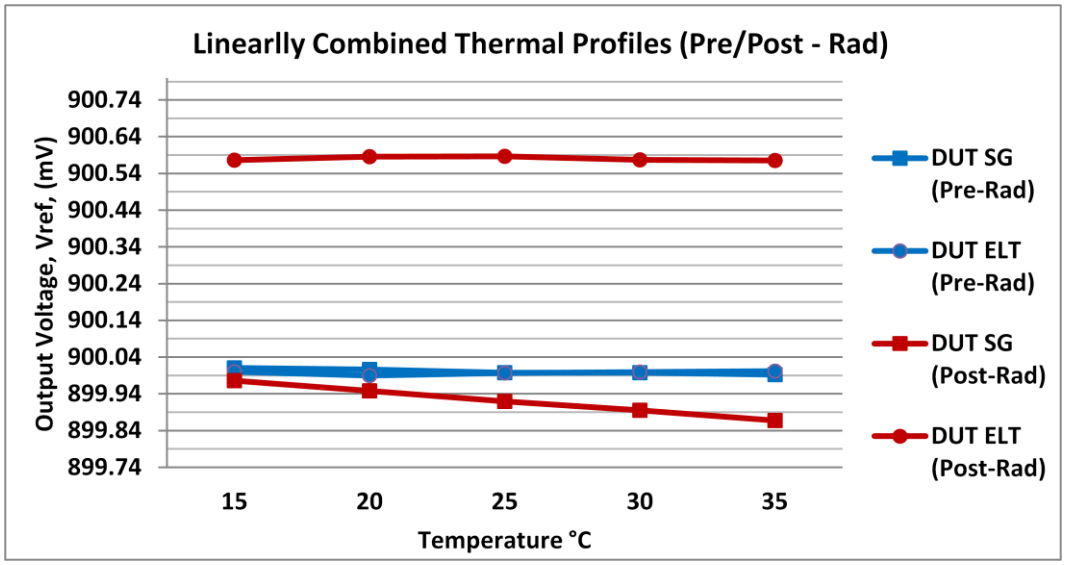
(b)

Figure 47: ***Pre/Post Irradiation Thermal Sweeps of Control Parts (a) Voltage (b) ppm/°C***

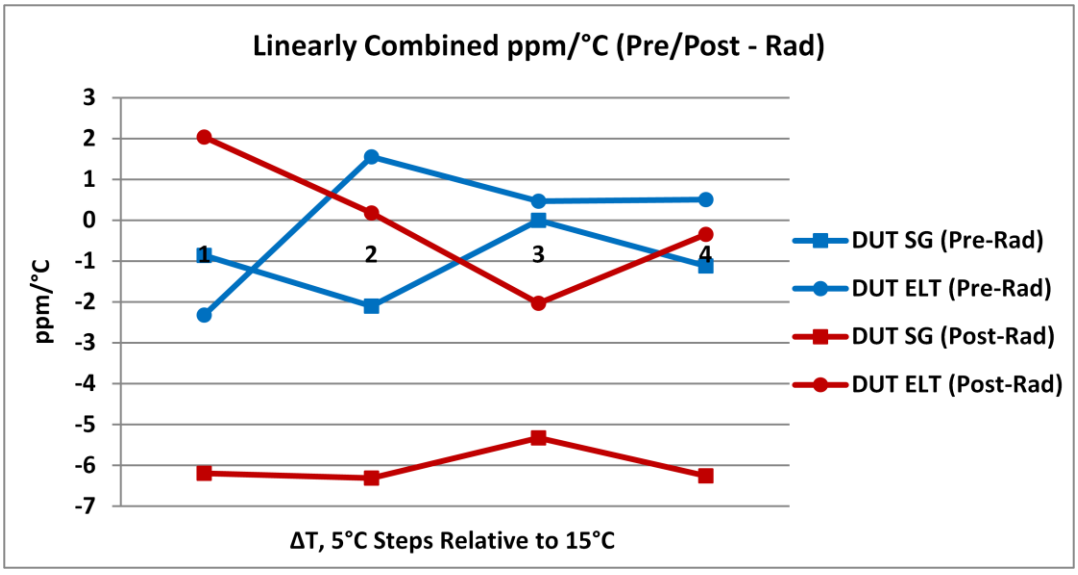
The small deviations in the ppm/°C for pre and post irradiation results are well within the measurement error for the test. It is clear that post irradiation measurements for both the voltage and

ppm/°C are for the most part identical to that of the pre irradiation measurements. The results for the DUTs are slightly different and telling to the effects of TID on SG NMOS devices.

The post irradiation results for the DUTs that were exposed to dose are shown in Figure 48.



(a)



(b)

Figure 48: ***Pre/Post Irradiation Thermal Sweeps of DUTs (a) Voltage (b) ppm/°C***

A static DC shift has occurred for SG and ELT references Figure 48 (a). While the control parts showed little to no deviation in there static DC voltages (V_{REF}) this is being attributed to test setup, but the actual cause of the DC shift is still unknown. The more telling data can be seen in Figure 48 (b) in which the ppm/°C are depicted. The pre irradiation data shows that the references are operating in the desired operating point, hovering around zero ppm/°C. The ELT reference is still operating in the same region pre and post irradiation; however the SG reference is clearly operating at a different ppm/°C. While the static DC voltages have shifted during post irradiation test, the thermal profile curves of the SG and ELT references are fairly different. During post irradiation the ELT reference's saddle point did not change from pre irradiation testing; whereas the SG reference's saddle point has shifted to a new temperature. The effects of TID on the SG reference were present during TID testing and have moved the reference out of the original operating point.

The static DC shifts in thermal profiles was noticed during some of the electrical and thermal testing and during calibration. These effects are attributed to measurement and human error. Again, I believe the real data can be inferred from the ppm/°C figure and that ELT references did not shift away from their desired operating point. In future phases of this work a user controllable network could be included in the linear combination such that these DC shifts could be corrected.

6.0 Conclusion

This thesis set out to validate the technique of mutual compensation of mobility and threshold voltage in a voltage reference in a standard bulk CMOS process, as well as use ELTs to make the voltage reference RHBD. Mutually compensated mobility/threshold was implemented for both a NMOS and PMOS and the technique was confirmed with experimental results. It was shown that this it is possible to achieve a voltage reference in a standard bulk CMOS 0.18µm process using this technique. The work also confirmed that ELT devices are less susceptible to the effects of TID. The ELT devices were successful implemented into the voltage reference and demonstrated that the voltage reference could be used in the natural radiation environment.

In the post-irradiation thermal sweeps, it was noted that both DUTs exposed to radiation showed a static DC shift. While the DUTs shifted their absolute output voltage, V_{Ref}, the ETL IC's operating point did not change but the SG IC did. Again with experimental results an efficient way to linear combine the two output voltages are being investigated, but was not implemented in this work.

The highlights of this thesis are that mutual compensation of mobility threshold voltage was verified as a valid technique to produce a ZTC for a diode connected NMOS or PMOS. Furthermore, it was shown that linearly combining the complimentary thermal profiles of a diode connected NMOS and PMOS can produce a more superior voltage reference. The RHBD technique of using ELT in place of SG NMOS devices was confirmed, and it was shown empirically, that the ELT ICs were less susceptible to the effects of radiation as compared to their SG counterparts. The references were shown to be RD up to 1 Mrad.

Future Work

This research has laid the foundation for using mutual compensation of mobility and threshold voltage as an approach to creating a superior voltage reference and the necessary techniques which make RHBD. In the future, there are a few things that will have to be investigated: an accurate characterization of ELT devices for their use in analog ICs and implementing the linear combination method on chip.

Additional ICs were made fabricated such that ELTs of varying channel length could be evaluated. The intrinsic transconductance, threshold voltage, and effective aspect ratio will be extracted. More work is currently being done to characterize the effective aspect ratio for different channel length devices. By obtaining the different IV curves for varying channel length device including the one implemented for the voltage reference, a more accurate description can be obtained for ELT devices. Matching will also be investigated.

Another goal for future work will be to implement the linear combination technique will have to be designed to combine of the two output voltages on chip to make a superior voltage reference. The design to implement the linear combination will also have to be RH, and as such the proper characterization of the ELT only stands to benefit this additional goal. Once the linear combination technique has been implemented and combined with the body of this work a truly RHBD voltage reference will be realized in a standard-bulk CMOS process.

There have been many advances in making electronics less susceptible to radiation damage including RH processes and clever design techniques. Most importantly, I believe that it is essential that design techniques used to mitigate the effects of radiation become the dominant force behind making RH electronics. While it is beneficial to have RH processes in place, these foundries may not be there forever. Design and layout techniques, on the contrary, do not depend on one specific foundry but

merely the designer. Developing a comprehensive suite of RHBD analog and digital circuits, which has already begun for some companies, would be the best step towards making electronics less susceptible to radiation damage.

7.0 Appendix

Characterization of ELT devices

One of the next goals of this work is to accurately predict the effective aspect ratios of ELTs. Several ELTs, with varying channel lengths from 0.18µm through 12.0µm, were fabricated so that there process parameters k'_n and $(W/L)_{eff}$ could be extracted. A PCB was designed to test the ELTs. There are 12 ELTs on an IC, one pair of ELTs of the six different channel lengths, having pairs of the same ELT device would provide insight into matching. All ELTs shared the same source and a pin was dedicated to the gate and drain of each ELT.

During the ELT parameter extraction test, the devices were biased in the linear region results this will become apparent after analyzing the drain current see Eq. (41) . The drain current is given by

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)_{eff} \left[(V_{GS} - V_{thn})V_{DS} - \frac{V_{DS}^2}{2}\right](1 + \lambda V_{DS}) \qquad (41)$$

In the linear region $(V_{GS} - V_{thn}) \geq V_{DS}$, V_{DS} was set to be approximately 50mV for the experiments. With V_{DS} at this low value Eq. (41) can be simplified.

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)_{eff} \left[(V_{GS} - V_{thn})V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad (42)$$

By rewriting Eq. (42) we can get the IV characteristic in the form $\boldsymbol{y} = mx + b$.

$$I_D = mV_{GS} + b \tag{43}$$

Where $m = (\mu_n C_{ox} \left(\frac{W}{L}\right)_{eff} V_{DS})$ and $b = -\mu_n C_{ox} \left(\frac{W}{L}\right)_{eff} V_{DS}(V_{thn} + \frac{V_{DS}^2}{2})$**.** Taking the derivative of I_D with respect to V_{GS} we obtain the transconductance of the ELT which is only a function V_{DS}, the effective aspect ratio and the intrinsic transconductance, $\mu_n C_{OX} = k'_n$. The maximum of the derivative occurs when $V_{GS} - V_{thn}$ is approximately V_{dsat}, this value of m was used to extract the effective aspect ratio (see Eq. (44)).

$$\left(\frac{W}{L}\right)_{eff} = \frac{m_{max}}{\mu_n C_{ox} V_{DS}} \tag{44}$$

Using the value of effective aspect ratio found in Eq. (44) the x-intercept can be calculated from Eq. (43) and with it the threshold voltage (see Eq. (45)).

$$V_{thn} = -\frac{I_D}{m_{max}} + V_{GS} - \frac{V_{DS}}{2} \tag{45}$$

The experiments were performed such that the parameters of the ELT used in the voltage reference were evaluated first. The dataset included the two ELTs with the same channel length (matching) from five ICs. The drain current and gate source voltage were collected five times sequentially for a single ETL and averaged. The drain currents and gate source voltages were collected

from all ELT devices with L = 12µm and averaged again. The extracted IV curve can be seen next to the simulated IV curve in Figure 49.

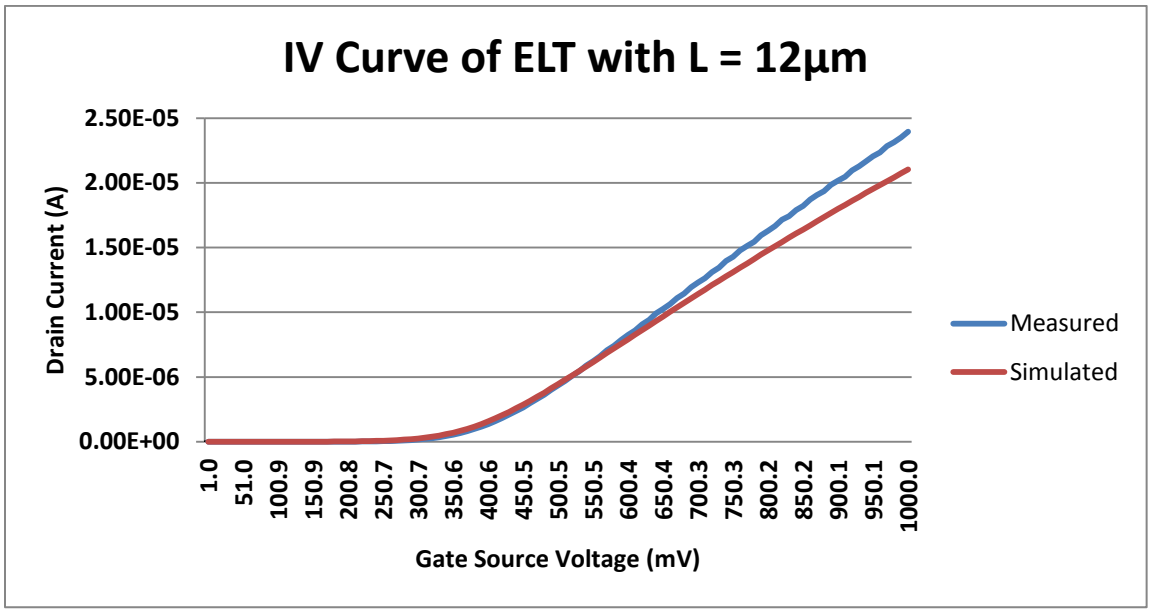


Figure 49: Measured and Simulated *IV Curves for ELT used in the Voltage Reference*

Following the procedure outlined above, the threshold voltage, V_{thn}, and effective aspect ratio, Z_{eff}, were extracted for each of the ELT used in the voltage reference. The distributions of the extracted V_{thn} and Z_{eff} can be seen in Figure 50 Figure 51.

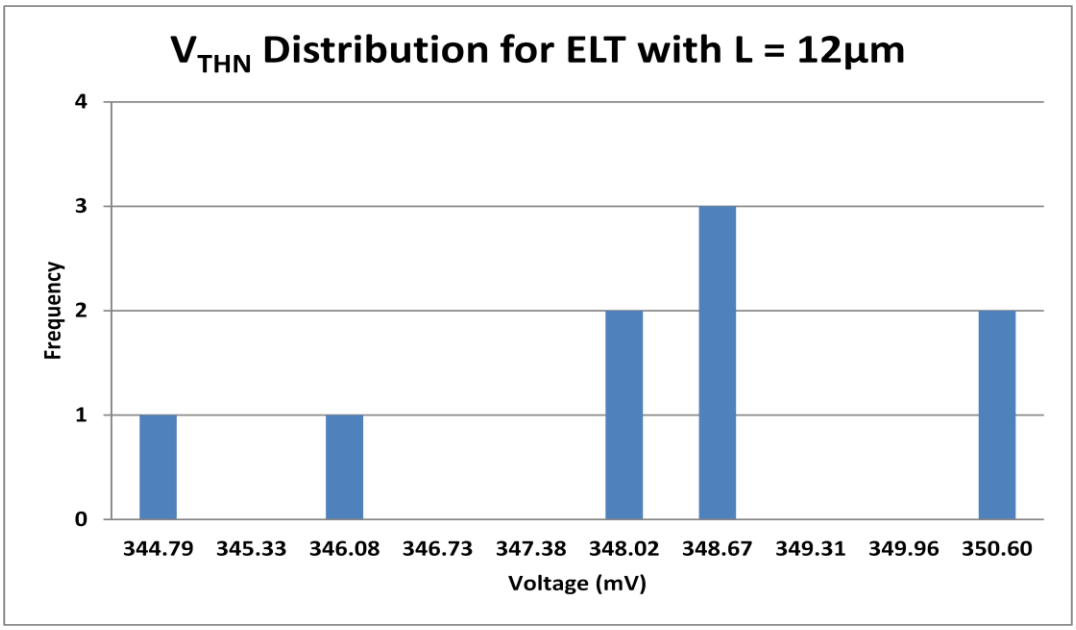


Figure 50: ***Distribution of Extracted Threshold Voltage for ELTs***

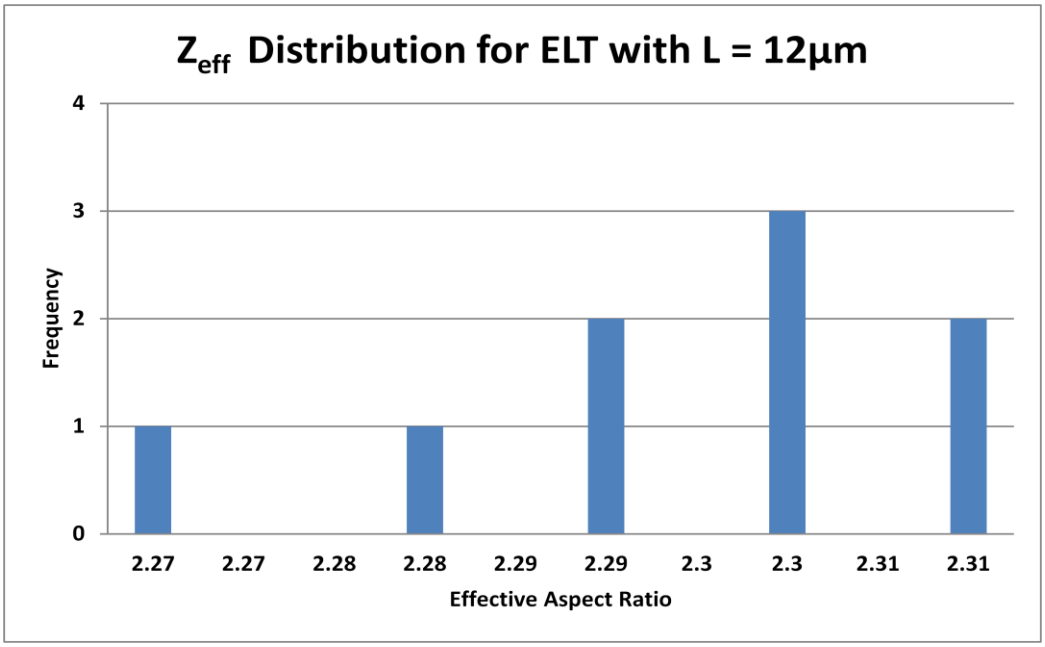


Figure 51: ***Distribution of Extracted Effective Aspect Ratio for ELTs***

Due to the small sample size the curves do not appear Gaussian. It is expected that if the sample size was higher a more accurate representation of the extracted parameters can be obtained. The extracted aspect ratio can now be compared to what was predicted by simulation (see Table 4).

Table 4: ***A Comparison of the Effective Aspect Ratios Predicted by Models to Extracted Results***

Z_{eff} **from Eq. (8)**	Z_{eff} **from Eq. (2)**	**Extracted** Z_{eff}
2.1976	1.7404	≈2.3

Preliminary analysis shows that both equations underestimated the effective aspect ratio; however the equation used to design the ELTs used for this thesis was closer to the extracted effective aspect ratio. The data presented in this section was only the ELT devices with L = 12µm. The extracted threshold voltage is approximately equal to the threshold voltage expected from the technology. The other ELT devices were also be characterized and similar comparisons will be made. After these experiments are completed a more detailed analysis will be performed comparing the different equations used to characterize the effective aspect ratio of ELTs. Matching as well as channel length modulation error can also be observed. Proper characterization of ELTs parameters are crucial if they are to be used reliably in analog ICs.

MATLAB Script Used For Data Acquisition

Electrical and Thermal Calibration Script:

Initial Calibration:

```
%% Declaring Variables N450,M1,O6,L50
clear all
%%% 100 ~ 30 seconds or .3seconds/1data point
L = 0;      % L is the number of data points for temperature readings
M = 1;       % M is the number of sets of (N point) for measuring Vn and Vp
N = 10;     % N is the number of data points during each soak interval acquired for measuring Vn
and Vp
O = 5;      % O is the number of soak intervals
             % A soak interval is approximately
             % =2*{(.3*L)+(.3*N)*M}=.6(L+N*M)(seconds)
%%%For each temperature  a soak interval will be in minutes

ps1 = E3631A_class(7);
%ps1.on;


h = 4; %%% The number of kethleys aquiring data

o_time_minutes = 38;
overnight_time= 0*o_time_minutes*60;
%overnight_time = 0;
SOAK_TIME = h*.30*(L+N*M)/60;
SOAK_INTERVAL = o_time_minutes%O*SOAK_TIME;
Tlow = 23;
Thigh = 28;
dT = 5;


T_range = Tlow

TEMP_POINTS = linspace(Tlow,Thigh,((Thigh-Tlow)/(dT))+1);
TEST_TIME = (length(TEMP_POINTS))*(SOAK_INTERVAL+SOAK_TIME)/60;
dstring=['Each for a soak interval ' num2str(SOAK_INTERVAL) '(minutes)'];
display(dstring)
dstring2=['This Experiment will take ' num2str(TEST_TIME) '(hours)'];
display(dstring2)




chm = thermotron_class(10);
chm.rst;
chm.run;
chm.set(Tlow)

tic


%%Hacked version of xxFunction_Experiment_DEBUG2
```

```
add2 = 17;  %low ppm NMOS SG
add1 = 18;  %low ppm PMOS SG
add3 = 15;  %low ppm PMOS ELT
add4 = 16;  %low ppm NMOS ELT
% Data from DMM with Address 15 --> Vout1
bigD1 = zeros(N,M);

Vout_mean1 = zeros(1,M);
Vout_std1 = zeros(1,M);

% Data from DMM with Address 16 --> Vout2
bigD2 = zeros(N,M);

Vout_mean2 = zeros(1,M);
Vout_std2 = zeros(1,M);

bigD3 = zeros(N,M);

bigD4 = zeros(N,M);

%Sweep_NMOS_mean = zeros(length(T_range),M);
%Sweep_PMOS_mean = zeros(length(T_range),M);
%Sweep_NMOS_std = zeros(length(T_range),M);
%Sweep_PMOS_std = zeros(length(T_range),M);

%%% For each temperature (length k) with delta T
%%% the means of the M runs with N samples for NMOS and PMOS
%NMOS_mean = zeros(O,length(T_range));
%PMOS_mean = zeros(O,length(T_range));
%NMOS_std = zeros(O,length(T_range));
%PMOS_std = zeros(O,length(T_range));

NMOS_RAW = zeros(length(T_range),N);
PMOS_RAW = zeros(length(T_range),N);
PMOS_ELT_RAW = zeros(length(T_range),N);
NMOS_ELT_RAW = zeros(length(T_range),N);


Vn_mean = zeros(1,length(T_range));
Vp_mean = zeros(1,length(T_range));
Vp_ELT_mean = zeros(1,length(T_range));
Vn_ELT_mean = zeros(1,length(T_range));


Big_NMOS_RAW = zeros(O,N);
Big_PMOS_RAW = zeros(O,N);
Big_NMOS_ELT_RAW = zeros(O,N);
Big_PMOS_ELT_RAW = zeros(O,N);



%DA_K2010_filter(add2)
%DA_K2010_filter(add1)
%DA_K2010_filter(add3)
%DA_K2010_filter(add4)



for kk = 1:O

    %k = 1;
    reply = input('_____________________RECORD NMOS_SG_REF5', 's');
    DA_K2010_filter_OFF(add2)
    pause(.05)
    DA_K2010_RATE_FAST(add2)
    bigD2 = Sampling(add2,N,M);%low ppm NMOS SG

    %NMOS_RAW(k,:) = bigD2';
```

```
    Big_NMOS_RAW(kk,:) = bigD2';

    reply = input('_____________________RECORD PMOS_SG_REF5', 's');
    DA_K2010_filter_OFF(add1)
    pause(.05)
   DA_K2010_RATE_FAST(add1)
    bigD1 = Sampling(add1,N,M);

    %PMOS_RAW(k,:) = bigD1';
    Big_PMOS_RAW(kk,:) = bigD1';%low ppm PMOS SG
   %%
    reply = input('_____________________RECORD PMOS_ELT_REF5', 's');
    DA_K2010_filter_OFF(add3)
    pause(.05)
   DA_K2010_RATE_FAST(add3)
    bigD3 = Sampling(add3,N,M);

    %PMOS_ELT_RAW(k,:) = bigD3';
    Big_PMOS_ELT_RAW(kk,:) = bigD3';%ELT PMOS low ppm

    reply = input('_____________________RECORD NMOS_ELT_REF5', 's');
    DA_K2010_filter_OFF(add4)
    pause(.05)
    DA_K2010_RATE_FAST(add4)
    bigD4 = Sampling(add4,N,M);

    %NMOS_ELT_RAW(k,:) = bigD4';
    Big_NMOS_ELT_RAW(kk,:) = bigD4';%ELT NMOS low ppm


    %%%%%%%%%%%%%%%%%% FOR EACH RESISTANCE!!!!!!!!!!!!!!!!!!!
    Vn_mean(kk) = mean(Big_NMOS_RAW(kk,:));
    Vp_mean(kk) = mean(Big_PMOS_RAW(kk,:));
    Vp_ELT_mean(kk) = mean(Big_PMOS_ELT_RAW(kk,:));
    Vn_ELT_mean(kk) = mean(Big_NMOS_ELT_RAW(kk,:));

  save Run_NTM_SG02_REF5_FEB2


end

    %%%%%%%%%%%%%%%%%% FOR TEMPERATURE RUNS!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
    %Vn_mean(k) = mean(NMOS_RAW(k,:));
    %Vp_mean(k) = mean(PMOS_RAW(k,:));
    %Vp_ELT_mean(k) = mean(PMOS_ELT_RAW(k,:));
    %Vn_ELT_mean(k) = mean(NMOS_ELT_RAW(k,:));


toc

Vn_mean
Vp_mean
Vp_ELT_mean
Vn_ELT_mean

save Run_NTM_SG02_REF5_FEB2


ps1.del
```

Temperature Sweeps:

```
%% Declaring Variables N450,M1,O6,L50
clear all
%%% 100 ~ 30 seconds or .3seconds/1data point
L = 0;     % L is the number of data points for temperature readings
M = 1;      % M is the number of sets of (N point) for measuring Vn and Vp
N = 450;    % N is the number of data points during each soak interval acquired for measuring Vn
and Vp
O = 1;     % O is the number of soak intervals
            % A soak interval is approximately
            % =2*{(.3*L)+(.3*N)*M}=.6(L+N*M)(seconds)
%%%For each temperature  a soak interval will be in minutes

ps1 = E3631A_class(7);
%ps1.on;


h = 4; %%% The number of kethleys aquiring data

o_time_minutes = 38;
overnight_time= o_time_minutes*60;
%overnight_time = 0;
SOAK_TIME = h*.30*(L+N*M)/60;
SOAK_INTERVAL = o_time_minutes%O*SOAK_TIME;
Tlow = 15;
Thigh = 35;
dT = 5;


T_range = linspace(Tlow,Thigh,((Thigh-Tlow)/(dT))+1)

TEMP_POINTS = linspace(Tlow,Thigh,((Thigh-Tlow)/(dT))+1);
TEST_TIME = (length(TEMP_POINTS))*(SOAK_INTERVAL+SOAK_TIME)/60;
dstring=['Each for a soak interval ' num2str(SOAK_INTERVAL) '(minutes)'];
display(dstring)
dstring2=['This Experiment will take ' num2str(TEST_TIME) '(hours)'];
display(dstring2)







chm = thermotron_class(10);
chm.rst;
chm.run;
chm.set(Tlow)

tic


%%Hacked version of xxFunction_Experiment_DEBUG2
add2 = 17;  %low ppm NMOS SG
add1 = 18;  %low ppm PMOS SG
add3 = 15;  %low ppm PMOS ELT
add4 = 16;  %low ppm NMOS ELT

%%%%<MADE CHANGE

add2 = 16;
add1 = 15;


% Data from DMM with Address 15 --> Vout1
bigD1 = zeros(N,M);


% Data from DMM with Address 16 --> Vout2
```

```
bigD2 = zeros(N,M);



NMOS_RAW = zeros(length(T_range),N);
PMOS_RAW = zeros(length(T_range),N);
PMOS_ELT_RAW = zeros(length(T_range),N);
NMOS_ELT_RAW = zeros(length(T_range),N);


Vn_mean = zeros(1,length(T_range));
Vp_mean = zeros(1,length(T_range));
Vp_ELT_mean = zeros(1,length(T_range));
Vn_ELT_mean = zeros(1,length(T_range));


Big_NMOS_RAW = zeros(O,N);
Big_PMOS_RAW = zeros(O,N);
Big_NMOS_ELT_RAW = zeros(O,N);
Big_PMOS_ELT_RAW = zeros(O,N);


for k = 1:length(T_range)

    chm.rst
    chm.run
    chm.set(T_range(k))
    pause(overnight_time)

%pause(60*30)
for kk = 1:O
    display('____________________This is run')
    k
    %k = 1;

    DA_K2010_filter_OFF(add2)
    pause(.05)
    DA_K2010_RATE_SLOW(add2)
    bigD2 = Sampling(add2,N,M);%low ppm NMOS SG

    NMOS_RAW(k,:) = bigD2';
    %Big_NMOS_RAW(kk,:) = bigD2';


    DA_K2010_filter_OFF(add1)
    pause(.05)
   DA_K2010_RATE_SLOW(add1)
    bigD1 = Sampling(add1,N,M);

    PMOS_RAW(k,:) = bigD1';
    %Big_PMOS_RAW(kk,:) = bigD1';%low ppm PMOS SG



    %%%%%%%%%%%%%%%%%% FOR EACH RESISTANCE!!!!!!!!!!!!!!!!!!!
    %Vn_mean(kk) = mean(Big_NMOS_RAW(kk,:));
    %Vp_mean(kk) = mean(Big_PMOS_RAW(kk,:));
    %%%%%%%%%%%%%%%%%% FOR TEMPERATURE RUNS!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
    Vn_mean(k) = mean(NMOS_RAW(k,:));
    Vp_mean(k) = mean(PMOS_RAW(k,:));

  save Run_Temp_Sweep_Insitu_SG02_REF5_FEB2_THIGH_SLOW_RATE



end
end
    %%%%%%%%%%%%%%%%%% FOR TEMPERATURE RUNS!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
```

```
    %Vn_mean(k) = mean(NMOS_RAW(k,:));
    %Vp_mean(k) = mean(PMOS_RAW(k,:));
    %Vp_ELT_mean(k) = mean(PMOS_ELT_RAW(k,:));
    %Vn_ELT_mean(k) = mean(NMOS_ELT_RAW(k,:));


toc

Vn_mean
Vp_mean


save Run_Temp_Sweep_Final_SG02_REF5_FEB2_THIGH_SLOW_RATE

chm.del
ps1.del
```

TID Testing Script:

```
%% Initialize Meters/Power Supplies/Yoko RAD

ps1 = E3631A_class(7);
ps1.del;
add1 = 15;     %Voltages
add2 = 18;      %Iq1
add3 = 17;      %Iq2
add4 = 1;       %Yoko
add5 = 16;      %Thermistor

DA_K2010_filter_SLOW(add1)
DA_K2010_filter_Current_FAST(add2)
DA_K2010_filter_Current_FAST(add3)
DA_K2010_filter_SLOW(add5)




display('BNC Connector Label Definitions:')
display('BNC 1 --> VDD')
display('BNC 2 --> Iq1')
display('BNC 3 --> Iq2')
display('BNC 4 --> Thermistor')
display('BNC 5 --> SG REF1 NMOS')
display('BNC 6 --> SG REF1 PMOS')
display('BNC 7-->  SG REF2 NMOS')
display('BNC 8 --> SG REF2 PMOS')
display('BNC 9 --> ELT REF1 NMOS')
display('BNC 10 --> ELT REF1 PMOS')
display('BNC 11 --> ELT REF2 NMOS')
display('BNC 12 --> ELT REF2 PMOS')
display('BNC 13 --> CTRL SG REF1 NMOS')
display('BNC 14 --> CTRL SG REF1 PMOS')
display('BNC 15 --> CTRL ELT REF1 NMOS')
display('BNC 16 --> CTRL ELT REF1 PMOS')
%%%%%%%%%%%%%%%%%%%

I = DA_Y7651(1,1);
%YOKO!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
%%%%%%%%%%%%%%%%%%%
%YOKO!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
%%%%%%%%%%%%%%%%%%%
%YOKO!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
%%%%%%%%%%%%%%%%%%%
%YOKO!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!


%% In HOUSE TID measurement Fine Run
```

```
L = 3;

I = DA_Y7651(1,1);
N = 450;
M = 1;
O = 1;
Iq1 = zeros(N,M);
Iq2 = zeros(N,M);
Iq1_RAW = zeros(O,L);
Iq2_RAW = zeros(O,L);

Mean_Iq1_RAW = zeros(O,1);
Mean_Iq2_RAW = zeros(O,1);

Temp_RAW = zeros(O,L);
Vtherm_RAW = zeros(O,L);
Res_RAW = zeros(O,L);


Mean_Temp_RAW= zeros(O,1);;
Mean_Vtherm_RAW= zeros(O,1);
Mean_Res_RAW = zeros(O,1);

    bigD1 = zeros(N,M);
    bigD2 = zeros(N,M);
    bigD3 = zeros(N,M);
    bigD4 = zeros(N,M);
    bigD5 = zeros(N,M);
    bigD6 = zeros(N,M);
    bigD7 = zeros(N,M);
    bigD8 = zeros(N,M);
    bigD9 = zeros(N,M); %%%%Xontrol Parts
    bigD10 = zeros(N,M); %%%%Xontrol Parts
    bigD11 = zeros(N,M); %%%%Xontrol Parts
    bigD12 = zeros(N,M); %%%%Xontrol Parts



Big_NMOS_REF1_RAW = zeros(O,N);
Big_PMOS_REF1_RAW = zeros(O,N);
Big_NMOS_ELT_REF1_RAW = zeros(O,N);
Big_PMOS_ELT_REF1_RAW = zeros(O,N);
Big_NMOS_REF2_RAW = zeros(O,N);
Big_PMOS_REF2_RAW = zeros(O,N);
Big_NMOS_ELT_REF2_RAW = zeros(O,N);
Big_PMOS_ELT_REF2_RAW = zeros(O,N);

CTRL_NMOS_REF1_RAW = zeros(O,N);
CTRL_PMOS_REF1_RAW = zeros(O,N);
CTRL_NMOS_ELT_REF1_RAW = zeros(O,N);
CTRL_PMOS_ELT_REF1_RAW = zeros(O,N);


Mean_NMOS_REF1_RAW = zeros(O,1);
Mean_PMOS_REF1_RAW = zeros(O,1);
Mean_NMOS_ELT_REF1_RAW = zeros(O,1);
Mean_PMOS_ELT_REF1_RAW = zeros(O,1);
Mean_NMOS_REF2_RAW = zeros(O,1);
Mean_PMOS_REF2_RAW = zeros(O,1);
Mean_NMOS_ELT_REF2_RAW = zeros(O,1);
Mean_PMOS_ELT_REF2_RAW = zeros(O,1);
Mean_CTRL_NMOS_REF1_RAW = zeros(O,1);
Mean_CTRL_PMOS_REF1_RAW = zeros(O,1);
Mean_CTRL_NMOS_ELT_REF1_RAW = zeros(O,1);
Mean_CTRL_PMOS_ELT_REF1_RAW = zeros(O,1);
%for kk = 1:O
```

```
while O>0
  kk=O;
  if kk <2
  reply = input('First Round of Dose ', 's');

  else
  reply = input('Next Round of Dose ', 's');
  end

  display('Measuring quiescent current and temperature')
  %reply = input('Record Iq from DUT 1', 's');

  Iq1 = Sampling_Current(add2,L,M);
  Iq1_RAW(kk,:) = Iq1';
  Mean_Iq1_RAW(kk) = mean(Iq1_RAW(kk,:))

  %reply = input('Record Iq from DUT 2', 's');

  Iq2 = Sampling_Current(add3,L,M);
  Iq2_RAW(kk,:) = Iq2';
  Mean_Iq2_RAW(kk) = mean(Iq2_RAW(kk,:))


  %reply = input('Record Thermistor Data', 's');
  [Vtherm,Temp,Res] = Sampling_Rate_test_2p0(add5,L,1,I);
  Vtherm_RAW(kk,:) = Vtherm;
  Temp_RAW(kk,:) = Temp;
  Res_RAW(kk,:) = Res;


  Mean_Temp_RAW(kk) = mean(Temp_RAW(kk,:))
  Mean_Vtherm_RAW(kk) = mean(Vtherm_RAW(kk,:));
  Mean_Res_RAW(kk) = mean(Res_RAW(kk,:));



  DA_K2010_filter_OFF(add1)
  reply = input('_________________RECORD NMOS_SG_REF1; BNC 5 ', 's');
  DA_K2010_filter_SLOW(add1)
  pause(.05)
  bigD2 = Sampling(add1,N,M);
  Big_NMOS_REF1_RAW(kk,:) = bigD2';


  DA_K2010_filter_OFF(add1)
  reply = input('_________________RECORD PMOS_SG_REF1; BNC 6', 's');
  DA_K2010_filter_SLOW(add1)
  pause(.05)
  bigD1 = Sampling(add1,N,M);
  Big_PMOS_REF1_RAW(kk,:) = bigD1';


  DA_K2010_filter_OFF(add1)
  reply = input('_________________RECORD NMOS_SG_REF2; BNC 7 ', 's');
  DA_K2010_filter_SLOW(add1)
  pause(.05)
  bigD6 = Sampling(add1,N,M);
  Big_NMOS_REF2_RAW(kk,:) = bigD6';

  DA_K2010_filter_OFF(add1)
  reply = input('_________________RECORD PMOS_SG_REF2; BNC 8 ', 's');
  DA_K2010_filter_SLOW(add1)
  pause(.05)
  bigD5 = Sampling(add1,N,M);
  Big_PMOS_REF2_RAW(kk,:) = bigD5';

  DA_K2010_filter_OFF(add1)
  reply = input('_________________RECORD NMOS_ELT_REF1; BNC 9', 's');
```

```
DA_K2010_filter_SLOW(add1)
pause(.05)
bigD4 = Sampling(add1,N,M);
Big_NMOS_ELT_REF1_RAW(kk,:) = bigD4';

DA_K2010_filter_OFF(add1)
reply = input('_________________RECORD PMOS_ELT_REF1; BNC 10', 's');
DA_K2010_filter_SLOW(add1)
pause(.05)
bigD3 = Sampling(add1,N,M);
Big_PMOS_ELT_REF1_RAW(kk,:) = bigD3';

DA_K2010_filter_OFF(add1)
reply = input('_________________RECORD NMOS_ELT_REF2; BNC 11 ', 's');
DA_K2010_filter_SLOW(add1)
pause(.05)
bigD8 = Sampling(add1,N,M);
Big_NMOS_ELT_REF2_RAW(kk,:) = bigD8';

DA_K2010_filter_OFF(add1)
reply = input('_________________RECORD PMOS_ELT_REF2; BNC 12 ', 's');
DA_K2010_filter_SLOW(add1)
pause(.05)
bigD7 = Sampling(add1,N,M);
Big_PMOS_ELT_REF2_RAW(kk,:) = bigD7';


DA_K2010_filter_OFF(add1)
reply = input('_________________RECORD CTRL NMOS_SG_REF1; BNC 13 ', 's');
DA_K2010_filter_SLOW(add1)
pause(.05)
bigD9 = Sampling(add1,N,M);
CTRL_NMOS_REF1_RAW(kk,:) = bigD9';

DA_K2010_filter_OFF(add1)
reply = input('_________________RECORD CTRL PMOS_SG_REF1; BNC 14 ', 's');
DA_K2010_filter_SLOW(add1)
pause(.05)
bigD10 = Sampling(add1,N,M);
CTRL_PMOS_REF1_RAW(kk,:) = bigD10';

DA_K2010_filter_OFF(add1)
reply = input('_________________RECORD CTRL NMOS_ELT_REF1; BNC 15 ', 's');
DA_K2010_filter_SLOW(add1)
pause(.05)
bigD11 = Sampling(add1,N,M);
CTRL_NMOS_ELT_REF1_RAW(kk,:) = bigD11';


DA_K2010_filter_OFF(add1)
reply = input('_________________RECORD CTRL PMOS_ELT_REF1; BNC 16 ', 's');
DA_K2010_filter_SLOW(add1)
pause(.05)
bigD12 = Sampling(add1,N,M);
CTRL_PMOS_ELT_REF1_RAW(kk,:) = bigD12';



Mean_NMOS_REF1_RAW(kk) =    mean(Big_NMOS_REF1_RAW(kk,:))
Mean_PMOS_REF1_RAW(kk) =    mean(Big_PMOS_REF1_RAW(kk,:))
Mean_NMOS_ELT_REF1_RAW(kk) = mean(Big_NMOS_ELT_REF1_RAW(kk,:))
Mean_PMOS_ELT_REF1_RAW(kk) = mean(Big_PMOS_ELT_REF1_RAW(kk,:))
Mean_NMOS_REF2_RAW(kk) =    mean(Big_NMOS_REF2_RAW(kk,:))
Mean_PMOS_REF2_RAW(kk) =    mean(Big_PMOS_REF2_RAW(kk,:))
Mean_NMOS_ELT_REF2_RAW(kk) = mean(Big_NMOS_ELT_REF2_RAW(kk,:))
Mean_PMOS_ELT_REF2_RAW(kk) = mean(Big_PMOS_ELT_REF2_RAW(kk,:))
```

```
    Mean_CTRL_NMOS_REF1_RAW(kk) =    mean(CTRL_NMOS_REF1_RAW(kk,:))
    Mean_CTRL_PMOS_REF1_RAW(kk) =    mean(CTRL_PMOS_REF1_RAW(kk,:))
    Mean_CTRL_NMOS_ELT_REF1_RAW(kk) = mean(CTRL_NMOS_ELT_REF1_RAW(kk,:))
    Mean_CTRL_PMOS_ELT_REF1_RAW(kk) = mean(CTRL_PMOS_ELT_REF1_RAW(kk,:))



    save Run_Prep_for_Insitu_Total_Dose_ICx_JAN18_


    O=O+1;
  end
%end

save Run_Prep_for_Total_Dose_ICx_JAN18
```

ELT Parameter Extraction Script:

```
%%%%%
%%% For 100 points alpha = .04 Ok
alpha = .04;    %alpha sets the threshold for when you reject an outlier
beta = 0.97;    %beta sets a weighted mean for the data points near the maximum value
% Both alpha = .04 and beta = 0.97 successfully reject the bad points and
% extract the maximum slope m.

delay = 0;      %delay is an appendix (left over variable that isn't useful and shouldn't be
touched)
                %delay sets when the algorithm kicks in


Vth_Array_12p0A = zeros(5,1);
Zeff_Array_12p0A = zeros(5,1);
Vth_Array_12p0B = zeros(5,1);
Zeff_Array_12p0B = zeros(5,1);
format long
%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%Paramter Extracrion for:
%%%%%%%%%%%%%%%%%%%%% TS2_12P0A_1
load TS2_1_12P0A_RETAKE3_1.mat   %%% Loads the data
                        %%% Nomenclature is as follows TSx_L(AorB)_Run#:
                                %x = IC name (TS1 or TS2)
                                %L = Channel Length, L (12P0,7P0,3P5, etc.
                                %(AorB) = Either A or B depending on the ELT
                                %Run# = Run name
display('With Data Manipulation [Vth, slope, Z]')
[TEST dat TEST_POLY]= ELT_Param_Extraction(data,alpha,delay,beta);% Function extracts Vth, max
slope, and Zeff.
TEST
TEST_POLY
```

Function ELT_Param_Extraction.m

```
%%% Post Processing ELT Data



function [ANS DATA ANS_poly] = ELT_Param_Extraction(data,alpha,delay,beta)

x = data(:,1);
y = data(:,2);
```

```
start = (length(data(:,1))-1)/2;
dy = diff(y)./diff(x);

dx = x(1:length(x)-1);
figure(1)
plot(x,y)
%stem(x,y, 'k')

hold on
grid on


p = polyfit(data(start:length(x),1),data(start:length(x),2),3);

x = linspace(0,1,length(x));
yp = p(1)*x.^3 + p(2)*x.^2 + p(3)*x+p(4);

%plot(x,yp, 'r')



dyp = diff(yp(start:length(x)))./diff(x(start:length(x)));


figure(2)

title('dId/dVgs')
grid on




dy_mod = dy;
MEAN_pre = mean(dy_mod(start:length(dx)));
MEAN = mean(dy(start:length(dx)));

for h = start+delay:length(dx)

    if dy_mod(h-1) > beta*MEAN  % Makes sure that the point of reference for the comparison below
is not a stray point

    else
    % Comparison of previous points
        if abs(dy_mod(h)-dy_mod(h-1))/dy_mod(h-1) > alpha*dy_mod(h)/dy_mod(h-1) %If the current
point dy_mod(h) is greater than the absolute change times some factor then the current point is
replaced by the previous point
            dy_mod(h) = dy_mod(h-1);
            c_prime = h;
        else
            dy_mod(h) = dy(h);  % If the points are close enough then we allow the point to exist
        end
     end
end

p = polyfit(data(start:length(dx),1),dy_mod(start:length(dy)),3);

x = linspace(0,1,length(dx));
yp_mod = p(1)*x.^3 + p(2)*x.^2 + p(3)*x +p(4);

MEAN

stem(dx,dy, 'k')
hold on
stem(dx,dy_mod,'r')
grid on
hold on
stem(dx,yp_mod, 'g')
legend('Data', 'Modified Data')
```

```
[m_manip,c] = max(dy_mod(start+delay:length(dx)));
c = c+start-1;
Vgs_manip = x(c)
I_manip = y(c)
z = data(:,3);
Vds_manip = z(c)

[m_manip_poly, c_manip_poly] = max(yp_mod(start:length(dx)));
c_manip_poly = c_manip_poly+start-1;
Vgs_manip_poly = x(c_manip_poly)
I_manip_poly = y(c_manip_poly)
z = data(:,3);
Vds_manip_poly = z(c_manip_poly)

display('With Data Manipulation2 [Vth, slope, Z]')
Vth_manip = -I_manip/m_manip + Vgs_manip -Vds_manip/2;
Vth_manip_poly = -I_manip_poly/m_manip_poly + Vgs_manip_poly -Vds_manip_poly/2;
%%%% MOSIS has k'n to be a little off ueff = 408.42 cm^2/V*s, tox = 4.5nm
Zeff_manip = m_manip/(313.38e-6*Vds_manip);
Zeff_manip_poly = m_manip_poly/(313.38e-6*Vds_manip_poly);

ANS = [Vth_manip, m_manip, Zeff_manip];
DATA = [dy_mod];
ANS_poly = [Vth_manip_poly, m_manip_poly, Zeff_manip_poly];

mean(dy_mod);
MEAN_pre;
```

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