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Article

0.5 µW Sub-Threshold Operational Transconductance Amplifiers Using 0.15 µm Fully Depleted Silicon-on-Insulator (FDSOI) Process

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Abstract: We present a low voltage, low power operational transconductance amplifier (OTA) designed using a Fully Depleted Silicon-on-Insulator (FDSOI) process. For very low voltage application down to 0.5 V, two-stage miller-compensated OTAs with both p-channel MOSFET (PMOS) and n-channel MOSFET (NMOS) differential input have been investigated in a FDSOI complementary metal oxide semiconductor (CMOS) 150 nm process, using 0.5 V threshold transistors. Both differential input OTAs have been designed to operate from the standard 1.5 V down to 0.5 V with appropriate trade-offs in gain and bandwidth. The NMOS input OTA has a simulated gain/3 dB-bandwidth/power metric of 9.6 dB/39.6 KHz/0.48 µW at 0.6 V and 46.6 dB/45.01 KHz/10.8 µW at 1.5 V. The PMOS input OTA has a simulated metric of 19.7 dB/18.3 KHz/0.42 µW at 0.4 V and 53 dB/1.4 KHz/1.6 µW at 1.5 V with a bias current of 125 nA. The fabricated OTAs have been tested and verified with unity-gain configuration down to a 0.5 V supply voltage. Comparison with bulk process, namely the IBM 180 nm node is provided and with relevant discussion on the use of FDSOI process for low voltage analog design.

Keywords: sub-threshold; weak inversion; analog design; OTA; low power; FDSOI

1. Introduction

The growth in the area of portable biosensors, handheld wireless devices and implanted medical devices has created more interest in low power circuits [1]. Advances in CMOS technology have allowed for lower dynamic power dissipation, higher speed of operation, higher density and many other advantages. Silicon-On-Insulator (SOI) technology is being proposed as the next node in the design of low power digital Very Large Scale Integration (VLSI) circuits. This technology allows for further decrease in power and thus heat dissipation by, first, extending the trend in minimizing the voltage supply and, second, by reducing the capacitance; as the insulated localized "body" reduces the capacitance and thus minimizes the required charge to create the channel. These two benefits lower the dynamic power, which for digital circuits is approximately proportional to CV^2f, where C is the sum total of all the capacitances in the circuit, V is the power supply, and f is the frequency of operation. We also expect that these benefits will carry over to analog circuits if appropriate analog-favorable options such as high transconductance, higher output impedance, *etc*. can be provided in these processes; thus eventually allowing one to achieve a mixed-signal system on chip (SoC) solutions.

Whereas the devices in the standard bulk CMOS process are fabricated on the silicon bulk/substrate, the devices in the SOI are fabricated on a thinner silicon layer, which is separated from the bulk by an insulation layer. The main advantage will be the reduced capacitance, hence increased speed, and reduced coupling or interference through the substrate that reduces overall noise. Low power amplifiers in standard SOI processes have been demonstrated in previous studies [2,3]. The SOI process comes in two types: the partially depleted SOI (PDSOI) process and the fully depleted SOI (FDSOI) process.

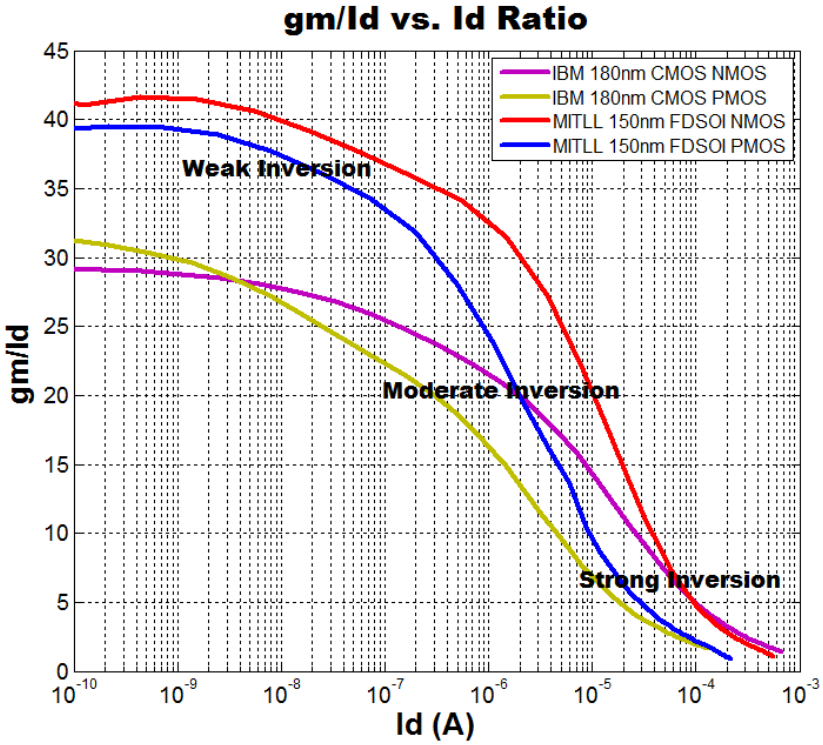
In FDSOI, the top silicon layer is much thinner than in PDSOI (<100 nm *vs.* >100 nm). The PDSOI process also exhibits a floating body effect, as the region under the channel is partially depleted of charges, leading to some charge accumulation. Since the body is not connected to any potential, the accumulated charge alters the threshold voltage of the devices and could result in transistors exhibiting large threshold voltage variation within the same die. In FDSOI, the thinness of the silicon under the channels results in full depletion and no charge accumulation, and while the body is still floating, the effect on the threshold voltages of the transistor is uniform across the die. This makes FDSOI an ideal choice for analog circuitry where process variations can result in high offsets or common mode noise.

Both processes have been optimized and brought to market for digital designs. In such designs, where one cares merely whether the switch is turned on or off, the floating body or a kink effect in such SOI processes causes only minor degradation, such as a shift in threshold voltage. This may limit the speed of operation of the device by affecting the delay of the logic cell and may affect the noise margin [4]. However simple design approaches suffice to mitigate such issues in digital applications. In analog design such shifts may result in non-linearity effects, noise degradation and dynamic range especially in low voltage implementations where voltage headroom is not sufficient.

FDSOI is now also an analog compatible process as diodes, capacitors and resistors are part of the available technology. Given that not much has been studied in terms of analog design, we are planning on studying basic analog blocks in such a process. Furthermore, these processes are being optimized for very low supply voltages for both digital and analog circuitry. Low power applications such as biomedical implantable devices and others applications require high energy efficiency and operating the transistors in saturation region is not too favorable. Sub-threshold region or weak inversion region provides the best option for the highest energy efficiency when the frequency or bandwidth is not an important requirement [5].

Besides the benefits of supply voltage and thus power reduction in weak inversion operation, sub-threshold operation can also provide the highest transconductance (g_m) for a given drain current [6]. For the chosen process, as well as the IBM 180 nm node, we observe a high number of g_m/I_d in weak inversion, as shown in Figure 1. The IBM 180 nm process was chosen as this technology has already been validated for analog design in the sub-threshold operation with conventional bulk devices [7]. Given the benefits of sub-threshold operation, our focus in this paper is on verifying its suitability in realizing a two stage operational amplifiers with ultra-low power of less than 0.5 µW in a sub-threshold region optimized 150 nm FDSOI CMOS digital process.

Figure 1. g_m/I_d curve of PMOS and NMOS devices for MITLL 150 nm FDSOI and IBM CMOS 180 nm.



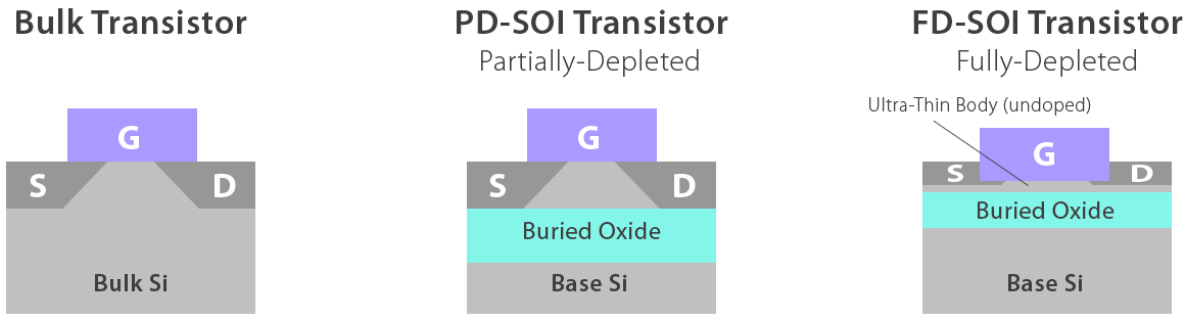
2. Analysis and Simulation Results

2.1. FDSOI vs. *PDSOI* vs. *Bulk Process*

Analog design has been proven robust in standard digital bulk processes for decades, but as the technology migrates to Partially Depleted Silicon-on-Insulator (PDSOI) and then onto FDSOI, an

investigation of the merits of FDSOI for analog amplifiers is timely. The merits of the technology are many, from the proven shrinking of the CMOS device, the lower leakage current, less short channel effects (SCE), lower expected V_{th} variations due to lower dopant fluctuations, lower voltage supply and thus lower expected power consumptions. Figure 2 below displays the comparison between bulk PDSOI and FDSOI.

Figure 2. Comparison between bulk PDSOI and FDSOI silicon processes [8].



When compared to the PDSOI technology, the FDSOI process is free of the floating body effect and has higher immunity to the kink effect. The kink effect which is due to impact ionization can be observed when a discontinuity occurs in the Ids *vs.* V_{ds} curve for higher V_{ds} voltages in strong inversion, where the current increases at a faster rate beyond a certain V_{ds} [4]. This is due to an increase in the body potential, and hence it is more prevalent in PDSOI than in FDSOI. The kink effect needs to be considered in analog design as it may contribute to device V_{th} mismatch. With SOI, smaller junction capacitance results in lower leakage current, due to less junction area and the non-existence of a leakage path to the substrate as the bulk is separated from the device by an oxide layer. Steep sub-threshold slope for high gain (and energy efficiency) may therefore be achieved in the FDSOI process which is impossible in the standard bulk process due to the inherent body effect.

Simulation results were carried out to evaluate the benefit of the MITLL FDSOI XLP 150 nm node process when compared to IBM's Bulk process at the 180 nm node. The threshold voltages were found to be 0.22 V for the NMOS and 0.27 V for the PMOS in the bulk IBM 180 nm process and approximately 0.45 V–0.5 V in the FDSOI process. This digital process was of interest as, not only was it capable of ultra-low power operation, but it came with available resistors and capacitors that made the biasing and compensation of analog cells possible. The process also claimed an "anomalously steep sub-threshold slope" [9] and the kink effect was only present above a V_{ds} of 1.1 V. Keeping devices below that bias voltage could thus minimize any kink effects. The sub-threshold slope and the g_m/I_d ratios were compared for both PMOS and NMOS devices. Both NMOS and PMOS device used have a width of 5 µm and a length of 1 µm. Minimum lengths were avoided to mitigate some short channel effects and because core analog blocks rarely rely on minimum length for matching purposes. From Figure 1, the g_m/I_d of the FDSOI process is maximized for weak inversion with a max ratio of approx. 42; which is much higher than in the strong inversion region where the g_m/I_d varies between 1 and 10 ($V_{gs} - V_{th} > 0.1$ V). When comparing to IBM's 180 nm bulk CMOS process, the g_m/I_d ratio for very low I_d is 28 for the NMOS and 32 for the PMOS. As displayed in Figure 1, the

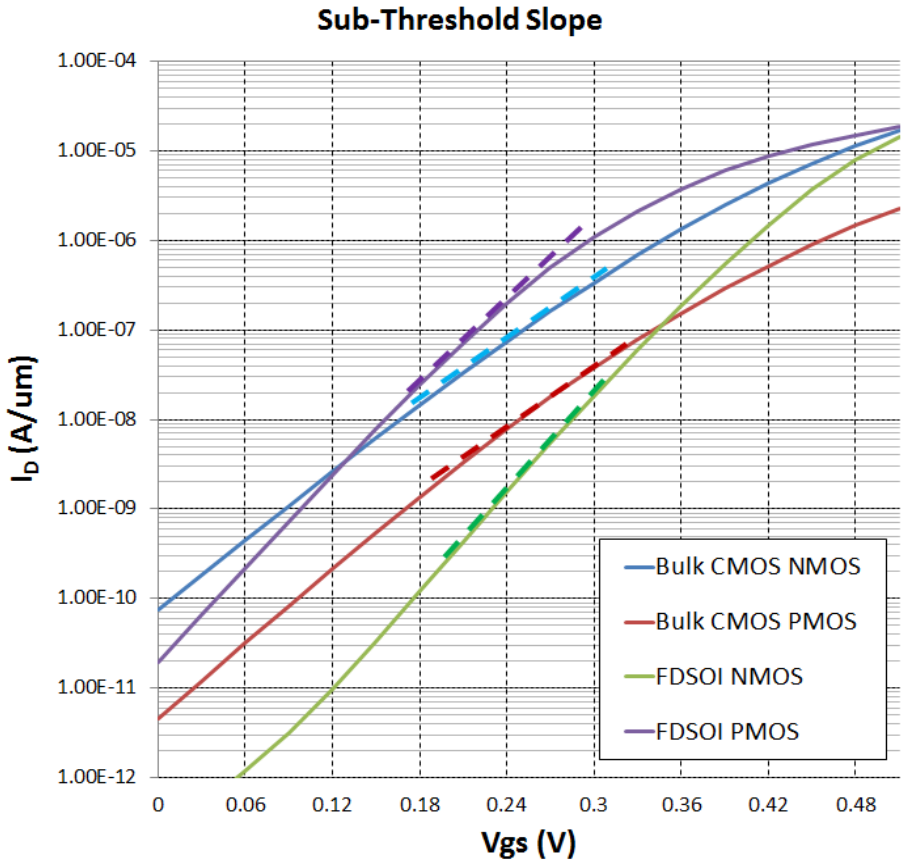
FDSOI process proves to be superior at very low I_d for both MOS devices that makes it an excellent choice for very low power application.

The sub-threshold slope factor is a significant parameter for the weak inversion operation of a device in the intended V range of operation. Its theoretical lower limit is 60 mV/dec, the slope factor *S* can be obtained in the following way [10]:

$$S = \ln 10 \cdot (dV_{gs} / d \ln I_d) \quad (1)$$

At very low V_{gs} of 0.25 V, the slope of the FDSOI process is 50 mV/dev for the NMOS and 52 mV/dev for the PMOS device. For the Bulk process, it is found to be 82 mV/dev for both of the NMOS and the PMOS device. Figure 3 displays the logarithmic drain current versus V_{gs}, displaying that the FDSOI process can provide a superior sub-threshold slope to the 180 nm bulk process at a supply voltage of 0.5 V. As such the FDSOI process was the right choice to investigate sub-threshold analog design.

Figure 3. Sub-threshold slope of FDSOI and Bulk CMOS devices (VDD = 0.5 V).



Other advantages of the FDSOI process include reduced crosstalk, elimination of latch-up hazards, better transistor isolation (e.g., noise immunity), lower junction capacitance, and lower source-drain leakage [6]. These are all due to the reduced coupling to the substrate, as in effect all the devices are isolated from the bulk; and the n-type and p-types devices are more isolated from each other.

The main disadvantages of the FDSOI process when compared to the bulk are the higher costs, which would come down as the process becomes mainstream, the V_T sensitivity to the silicon thickness, the higher series resistor and the floating body effects [6]. It is however important to realize

that, as with any new technology, the total cost of production comes down once the technology becomes mainstream and is being mass produced.

2.2. Design of Two-Stage Differential Pair OTAs

In this paper, our goal was to utilize this advanced FDSOI process to realize a complete operational transconductance amplifier with both PMOS and NMOS input transistors and explore the possibility of aggressively scaling its supply voltage. A PMOS differential pair as well as a NMOS differential pair, as shown in Figures 4 and 5, respectively, were designed and optimized to work in the sub-threshold region as well as in strong inversion. Simulation results point to a nominal threshold voltage of approximately 0.45 V–0.5 V for the chosen device sizes. Both designs are two-stage Miller compensated OTAs designed to operate over a 0.5 V–1.5 V range. The PMOS design has its bias current generated off chip, for fine tuning of the device on the bench for optimal operation. Its PMOS differential pair as well as the NMOS load devices use a length of 500 nm, guaranteeing a minimum of matching (proportional to $\sqrt{(W*L)}$), while minimizing the voltage of operation. The NMOS design has its bias current generated on chip with a 1 MΩ resistor to GND. Its bias is set to (VDD−VGS)/R_b for the chosen VDD. The NMOS differential pair uses a length of 450 nm and the PMOS load devices use a length of 300 nm.

Figure 4. PMOS input differential Amplifier.

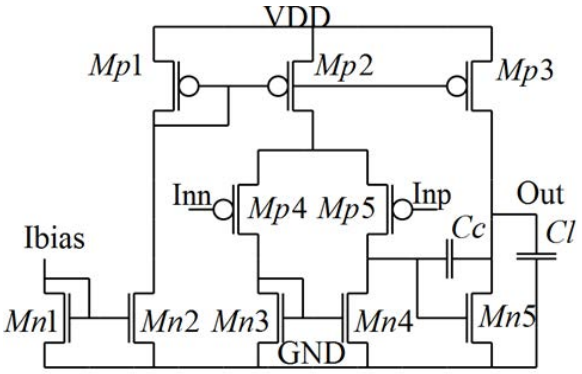
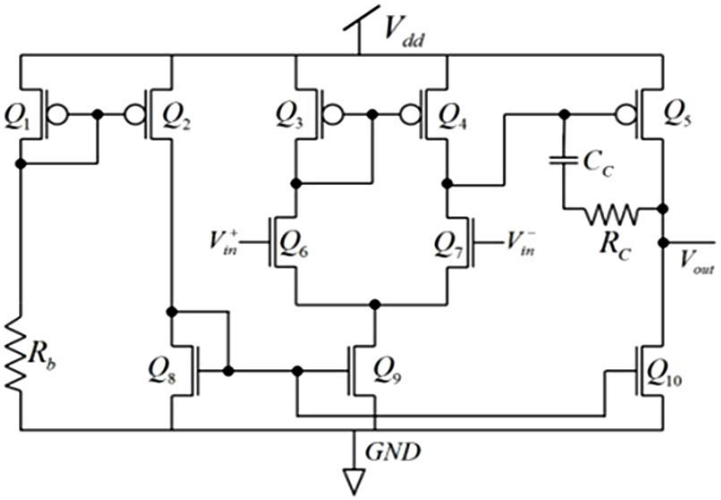


Figure 5. NMOS input differential Amplifier.



Although the minimal length for this technology is 150 nm, no devices in either amplifier used a length of less than 300 nm. This reduces channel length modulation and increases output impedance. Moreover it provides better matching (process variation is inversely proportional to the area) and minimizes short channel artifacts such as leakage and second order V_T dependencies. Only the ESD protections structure at each pin—off PMOS diode to VDD and off NMOS diode to GND—use the minimum length of 150 nm expecting these would turn on first during an ESD event. The equations of intrinsic parameters for a device in sub-threshold region with sufficient drain-source bias are as follow:

$$I_D = I_{D0}\frac{W}{L}e^{(V_{GS}-V_{Th})/nU_T},\ U_T = \frac{KT}{q},\ 1 < n < 3 \tag{2}$$

$$g_m = \frac{I_D}{nU_T},\ g_m r_o = \frac{1}{n\lambda U_T} \tag{3}$$

Leading to the gain of the OTAs to be the following [11]:

$$\begin{aligned} Avn &= g_m Q7 \cdot g_m Q5 \cdot \left(\frac{r_o Q7 \cdot r_o Q4}{r_o Q7 + r_o Q4}\right) \cdot \left(\frac{r_o Q5 \cdot r_o Q10}{r_o Q5 + r_o Q10}\right) \\ &= \frac{1}{n_{Q7} n_{Q5} \cdot (U_T)^2 \cdot (\lambda_{Q7} + \lambda_{Q4}) \cdot (\lambda_{Q5} + \lambda_{Q10})} \end{aligned} \tag{4}$$

$$\begin{aligned} Avp &= g_m MP5 \cdot g_m MN5 \cdot \left(\frac{r_o MP5 \cdot r_o MN4}{r_o MP5 + r_o MN4}\right) \cdot \left(\frac{r_o MP3 \cdot r_o MN5}{r_o MP3 + r_o MN5}\right) \\ &= \frac{1}{n_{MP5} n_{MN5} \cdot (U_T)^2 \cdot (\lambda_{MP5} + \lambda_{MN4}) \cdot (\lambda_{MP3} + \lambda_{MN5})} \end{aligned} \tag{5}$$

Since the amplifiers presented here are differential pairs, in layout all the transistors have their source local-body tied to eliminate any potential floating body effects and to ensure better matching, linearity and more stable V_T over voltage [12], thus minimizing the disadvantages of the FDSOI process from an analog design standpoint. However, we expect that even if such source–body connections were not made, that such metrics would be better than in a PDSOI process. Since these were designed to operate at ultra-low power, self-heating and temperature concerns were not important. Furthermore the kink effects are usually observed at voltages above 1 V, thus the risk of kink effect can be omitted as devices were operating below the voltage of concern and were optimized to work in sub-threshold. In essence, the technology seemed ideal for ultra-low voltage and low power operation.

2.3. Simulation Results

Both OTAs were simulated with Spectre in a Cadence environment using BSIMSOI models with various supplies for various biasing conditions. Bias current is 125 nA for PMOS differential pair OTA. Tables 1 and 2 summarize the various operating conditions. AC responses are presented in Figure 6 and transient results in Figure 7. All simulations were carried with 1 pF load.

Table 1. PMOS differential pair OTA simulation results.

VDD (V)	CM (V)	Gain (dB)	PM (deg)	−3dB BW (kHz)	Total I (µA)
1.5	0.75	53	80	1.4	1.1
1	0.5	55.8	68	4.2	1.2
0.75	0.38	52.4	70	1.4	1.1
0.5	0.2	33.7	78	9.5	1.1
0.4	0.15	19.7	92	18.3	1.05
0.35	0.15	10.1	107	10.5	1.05

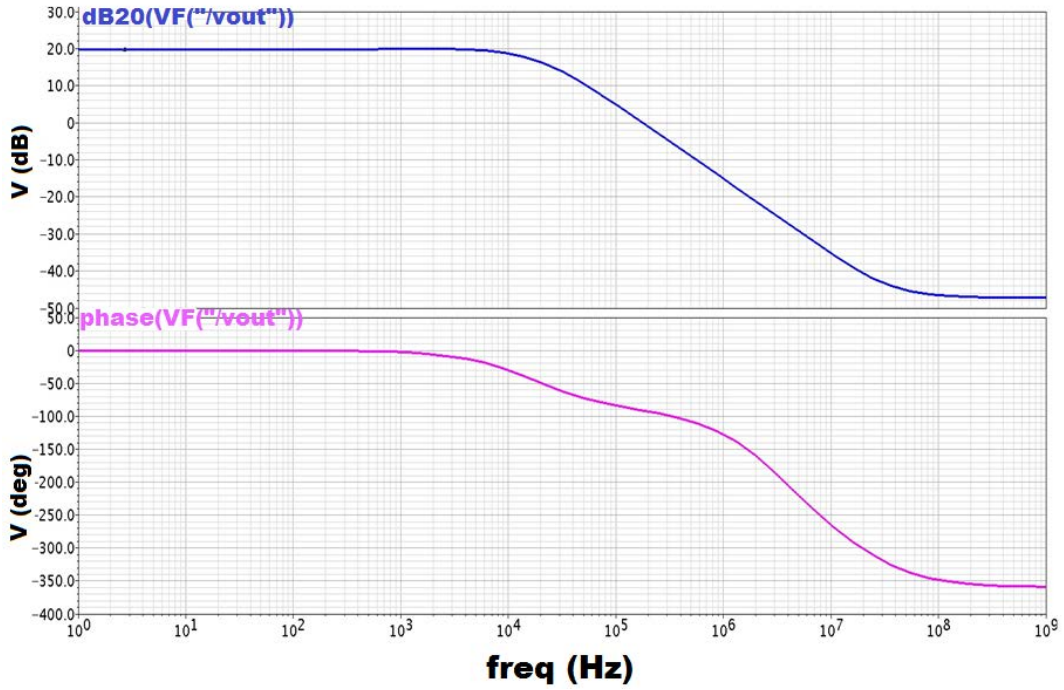
Table 2. NMOS differential pair OTA simulation results.

VDD (V)	CM (V)	Gain (dB)	PM (deg)	−3dB BW (kHz)	Total I (µA)
1.5	0.75	46.6	87	45.01	7.2
1.2	0.6	43.3	77	29.45	4.2
0.9	0.45	33	69	31.3	2.2
0.6	0.3	9.6	80	39.6	0.8

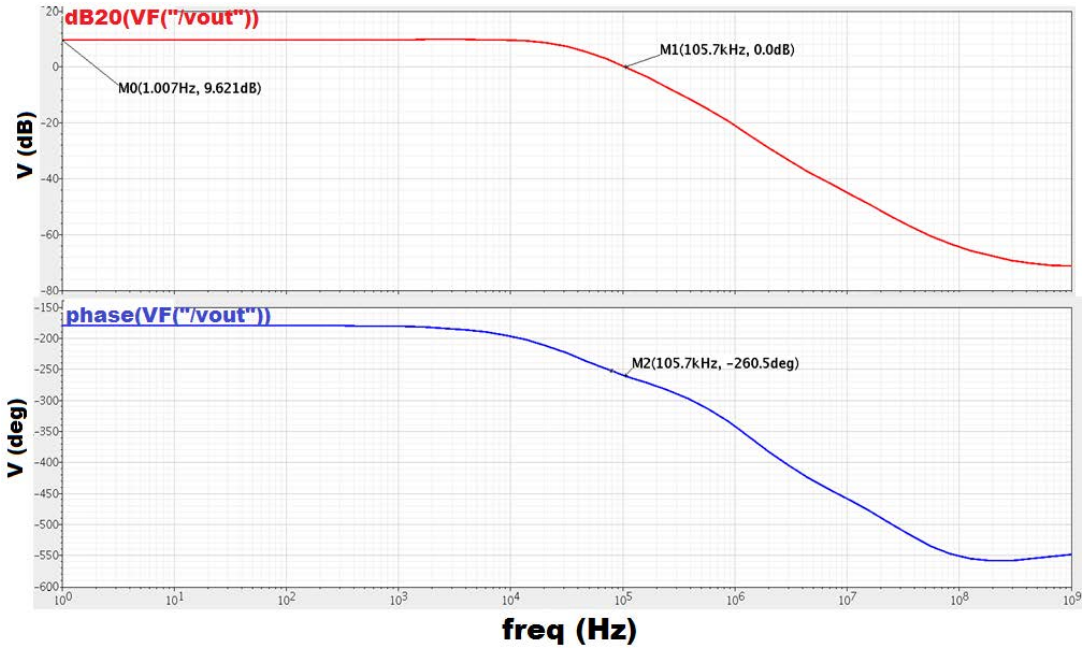
It can be observed that in both designs, the gain decreases with a decreasing supply voltage, falling drastically when the devices run out of headroom and even below the sub-threshold saturation (V_{DS} < 3 KT/q ~ 75 mV). It is also worth pointing out that for the NMOS design where the current is controlled off chip; as expected, the gain is higher for a lower current as the devices are biased further in the weak inversion region. For the lowest specified voltage and current bias, the amplifiers can reach an ultra-low power of 0.5 µW; however, the gain is relatively low in the 10 dB range. With a higher current, the gain increases to 46.6 dB for the NMOS pair amplifier and 55.8 dB for the PMOS differential pair. The results are comparable with prior work [2,3,13]. In a standard SOI process, an OTA gain of 44 dB was achieved for a power of 3.6 µW when the supply was 1.2 V [2], while in another FDSOI 180 nm implementation an OTA with a gain of 64.5 dB when the supplies were ±0.75 V for a current draw of 472 µA and a power dissipation of 708 µW was designed [13]. What is unique in this paper is that the results show that similar performance can also be achieved in a fully depleted process with potential for even lower power consumption due to better sub-threshold slope.

Neither amplifier was optimized for minimal noise contribution, as the primary goal was to drive the OTAs in deep sub-threshold while consuming ultra-low power. Noise optimization is left for a future exercise. In both designs, the main contribution of noise was flicker noise as the differential amplifier pairs are small: W/L (NMOS_OTA) = 9 µm/450 nm and W/L (PMOS_OTA) = 10 µm/500 nm. For a Supply voltage (VDD) of 1.5 V and a common voltage (V_{cm}) of 0.75 V, the input referred noise for the PMOS OTA is 89.33 nV/sqrt(Hz) for a bias current of 1 µA and it is 167.2 nV/sqrt(Hz) for a bias current of 125 nA. For a VDD of 0.5 V and a V_{cm} of 0.15 V, the input referred noise for the PMOS OTA is 99.4 nV/sqrt(Hz) for a bias current of 1uA and it is 163.3 nV/sqrt(Hz) for a bias current of 125 nA. For a VDD of 1.5 V and a V_{cm} of 0.75 V, the input referred noise for the NMOS OTA is 87.13 nV/sqrt(Hz) and it is 213.7 nV/sqrt(Hz) for a VDD of 0.6 V and a cm of 0.3 V. Noise results are reported at 10 kHz.

Figure 6. AC response (**a**) PMOS differential pair for VDD = 0.4 V, CM = 0.15 V, I bias = 125 nA; (**b**) NMOS diff pair, VDD = 0.6 V, CM = 0.3 V.

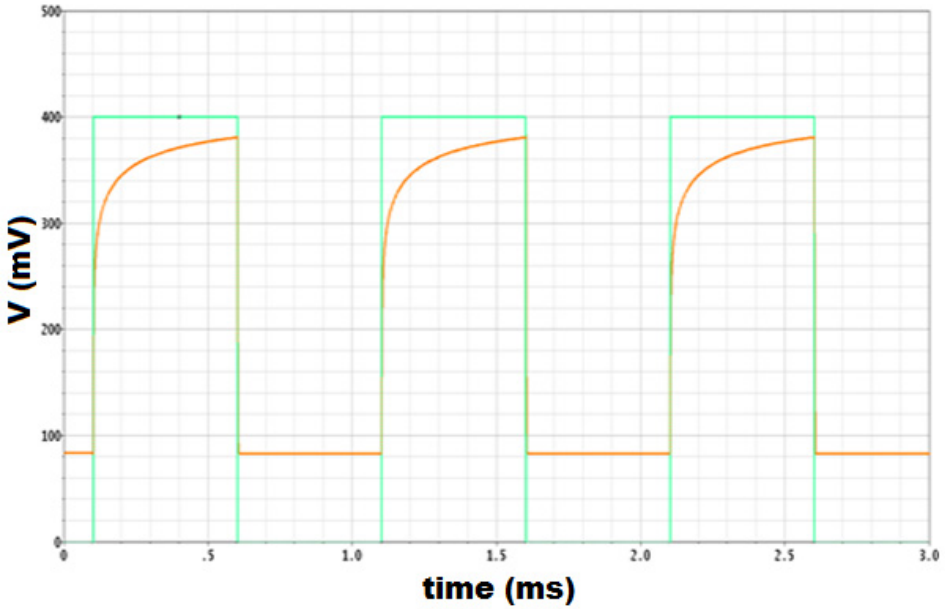


(**a**)



(**b**)

Figure 7. Transient response (**a**) PMOS amplifier; (**b**) NMOS amplifier in unity gain configuration.



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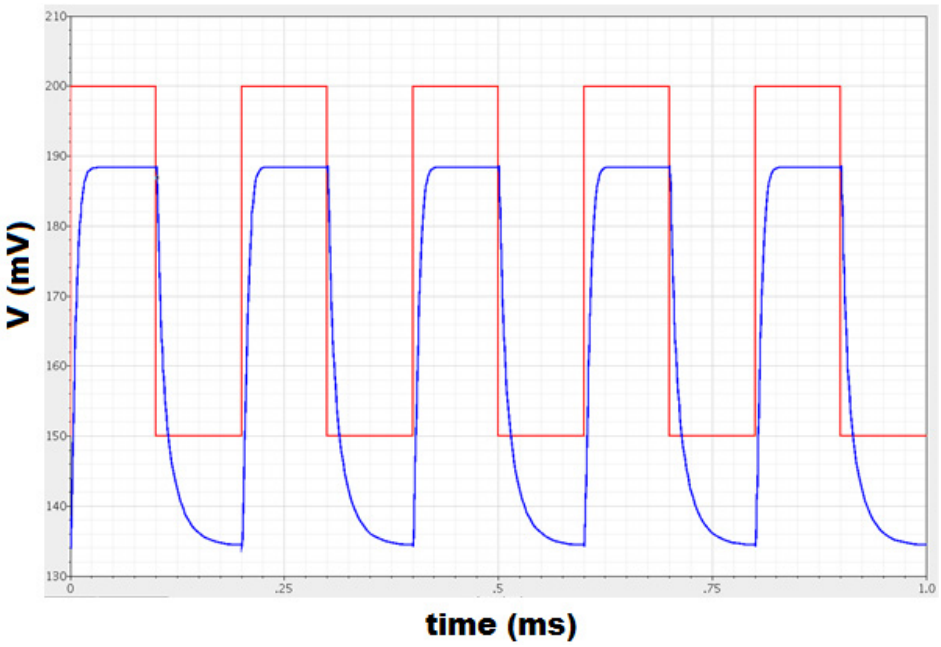


(**b**)

3. Experimental Results

Both amplifiers were fabricated on a chip in the MITLL XLP FDSOI 150 nm node. The microphotograph of the fabricated chip is displayed in Figure 8. All the pins for both amplifiers were brought out to pads, allowing for possible post processing, as well as for creating multiple configurations in the lab.

Figure 10(a) below displays transient results for the PMOS differential pair in unity gain configuration as in Figure 9, while Figure 10(b) displays the transient step response for the NMOS

differential amplifier. The observed currents are much higher than anticipated and the output becomes noisy when the supply is lowered. Both amplifiers work down to 0.6 V in the lab, offset error seems to be the cause of lower supply performance. The PMOS differential pair is being monitored by setting the bias current on the bench but working biasing currents are much higher than simulation results predict. As such it could be expected that a floating body could only further deteriorate the matching, this experiment is left for a future work. Other work in the FDSOI process have demonstrated the performance of an RF amplifier not to be degraded for lower VDD supplies when the body is left floating [14], but here the matching of the differential pairs is of primary concern. Both devices rely on capacitors for their compensation, the NMOS diff pair also relied on resistors for compensation and current generation. From the early results, it can be inferred that the capacitors and resistors worked well and suggests that the MITLL 150 nm SOI process is an analog design compatible process. The observed offset and poor yield of functional devices led us to conclude that much needs to be done to optimize this process for predictable and stable analog operation.

Figure 8. Microphotograph of the entire chip (2 mm × 2 mm).

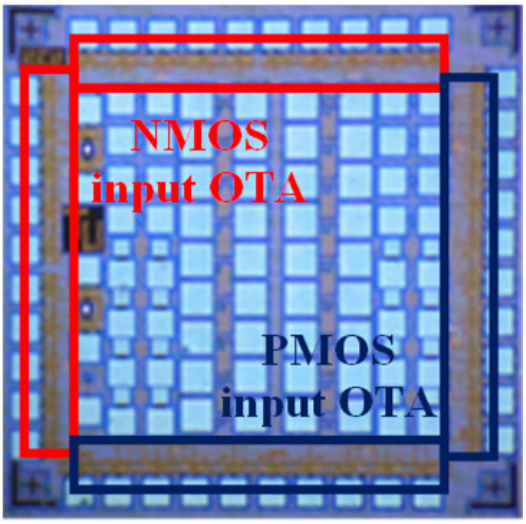


Figure 9. Schematic of Unity-Gain buffer configuration for test set-up.

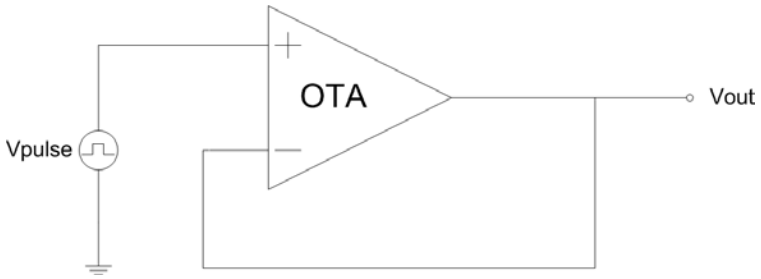
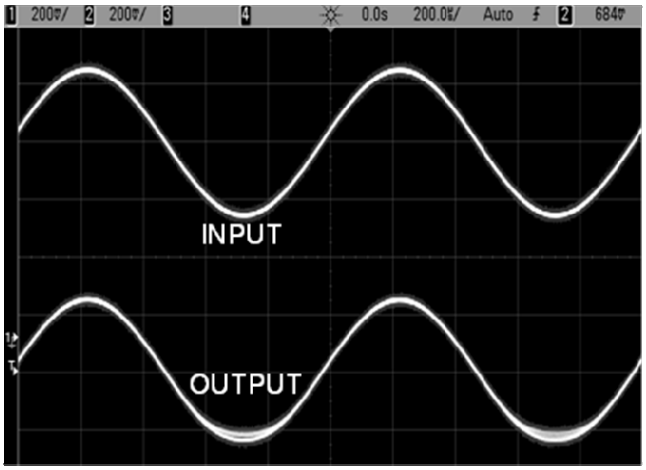
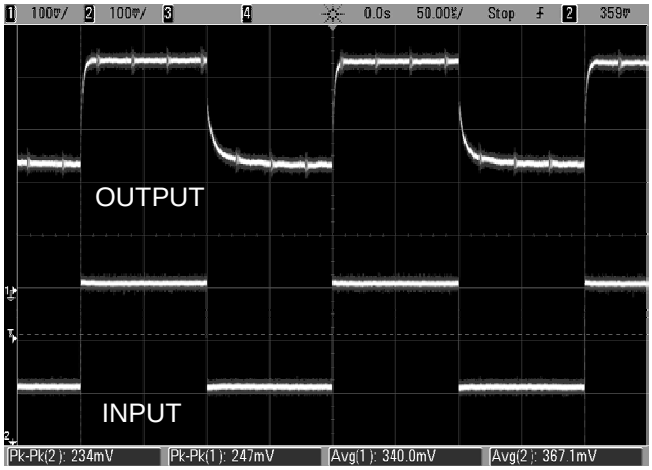


Figure 10. Measurement of transient response for Unity Gain buffer configuration (**a**) PMOS differential pair, VDD = 1.2 V; (**b**) NMOS differential pair, VDD = 0.8 V.



(**a**)



(**b**)

4. Conclusions

A pair of NMOS and PMOS differential input amplifiers were designed and optimized to work from below 0.5 V to 1.5 V in an ultra-low power FDSOI 150 nm process. Both designs have their source body connection tied to minimize any V_T mismatch. Simulation results show that a sub-threshold optimized FDSOI device can provide the capability of low power analog circuit design. Both designs were tested in the lab with mixed results, primarily attributed to the process being not fully mature. Besides the offset errors and noise present, which could be due to the setup, the FDSOI XLP 150 nm process can be a viable process for analog circuitry. As this node matures and yield improves, we expect to implement more designs in the future that will shed more light on the process and its utility for biomedical applications.

Acknowledgments

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