Large-Signal Modeling of GaN HEMT Devices for Power Amplifiers

A thesis

submitted by

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in partial fulfillment of the requirements for the degree of

Master of Science

in

Electrical and Computer Engineering

TUFTS UNIVERSITY

August 2012

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Abstract

The purpose of this thesis is to show that GaN can be used to construct superior radio frequency (RF) transistors for mobile handset power amplifiers (PAs) and similar applications in the 1-2 watt S-band regime. In order to advance research in this operating regime, it is essential to have a quick turnaround (device fabrication, model extraction, circuit design). This thesis will describe a low complexity equivalent circuit large-signal modeling technique to evaluate and design small, medium power GaN high electron mobility transistor (HEMT) based PA circuits; demonstrate both the devices and the described model by the design, fabrication, and testing of both a class AB and class E PA; and identify the properties of GaN that result in portions of the model which increase performance (linearity, efficiency, and spectral masking) compared to other device types.

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Chapter 1. Introduction

1.1. Mobile Communications

Mobile communications is a rapidly growing industry. In the United States alone there are over 300 million mobile phone subscriptions [1], as indicated in Figure 1.1, and upwards of 5 billion worldwide [2]. As of 2007, the mobile communications industry had revenue exceeding $400 billion, an amount that has been increasing by approximately $30 billion per year for over two decades [2].

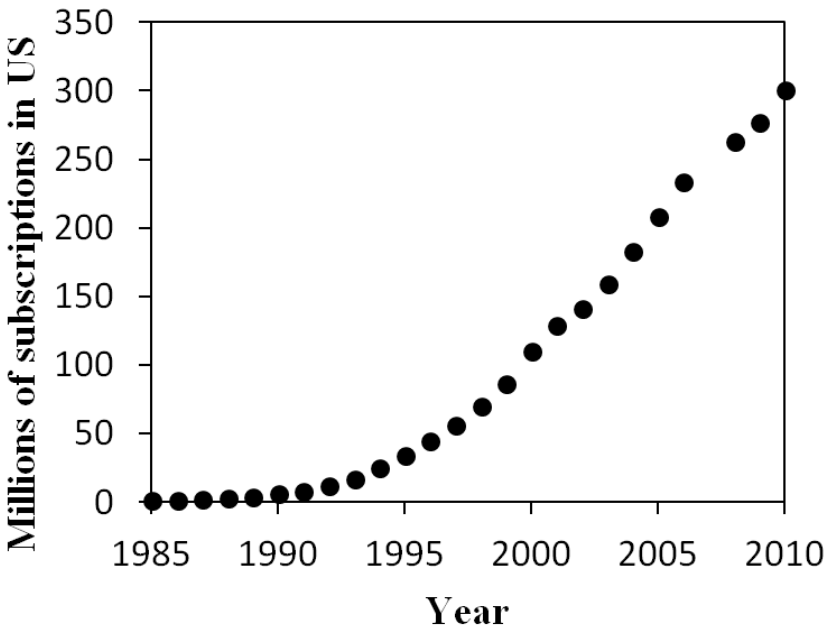


Figure 1.1: Trend in US mobile phone subscriptions [1].

Current and next generation mobile communications standards such as LTE and WiMAX are pushing the boundaries of data capacity, as shown in Figure 1.2, by increasing the complexity of waveforms to increase data throughput within tight bandwidth constraints [2]. To meet these tightening constraints as mobile devices shrink

in size there is increased need for high linearity and high efficiency power amplifiers (PAs) in the 1 W, S-band range.

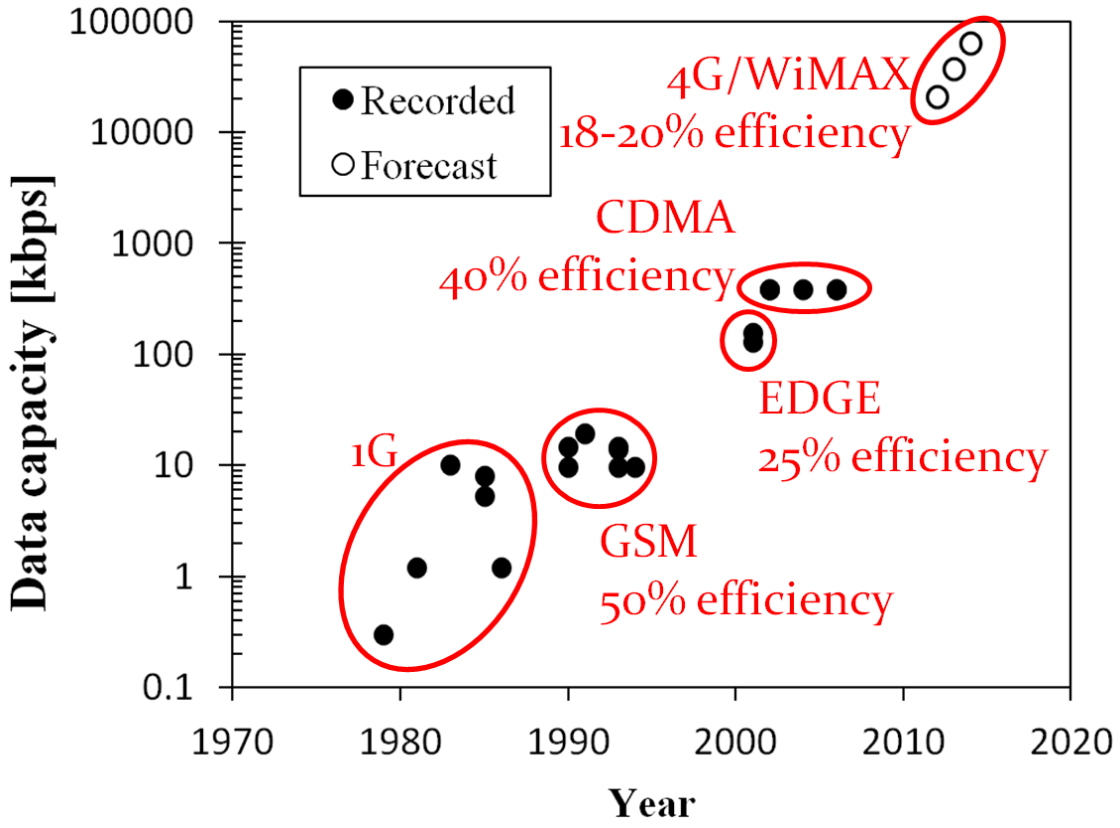


Figure 1.2: Data capacity of mobile communication systems by year [2] [3].

The PA is often the largest consumer of power in a mobile handset system and increasing the efficiency of the PA is the simplest way to increase battery life. The efficiencies of typical handset PAs are indicated in Figure 1.2 and it is clear that PA efficiency should be a growing concern in order to stay competitive in the market. Linearity is important to accurately amplify waveforms containing both phase and amplitude modulation such as orthogonal frequency division multiplexing (OFDM) as used in WiMAX and LTE systems. OFDM may require up to 8 dB power back off,

making PA efficiency important over a range of power levels, not just at peak output power.

As the PA is the largest consumer of power in a mobile handset, PA efficiency has a great impact on the battery life of a mobile device. For example, assume for simplicity that the average output power of a PA is 1 W during transmission and a battery is rated at 4 Wh. For the sake of illustration, the further simplification that all other functions of the mobile device have negligible power draw compared to the PA has been made. Figure 1.3 shows battery lifetime as a function of transmitting PA efficiency. From Figure 1.3, it is observed that increasing efficiency by 25% yields an additional hour of data transmission per battery charge cycle.

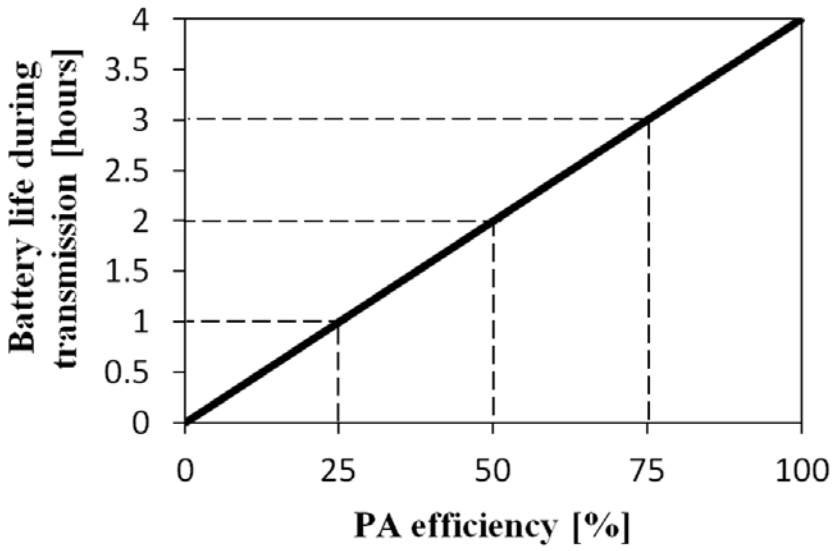


Figure 1.3: Battery lifetime vs. PA efficiency.

1.2. GaN HEMT Technology

GaN as a semiconducting material has seen rapid commercial growth in a range of applications from LEDs and lasers to radio frequency (RF), microwave, and millimeter

wave PAs. Significant focus has been placed on GaN high electron mobility transistor (HEMT) device properties that allow for power amplification at either high power levels (hundreds of watts) or high frequency (tens of GHz) [4]. These same properties should allow for operation at lower frequency and lower power levels (1 to 5 GHz at 1 to 5 watts) with efficiency and linearity in excess of conventional materials operating in this regime, making GaN an appealing contender for mobile handset PA applications.

1.3. Goals and Thesis Outline

The ultimate goal of this work was to demonstrate the benefits of GaN HEMT devices for use in mobile handset PA applications in terms of efficiency, linearity, and meeting spectral masking specifications. In order to make such a demonstration it was first necessary to first show that such PA circuits could be designed and fabricated, as most work with GaN HEMT PA circuits has focused on GaN's ability to achieve high power levels and it's use a lower power levels is a relatively new research topic. Being a relatively new topic meant it was necessary to work with custom GaN HEMT devices in order to achieve appropriate devices dimensions and geometries and to develop a device modeling procedure to rapidly evaluate those devices and use them in circuit designs. The goals of this thesis are summarized in Figure 1.4. A thorough demonstration of GaN HEMT PA circuits in LTE/WiMAX applications remains to be performed using the work presented in this thesis as a foundation.

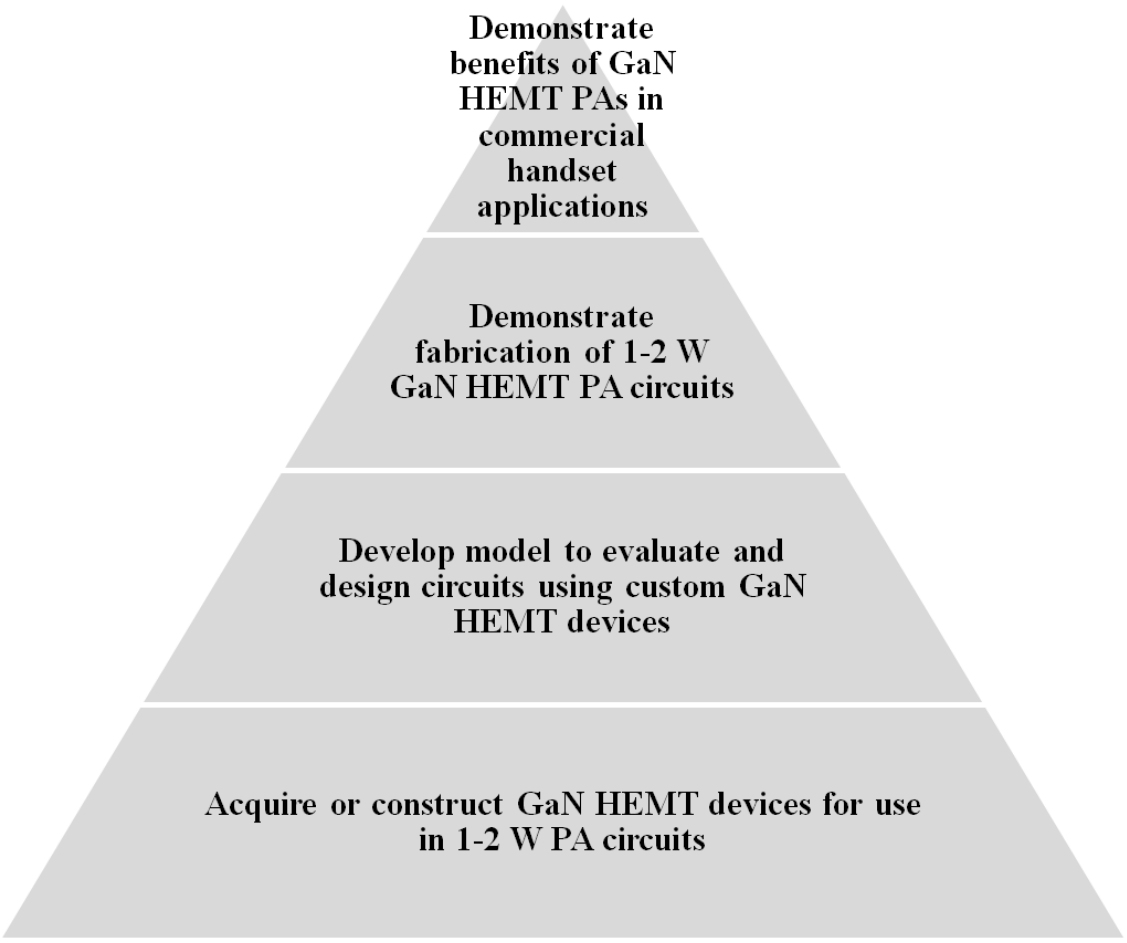


Figure 1.4: Overview of the goals of this thesis.

In order to advance research in this operating regime, it is essential to have quick turnaround (device fabrication, model extraction, circuit design) in order to evaluate and use custom GaN HEMT devices in circuits. This work describes a model that was needed to quickly describe the large-signal behavior of custom GaN HEMT devices to evaluate performance metrics and design PA circuits without need for specialized measurement equipment. With such a rapidly extracted simple model, optimal GaN HEMT designs could be converged upon, at which point a more sophisticated model

could be used requiring longer extraction time and more expensive procedures, such as the Angelov [5] or EEHEMT [6] models or services offered by Modelithics Inc..

Both the devices and their models will be demonstrated by the design, fabrication, and testing of both a class AB and a class E PA, which will be described and shown to possess properties of many standard PA classes used in a variety of PA architectures. The fabricated PAs will allow the identification of properties of GaN HEMTs that result in portions of the model which increase performance (linearity, efficiency, and spectral masking) compared to other device types.

Other GaN HEMT models include EEHEMT [6], Angelov [5], the model described by Negra [7], and the model described by Jarndal [8]. The benefit of the model described in this thesis is the ease and speed of model extraction. The entire model is extracted from standard small-signal S-parameter measurements and DC IV curves using an RF probe station, as opposed to additional temperature measurement equipment and custom test fixtures as described in [5]. This model has the additional benefit of avoiding the need to forward bias the gate junction, as described by [9]. By avoiding such measurements there is no loss of devices in the modeling process and the device for which the model is extracted may be used in circuit fabrication. This is important when dealing with custom research devices as cost per device is high and device yields are low.

The work described in this thesis arose from a collaborative project between the NanoLab at Tufts University, C. S. Draper Lab, and the Advanced Semiconductor Materials and Devices Group at MIT. NanoLab and Draper had the goal of fabricating a 1-2 W PA circuit with highest efficiency and minimum footprint operating around 2.5 GHz and the group at MIT produced GaN HEMT devices for use in the PA circuit.

This thesis begins with background information regarding RF/microwave PAs (chapter 2) and GaN HEMT devices (chapter 3). The motivation for the GaN HEMT modeling work as well as a description of the model development and extraction procedure will be described in chapter 4. Verification of the model through the design and testing of PA circuits will be described in chapter 5 and the results will be discussed and future work will be described in the conclusion in chapter 6.

Chapter 2. Power Amplifiers

2.1. Power Amplifier Fundamentals

An RF/microwave power amplifier (PA) is an active circuit used to convert DC input power into RF/microwave output power. PAs are most commonly used to drive antennas for wireless communications or RADAR but may also be used in applications such as RF/microwave heating or miniature DC/DC converters [10]. There are a wide variety of PA types and transmitter architectures with a vast array of benefits and drawbacks, several of which will be discussed in this chapter.

In order to discuss PA performance and properly make required design trade-offs, it is necessary to examine some figures of merit. These figures to be discussed here include gain, maximum output power, linearity, bandwidth, efficiency, and power added efficiency (PAE).

The primary function of a PA is to provide power gain, so a measurement of gain and maximum output power are the first figures to review. Gain is the ratio of output power to input power. In units of decibels (dB), gain is given by

$$G(\text{dB}) = P_{out}(\text{dBm}) - P_{in}(\text{dBm}) \tag{2.1}$$

where P_{out} and P_{in} are the output and input signal power levels in units of dBm, respectively. The maximum output power is often described in terms of P_{1dB}, the 1 dB saturation power. As the output power level is increased there is a point above which the PA's gain starts to decrease. P_{1dB} is the output power at which the gain is 1 dB below its value at lower power levels. This represents the maximum linear output power of the PA.

By linear output power, what is meant is that the waveform at the output accurately tracks the changes in amplitude and phase of the input waveform and that the only significant difference between the input and output signal waveforms is an increased power level, as determined by the gain. Linearity is often measured in terms of third-order intercept point (IP3) or error vector magnitude (EVM) [11].

Bandwidth is a measure of the frequency range over which a PA can operate. Modern modulation schemes such as orthogonal frequency division multiplexing (OFDM) may require bandwidths of up to 120 MHz, whereas simple amplitude modulation (AM) signals need only operate at a single frequency.

An RF PA is typically the largest consumer of power in a system and for this reason efficiency is an important figure of interest. There are two main methods of measuring the efficiency of a PA, the first is drain efficiency, often referred to simply as efficiency. It is given by

$$\eta = \frac{P_{out}}{P_{in,DC}}, \tag{2.2}$$

the ratio of RF output power to input DC power, both in units of Watts. The other is measure of efficiency is power added efficiency (PAE), which is given by

$$PAE = \frac{P_{out} - P_{in}}{P_{in,DC}}. \tag{2.3}$$

PAE is similar to drain efficiency when the power gain is relatively high but it also accounts for the loss of efficiency when additional input power is needed because the gain is relatively low.

There is typically a trade-off that must be made in terms of the described figures of merit. The trade-offs may be accomplished by proper selection of PA operating class or transmitter architecture, both of which will be discussed below.

2.2. PA Classes

There is a wide variety of operating modes to consider in PA design and each mode of operation is designated by a class. Most standard PA classes can be divided into two groups: linear PAs such as classes A, AB, B, and C; and switching PAs such as classes D, E, and F. A summary of the following discussion on PA classes is found in Table I [12].

In the typical linear PA, the active device is operating as a controlled current source, providing a large output current in proportion to some modulating control signal. Linear PAs are typically used in applications where a large bandwidth or accurate reproduction of the input signal's amplitude variation is required, which comes at the cost of reduced efficiency.

In a switching PA, the active device is operated as a switch controlled by an input signal. The switch is ideally either open, allowing current to flow with no voltage across the device, or closed, with voltage across the device but no current flowing. In the ideal case, this switching allows for 100% efficient operation, which comes at the cost of reduced linearity and bandwidth.

The abovementioned PAs are typically used in the context of a transmitter, of which there is a wide variety of architectures to choose from. Clever transmitter architectures can be used to enhance certain performance characteristics of specific PA

classes as necessary and will be discussed in the following section with a summary found in Table II.

2.2.1. Linear PA

The fist linear PA class to consider is class A, which operates much like a small-signal amplifier. The bias point of the transistor is chosen such that current is flowing throughout the entire cycle of the input waveform. Figure 2.1 shows an input voltage driving an output current, as in a typical FET [11]. In the class A case the instantaneous input voltage is never below the FET's threshold voltage level. The class A bias point is set to half of the maximum current and allowed to swing from zero to I_{max}. The drain voltage is biased at some value, V_{dd}, and allowed to swing from near-zero to twice the value of the DC bias. The instantaneous drain voltage cannot reach down to zero volts due to the knee voltage of the transistor.

The maximum output power of a class A PA is given by

$$P_{max} = \frac{1}{2}(V_{dd})\left(\frac{1}{2}I_{max}\right) = \frac{1}{4}V_{dd}I_{max}\,, \tag{2.4}$$

where R is the PA's load [11]. The maximum drain efficiency, η, using equation (2.2) is

$$\eta_{max,A} = \frac{\frac{1}{4}V_{dd}I_{max}}{(V_{dd})\left(\frac{1}{2}I_{max}\right)} = \frac{1}{2}\,. \tag{2.5}$$

In a class B PA the bias point is shifted from the class A point so the gate bias is at the threshold voltage. This results in a FET conducting current for half of the input waveform cycle. As depicted by Figure 2.1, the instantaneous drive voltage is below the FET's threshold voltage for half of the waveform's cycle and the current swings from zero to I_{max}. The voltage swings from near-zero to $2V_{dd}$. This is similar to class A and, in

fact, the maximum power of a class B PA is also given by equation (2.4). The efficiency, however, increases from the class A case because the DC current is reduced from ½ I_{max} to 1/π I_{max}. Thus the efficiency of an ideal class B PA is

$$\eta_{max,B} = \frac{\frac{1}{4}V_{dd}I_{max}}{(V_{dd})\left(\frac{\pi}{2}I_{max}\right)} = \frac{\pi}{4} \approx 0.785 \, . \tag{2.6}$$

The class B PA can be either single ended or push-pull. In a single ended class B there is only one transistor with half of the input waveform (below the FET's threshold) is not reproduced at the output. Push-pull refers to a PA having two transistors of opposing polarities, allowing the PA to reproduce the entire input waveform. The two configurations have identical efficiency in the ideal case, while the push-pull configuration has higher linearity and gain. In reality, however the single ended configuration will be more efficient because the losses suffered due to transistor and circuit non-idealities will be smaller.

Class AB is used as a compromise between classes A and B. The bias point is somewhere between that of class A and class B, thus producing the same maximum output power with efficiency somewhere between 0.5 and 0.785 depending on the exact bias point.

The bias point can be set below the conduction threshold of the FET as well. This is considered class C operation. This bias point results in output current for less than half of the input cycle, resulting in increased efficiency at the expense of reduced linearity and gain. As the bias point is arbitrarily reduced current is produced for smaller portions of the input cycle the efficiency approaches 100% as the conduction angle approaches zero, thus the class C PA has efficiency between 0.785 and 1.0.

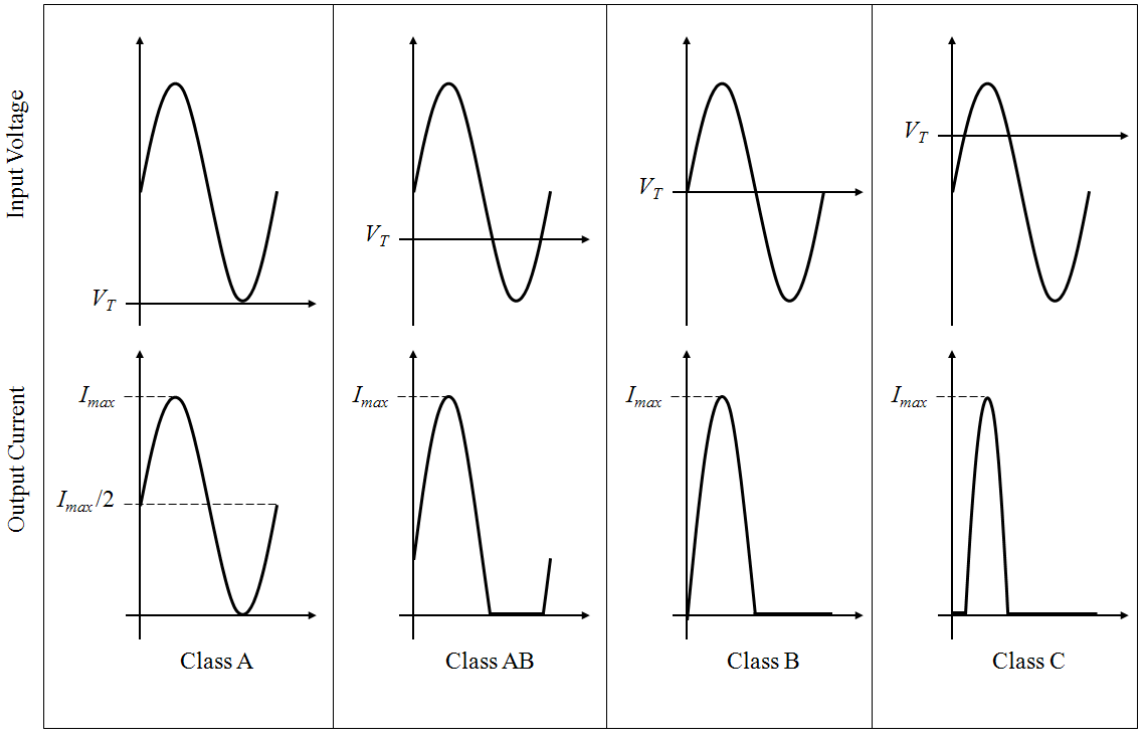


Figure 2.1: Input voltage and output current waveforms for FET based linear PA classes.

2.2.2. Switching PA

The standard use for a switching PA is in an application where efficiency is a high priority and linearity and bandwidth are much lower priorities. In the ideal switching PA the active device performs a switching operation: it is either open, allowing current to flow with no voltage drop across the active device, or closed, with a voltage drop across the device but no current flow. Since at no point is there both current through and voltage across the device, the ideal DC input power is zero and efficiency is 100%. In reality, however, a number of factors prevent the PA from reaching 100% efficiency as will be discussed below.

A significant result of operating the active device as a switch is the loss of the input signal's amplitude information, only phase information can be conveyed. Small

variations in the amplitude of the input waveform will result in no change to the output waveform while reducing the input signal amplitude to a large degree may have an impact on the device's ability to operate as a switch, causing the efficiency to decrease rapidly.

Class D operation utilizes two FET as switches to produce a drain voltage waveform resembling a square wave, which is then passed through a filter tuned to the fundamental frequency to output a sinusoidal waveform. A simplified schematic is shown in Figure 2.2. Non-ideal class D PAs suffer from non-instantaneous switching speeds and from the need to charge and discharge the drain capacitance of the FET each cycle of the RF signal. For these reasons, class D is restricted to relatively low operating frequencies (e.g. less than 500 MHz).

While the drain capacitance is an issue for class D operation, it is taken advantage of by the class E PA. As shown in Figure 2.3, a class E consists of a single FET operated as a switch with additional shut capacitance placed at the drain. The waveform, as shown in Figure 2.5, is the result of charging and discharging that capacitance. As in the class D case, the periodic charging and discharging of the capacitance limits high frequency operation of class E PAs.

Class F (shown in Figure 2.4) operation utilizes harmonic tuning to achieve high efficiency. The output voltage is tuned to promote odd harmonics which result in a square waveform and the output current is tuned to promote even harmonics in such a way as to produce a half sinusoid function as shown in Figure 2.5.

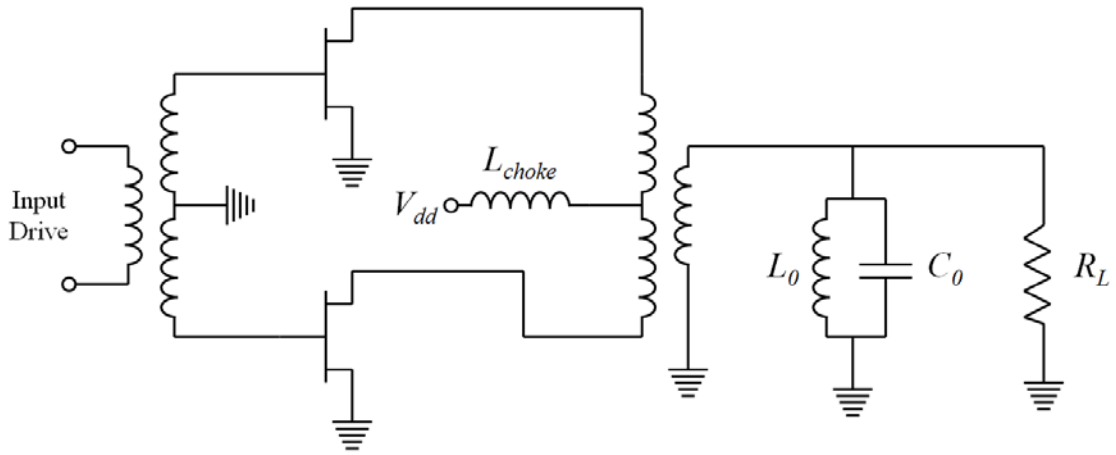


Figure 2.2: Simplified class D PA schematic [12].

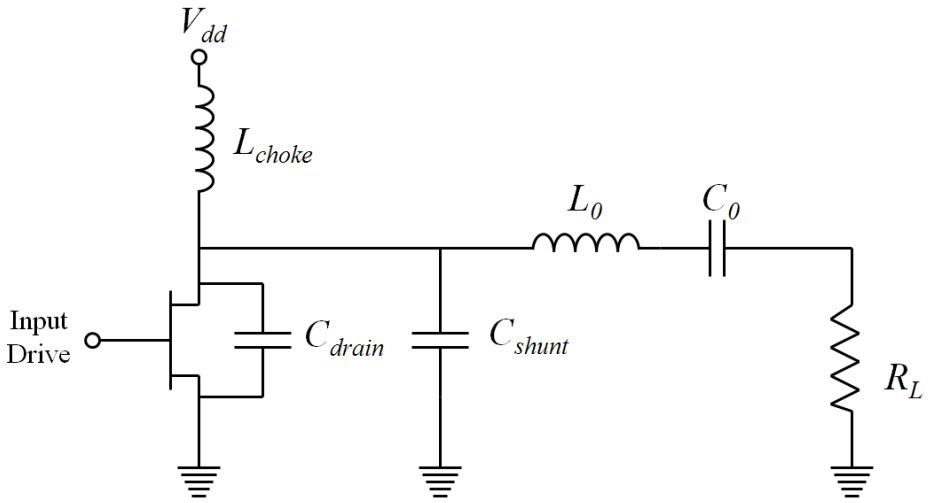


Figure 2.3: Simplified class E PA schematic [12].

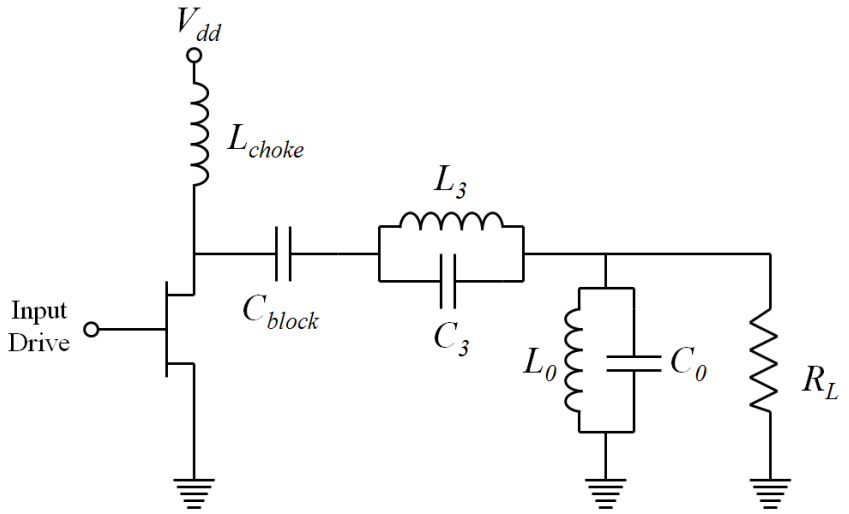


Figure 2.4: Simplified class F PA schematic [12].

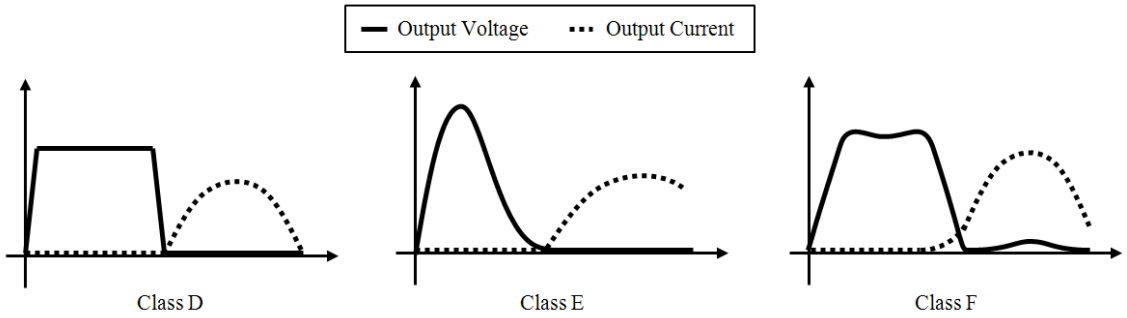


Figure 2.5: Voltage and current waveforms in ideal switching PA classes [12].

Table I: Comparison of described PA classes [12].

Class	Maximum Drain Efficiency	Linearity	Normalized Maximum Output Power
A	50	Very high	0.39
AB	50 – 78.5	Very High	0.39
B	78.5	High	0.39
C	78.5 – 100	High – Low	< 0.39
D	100	Very Low	1
E	100	Very Low	0.31
F	100	Very Low	0.5

2.3. Transmitter Architectures

The simplest PA architecture is the class A linear amplifier. It is both very simple to design and highly linear. Its simplicity and linearity, however, come at the expense of low efficiency. Switching amplifiers such as classes D, E, and F require more careful design and produce nonlinear outputs, but can achieve very high efficiency. This is the general trade off in PA design: linearity versus efficiency. The balance of these two metrics is increasingly important as portable devices become more feature rich and wireless data speeds increase. Modern modulation schemes used for robust high speed data transmission make use of very complex waveforms. High PA linearity is essential at preserving both amplitude and phase information of these waveforms and reducing the adjacent-channel power ratio (ACPR) to make efficient use of the wireless spectrum. The main drives to achieve high efficiency PAs are to extend battery life in mobile devices and to reduce thermal energy in the PA circuit. There are several techniques and transmitter architectures available to either increase the efficiency of highly linear PAs or to increase linearity of highly efficient PAs. This section includes descriptions of the more promising techniques. Following the individual descriptions is Table I a summary and comparison of the architectures described.

2.3.1. Doherty

A Doherty amplifier makes use of two separate PAs: a carrier PA and a peaking PA, whose outputs are then combined to form a single linear output. The benefit of the Doherty architecture is that it allows high efficiency operation at significantly backed-off input power (up to 10 dB power back-off) [11]. A schematic of a Doherty PA is shown in Figure 2.6.

The main PA is typically class B or AB followed by a quarter-wavelength transmission line or equivalent network. The peaking PA is typically class C and, conversely, is preceded by a quarter-wavelength line. The two PAs are biased such that up to a certain input amplitude the main PA is the sole producer of output and the peaking PA is biased off. Above that point the main PA begins to saturate and the peaking PA produces output. The output of the peaking PA is combined with the saturated main PA's output to produce a single output, which remains linear up to the saturation point of the peaking PA.

High efficiency is achieved by forcing the main PA to saturate at a power level significantly backed-off from the overall peak output power. The technique employs active load-modulation as described in [11].

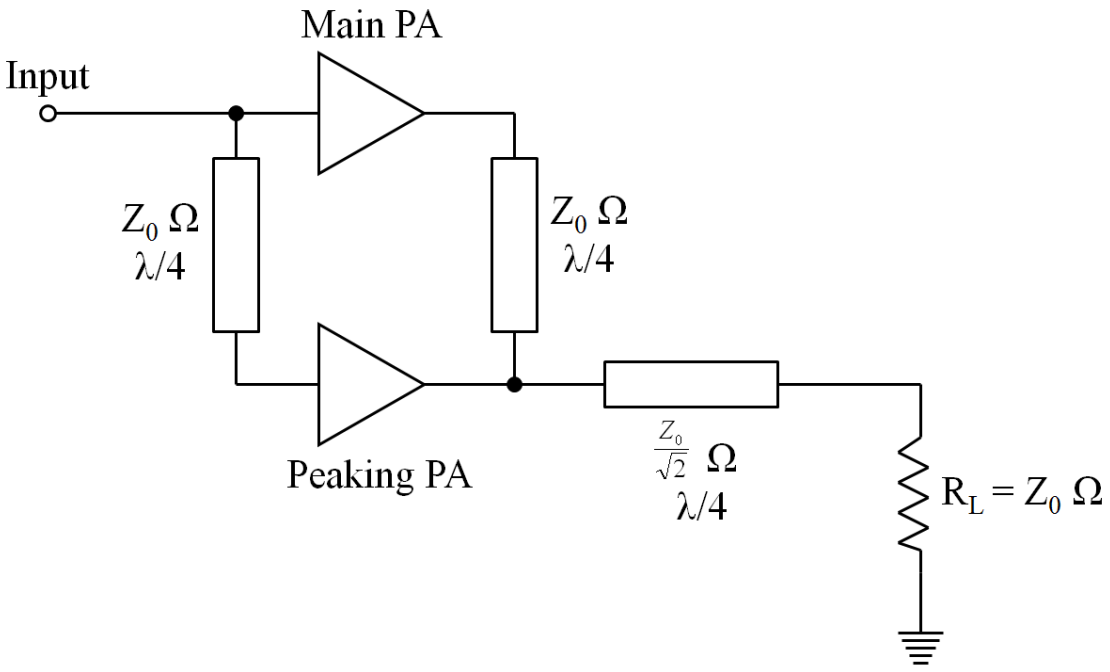


Figure 2.6: Schematic of Doherty PA architecture [11].

2.3.2. Polar Modulation, EER, and ET

Polar modulation, envelope elimination and restoration (EER), and envelope tracking (ET) are all variations on one central idea: using the envelope of the modulated signal to control the DC supply voltage of a PA. By controlling the DC supply voltage a PA can be kept at or near saturation, achieving its highest efficiency [10]. Each of these three techniques will be described separately.

In a polar modulation scheme, as shown in Figure 2.7, a system DSP is assumed to separately provide phase and amplitude signals to ultimately modulate a single carrier [10]. The phase information with constant amplitude is applied to a carrier and amplified in a PA. The amplitude information is conditioned and used to accurately control the DC supply voltage of the PA. By controlling the PA's supply voltage with high accuracy and amplifying a constant amplitude signal the PA can be kept close to saturation, achieving peak efficiency.

EER works on the same principal but instead of being supplied separate phase and amplitude signals, its input is a modulated RF carrier, as shown in Figure 2.8 [10]. A coupled envelope detector provides the envelope for conditioning and DC supply control and a limiter at the PA input ensures constant amplitude and undistorted phase information will be amplified.

ET is similar to EER with two significant exceptions. The ET architecture is shown in Figure 2.9. The first difference is the absence of the limiter. The input to the PA is an unmodified carrier with amplitude and phase modulation. The second difference is that the conditioning of the envelope for control of the DC supply voltage has much lower resolution in polar modulation or EER [10]. For example if the DC supply

controller has two voltage levels: when the signal is significantly backed off from its peak value the DC voltage may be at the lower level to keep the PA near saturation. As the input signal increases the DC supply voltage will change to the higher level to raise the level at which the PA saturates.

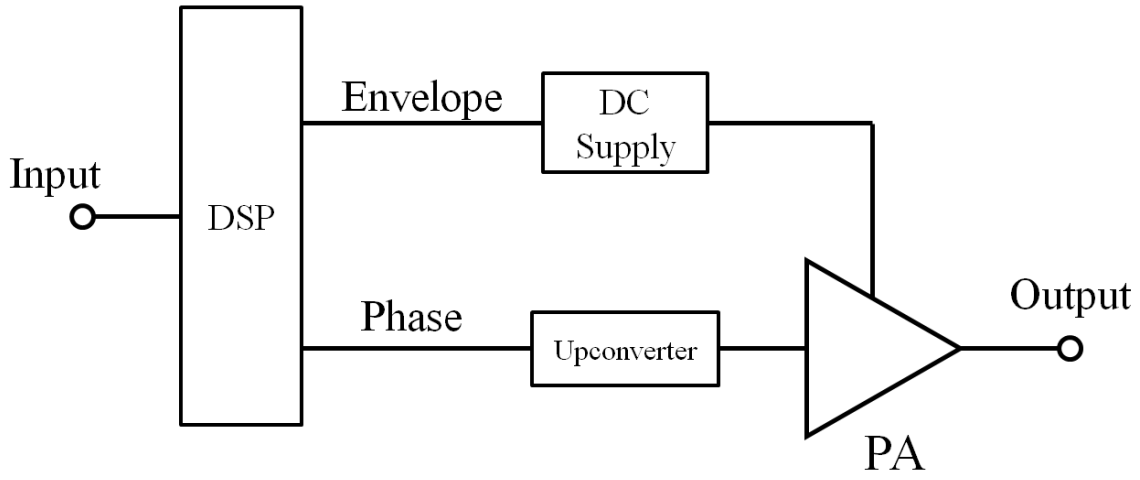


Figure 2.7: Schematic of polar PA architecture [10].

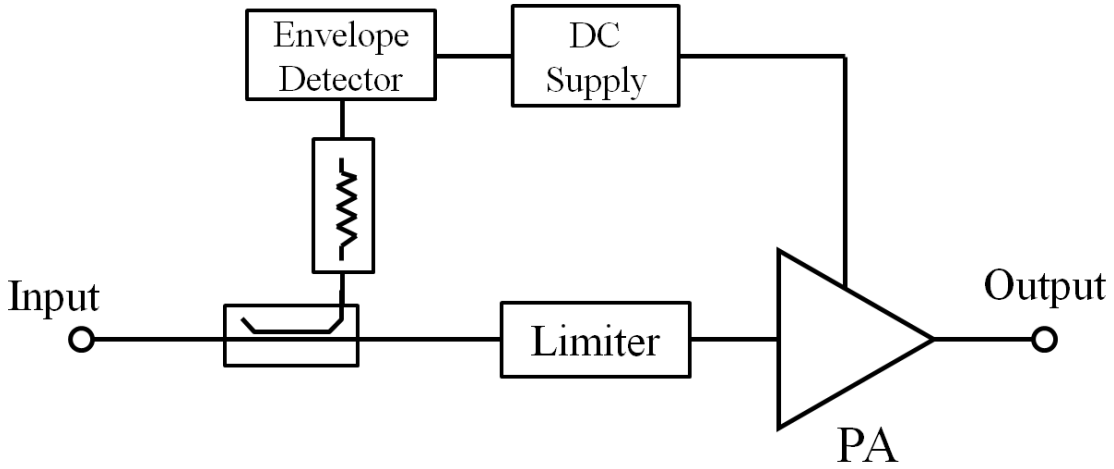


Figure 2.8: Schematic of EER PA architecture [10].

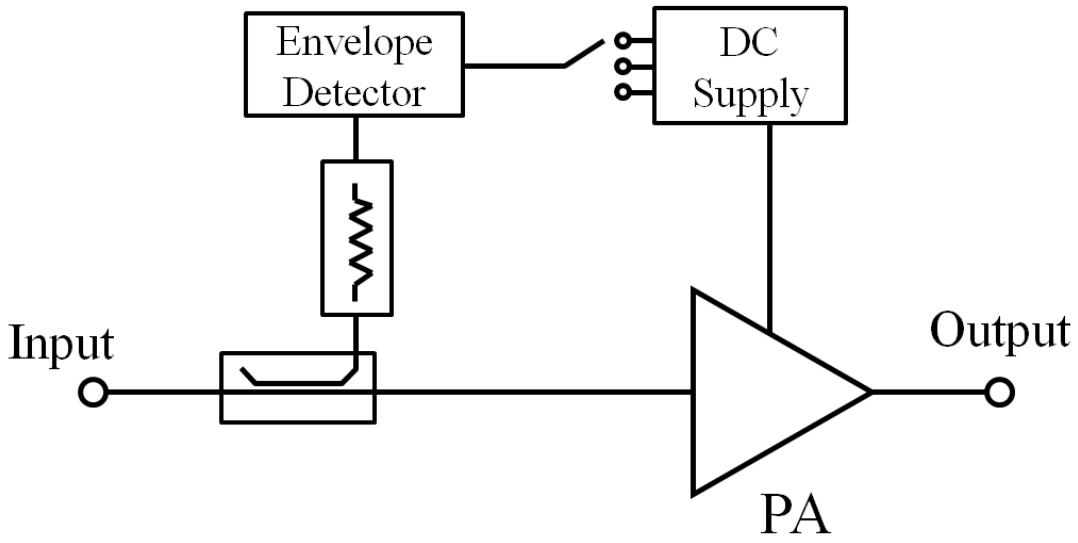


Figure 2.9: Schematic of ET PA architecture [10].

2.3.3. Predistortion

Predistortion is a linearization technique that applies nonlinear distortion to an input signal before amplification in a manner that is complimentary to the nonlinear distortion of the amplifier itself such that the product is a linearly amplified version of the original input waveform at the output of the PA [10]. The predistortion architecture is shown in Figure 2.10, along with a plot of the PA and predistorter output relationship. This technique can be applied in various ways, namely analog or digital baseband, analog or digital IF, and analog RF. The predistorting circuit itself has a large impact on the performance of the amplifier, typically by reducing the bandwidth of a PA.

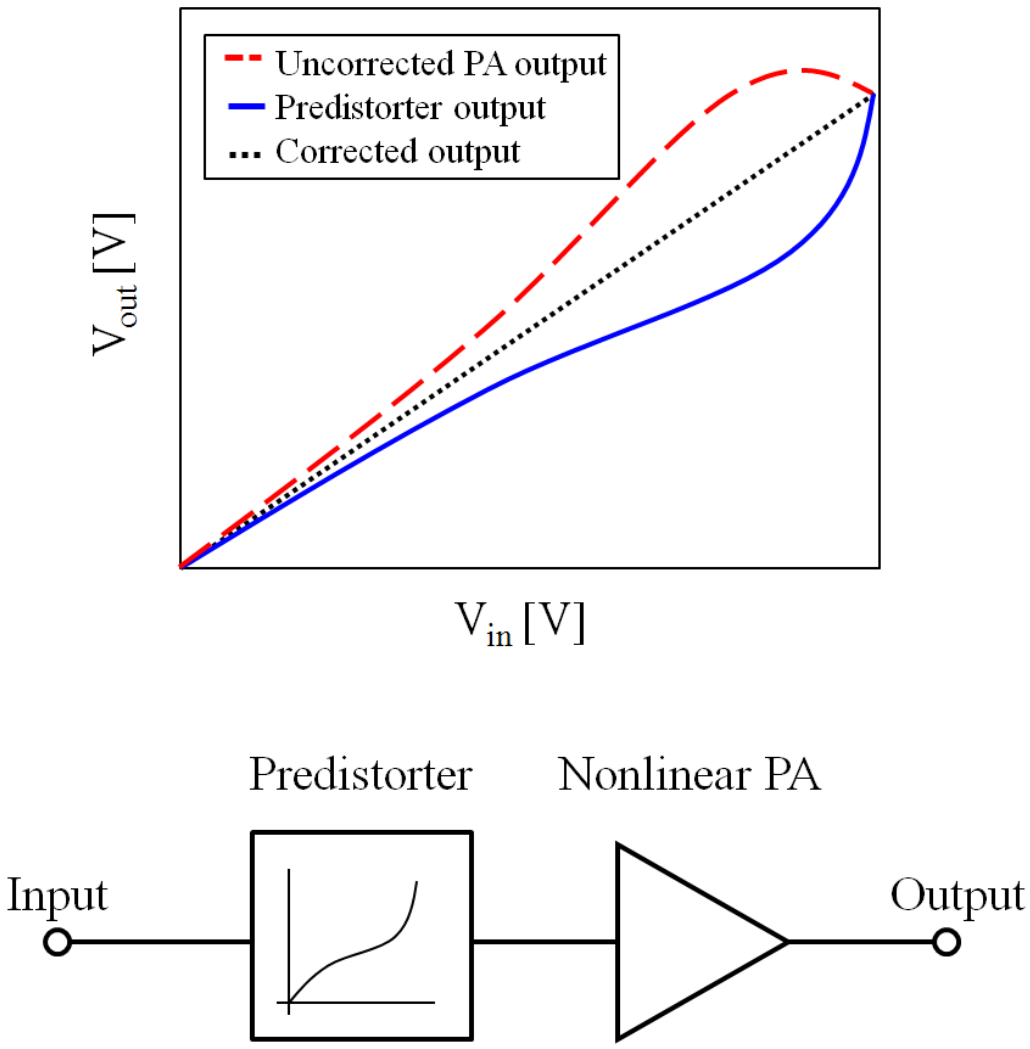


Figure 2.10: Schematic of predistortion PA architecture and plot of concept [10].

2.3.4. Class S with Bandpass Delta-Sigma Modulation

The class S architecture works with switching amplifiers to improve linearity in what would typically be a PA incapable of containing any envelope information [10]. It works by passing the input RF signal through a bandpass ΔΣ-modulator to produce a pulse-density-modulated (PDM) signal. An ideal PDM signal is a square waveform, which is also the ideal input for switched mode PAs to achieve maximum efficiency. The amplified PDM signal is then passed through a bandpass filter centered on the

fundamental frequency, leaving intact the phase and envelope information present in the input signal. This is shown in Figure 2.11. A significant limitation of class S is seen in its frequency response due to the necessarily narrow band pass filter at its output. Another constraint is that the ΔΣ-modulator must be capable of achieving switching speeds of approximately seven times the RF frequency [10].

An additional benefit of class S is the potential for integration into future systems. As DSPs get increasingly fast it may become possible to eliminate the ΔΣ-modulator portion of the amplifier and drive the switching PA directly from the final DSP stage [10].

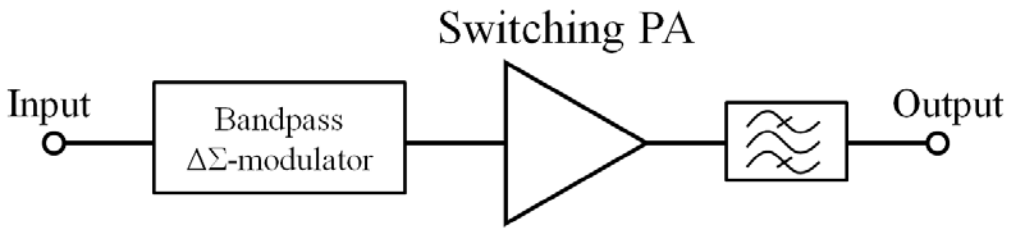


Figure 2.11: Schematic of class S PA architecture [10].

2.3.4. Feedback

Feedback can be used to increase linearity in an amplifier. The feedback can be either RF (applied directly around the RF amplifier) or envelope (applied around the modulation circuitry) [11]. In the case of RF feedback, linearity can be greatly increased but typically at the expense of a loss in gain and bandwidth. Close attention must be paid to the delay in an RF feedback configuration as significant delays could pose a serious threat to a PA's stability. The issue of delay is largely negated in the case of envelope feedback, as shown in Figure 2.12. Envelope feedback is typically much simpler to

implement and is therefore a more popular solution. A coupler at the output of the PA is fed into an envelope detector and that envelope can be compared to the envelope of the PA's input signal to determine the error and make any corrections.

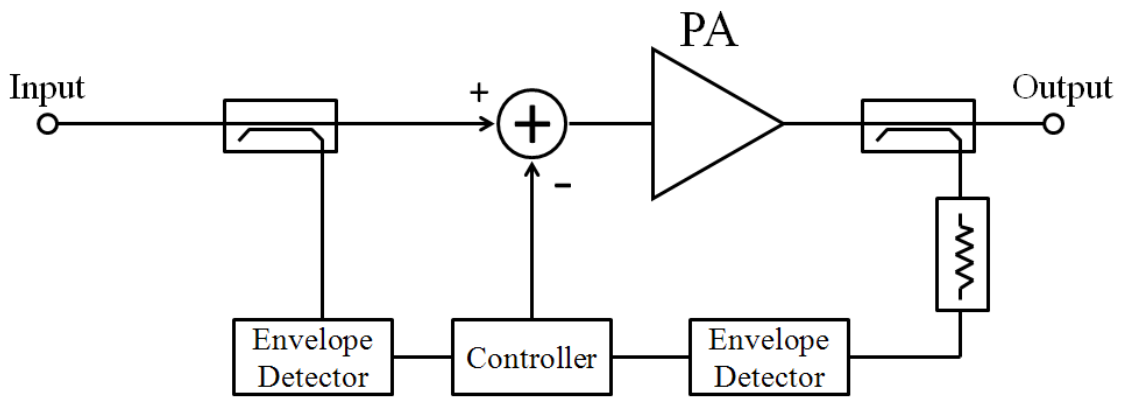


Figure 2.12: Schematic of feedback PA architecture [10].

Table II: Comparison of described PA architectures.

Architecture	Benefit	Drawback
Doherty	Efficiency & linearity	Needs two PAs, reduced bandwidth
Predistortion	Linearity	Lowers gain, requires additional DSP
Class S	Efficiency & linearity	Needs high frequency switching PA and DSP, reduced bandwidth
Polar	Efficiency & linearity	Requires DC power conditioning
Envelope Tracking	Efficiency & linearity	Requires DC power conditioning
EER	Efficiency & linearity	Requires DC power conditioning
Feedback	Linearity	Lower gain, reduced bandwidth

2.4. Recent PA Work

A summary of recent PA work reported in the literature is shown in Table III and shown graphically in Figure 2.13 in terms of PAE and output power. Several PA classes are shown using GaAs and GaN HEMT technology. It is observed that GaN is dominant

at higher supply voltages and output power levels and generally used in higher efficiency PAs. This information will be revisited in the conclusions in chapter 6 to compare the PAs that will be described in chapter 5.

Table III: Summary of recent GaAs and GaN HEMT PA work.

Reference	Technology	Class	Drain Supply [V]	Pout [dBm]	PAE [%]	f [GHz]	Gain [dB]	Year
[13]	GaAs	A	4	23.5	40	25	11	2012
[14]	GaAs	A	8	34	37.1	3.5	28	2008
[15]	GaAs	A	9	24	29	2.4	40	2007
[16]	GaAs	A	8	38.1	24	14	10.5	2007
[17]	GaAs	AB	5	33	35	5.8	14	2006
[18]	GaN	B	20	36	34	8	9	2003
[19]	GaN	D	10	39	65	2.35	10	2009
[20]	GaN	E/F	30	40	73.1	2.14	14.3	2011
[21]	GaN	F	28	36	66	2.7	13.8	2011
[22]	GaN	F	25	33.4	71.4	5.8	10	2010
[23]	GaN	F	42.5	42.3	85	2	13	2007
[24]	GaAs	F	5	19	68	2	14	2005
This work (measured)	GaN	AB	15	30.5	65.7	2.5	9.3	2012
This work (simulated)	GaN	E	20	31	70	2.5	10	2012
This work (measured)	GaN	E	12	30.1	64.4	2.6	10.6	2012

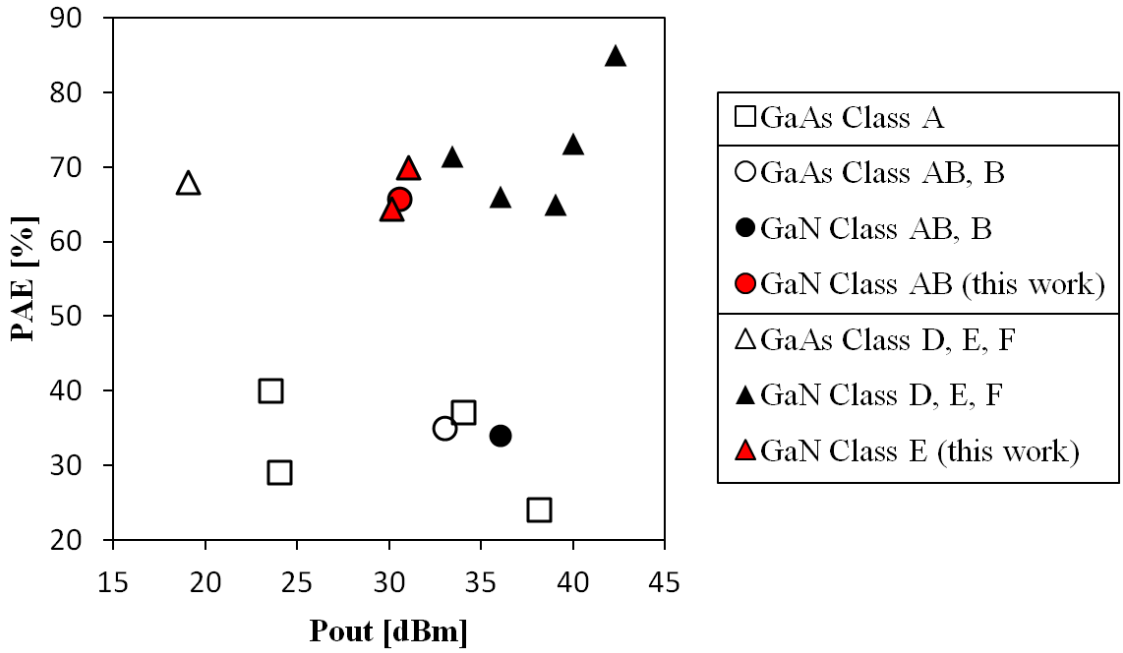


Figure 2.13: Summary of recent GaAs and GaN HEMT PA PAE vs. output power.

Chapter 3. GaN HEMT

3.1. GaN Background

The GaN HEMT is a semiconductor device used primarily in RF/microwave PA applications such as cellular phone and WiMAX base stations [25]. It is known chiefly for its high power and high frequency operation. This is enabled by high breakdown voltage due to its wide bandgap, high saturation velocity, and high electron mobility.

The high electron mobility of GaN HEMT devices is achieved by a two-dimensional electron gas (2DEG). A 2DEG exists at the interface of two semiconductor layers of differing band gaps (known as a heterojunction). Typically in a GaN HEMT these layers are AlGaN and GaN. The first observation of a 2DEG in an AlGaN/GaN heterojunction was reported in 1992 [4]. A carrier concentration was observed on the order of 10^{11} cm^{-2} with an electron mobility of 400-800 cm^2/V-s at room temperature. By 2000, devices achieving power densities of 11 W/mm were reported, and as of 2006 a record power density of over 40 W/mm was reported at 4 GHz. As of this writing, electron motilities as high as 2000 cm^2/V-s have been observed and operating frequencies as high as f_t = 225 GHz have been reported [26].

Although the first GaN HEMT was demonstrated in 1992, the HEMT device structure had first been demonstrated in 1980 using AlGaAs/GaAs [25]. Other materials have been used to construct HEMTs as well, including InAlAs/InGaAs, AlSb/InAs, and SiGe/Si. The HEMT is also known by several other names including heterojunction field effect transistor (HFET or HJFET), modulation doped field effect transistor (MODFET), two-dimensional electron gas field effect transistor (TEGFET), and selectively doped field effect transistor (SDFET) [27].

This chapter contains a discussion of the operation and underlying physics of the GaN HEMT device and will proceed to compare this device to other device structures and materials commonly used in similar high power and high frequency PA applications.

3.2. Device Physics

GaN is a type of III-V compound semiconductor, meaning it is a combination of two elements: one from group III (gallium) and one from group V (nitrogen). Some other common examples of III-V semiconductors are GaAs and InP. GaAs is a major point of comparison to GaN due to the prevalence of GaAs HEMTs. Operation of a GaN HEMT relies on the heterojunction which has several varieties, most commonly AlGaN/GaN, which will be discussed here.

The GaN HEMT is a type of field-effect transistor (FET). In the operation of a FET, an electric field resulting from a voltage applied to the gate electrode modulates the conductivity of a channel between the drain and the source electrodes. The profile of a simplified GaN HEMT is shown in Figure 3.1. In general, a HEMT is composed of two materials of different band-gaps forming a heterojunction, a gate electrode forming a Schottky barrier with the topmost semiconductor layer, and drain and source electrodes forming ohmic contacts with the semiconductor layers.

A Schottky barrier diode is formed at the interface of a metal and a semiconductor material, such as the gate electrode and AlGaN layer in a typical GaN HEMT. Since HEMTs are generally depletion mode devices, (e.g. a large negative control voltage applied to the gate will turn the device off and at zero volts the device will be on), the Schottky diode will be reverse biased and little-to-no current will flow in to the gate [27].

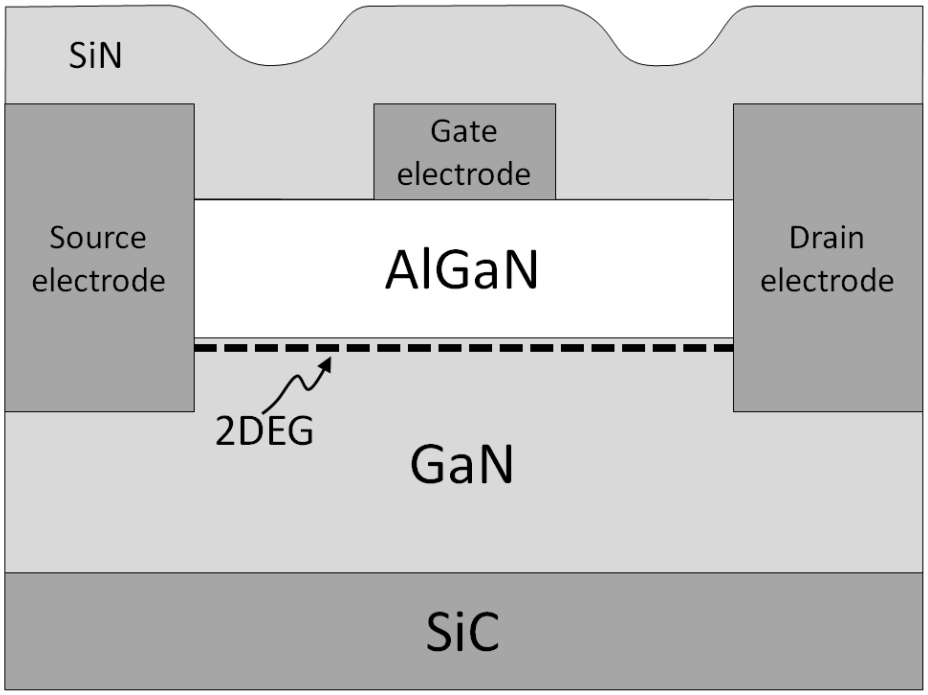


Figure 3.1: GaN HEMT device structure.

An ohmic contact is a metal semiconductor contact that does not operate as a Schottky barrier diode. This is achieved either by doping the semiconductor or selecting alloys for the electrode material to ensure sufficiently low Schottky barrier height or barrier depletion width. In order to achieve sufficiently low barrier height between an electrode and AlGaN, the electrode can be made of an Al-In alloy [28] or for sufficiently narrow depletion widths, the electrodes can be made of a Ti-Al alloy [26].

At the heterojunction is a two-dimensional electron gas (2DEG), which consists of electrons confined in a potential well that are free to move within the plane of the interface. An electron contained in a potential well has quantized energy. The term two-dimensional electron gas refers to this quantization of electrons' energy levels in the spatial direction perpendicular to the heterojunction while the electrons are free to move in directions parallel to the heterojunction. The energy-band diagram is shown in Figure 3.2 and the quantum well containing the 2DEG is indicated.

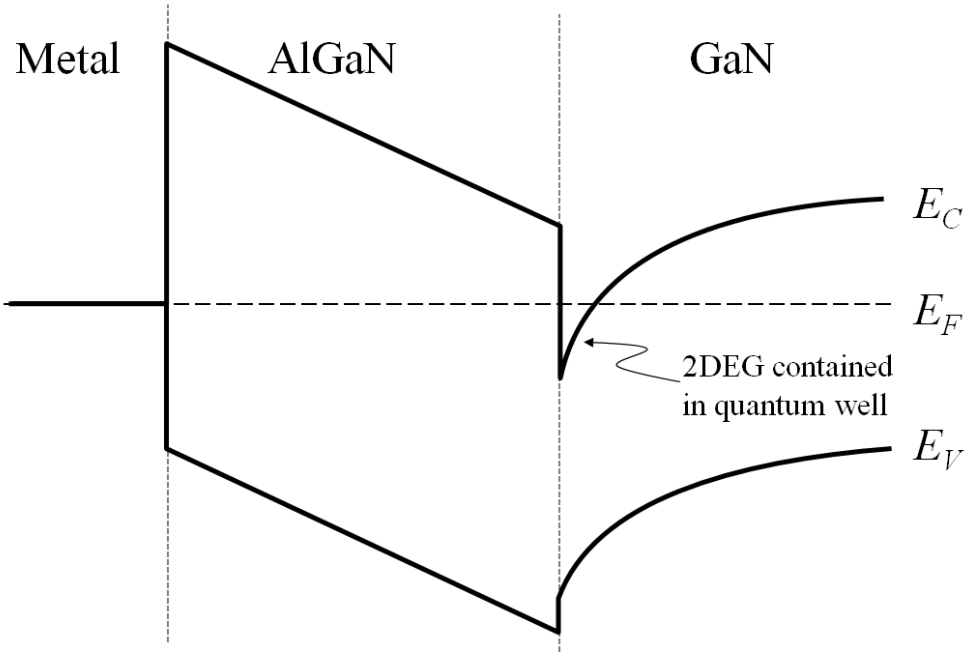


Figure 3.2: AlGaN/GaN HEMT band diagram.

Another property of the HEMT that allows for high mobility is the lack of doping at the channel. This reduces the degradation of ionized impurity scattering, thus increasing mobility and saturation velocity [27].

When a small positive voltage is applied to the Schottky gate, the edge of the conduction band of the GaN layer will lie below the Fermi level, giving rise to a large electron density in the 2DEG. This is shown in Figure 3.3 (a). However, when a large negative voltage is applied to the gate and $V_{gs} < V_T$, where V_T is the threshold voltage of the HEMT and V_{gs} is the gate-to-source voltage, the conduction band edge moves above the Fermi level, limiting current flow due to the small electron density in the 2DEG. This state is illustrated in Figure 3.3 (b) [27].

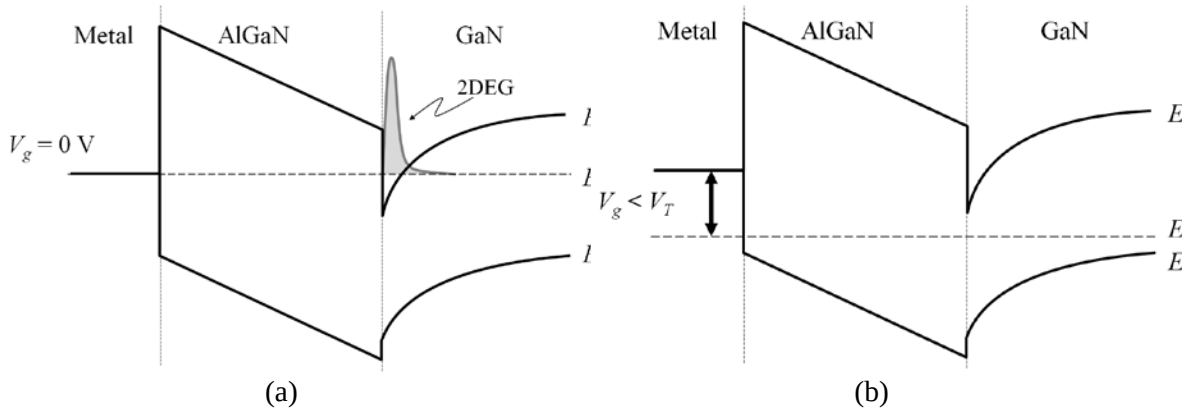


Figure 3.3: Energy band diagrams with HEMT biased (a) above and (b) below the threshold voltage.

Typical current voltage characteristics (IV curves) of a GaN HEMT are shown in Figure 3.4. The qualitative behavior of the IV curves is similar to that of most FET structures. There is a linear region for small values of V_{ds} and a saturation region for large values of V_{ds}. HEMT devices operate in depletion mode, meaning large negative voltages applied to the gate will reduce the 2DEG and prevent current flow between the drain and source. If the gate voltage rises above the build-in voltage of the Schottky barrier diode then the gate will be forward biased, potentially damaging the device and causing current to flow from the gate to source electrodes.

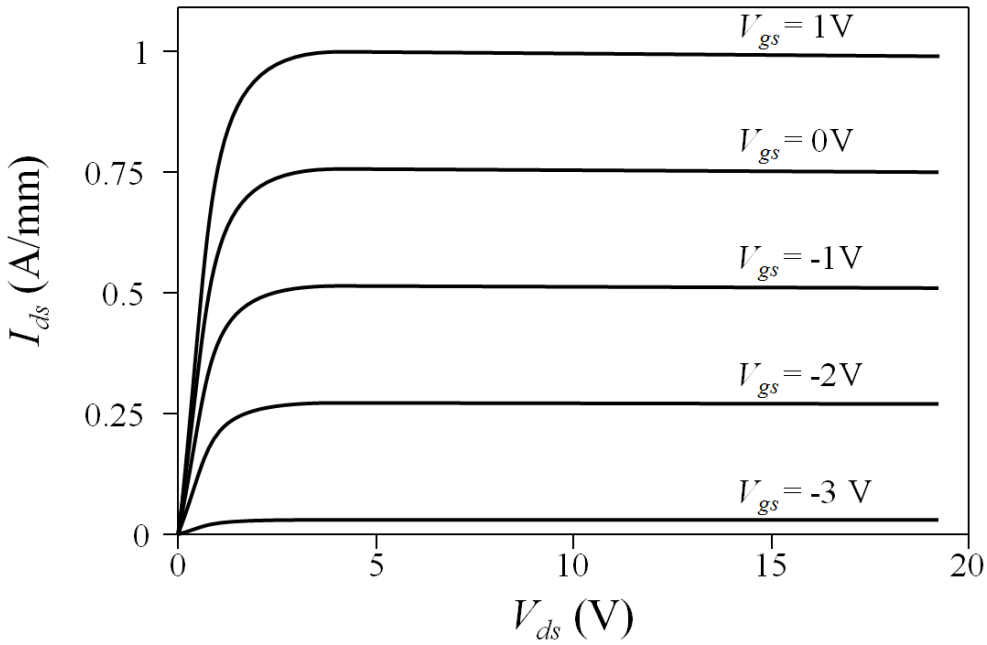


Figure 3.4: Typical current voltage characteristics of a GaN HEMT.

The current-voltage characteristics shown in Figure 3.4 are described in detail in [26] and are summarized as follows. For simplification of the analysis, the 2DEG is assumed to be perfectly two-dimensional. Under this assumption the charge density of the 2DEG under a linear charge control approximation is given by

$$qn_s = C_g(V_{gs} - V_T) = \frac{\epsilon}{d_{AlGaN}+\Delta d}\left(V_{gs} - \phi_B + \frac{\sigma_p\, d_{AlGaN}}{\epsilon} + \frac{\Delta E_c}{q}\right). \tag{3.1}$$

All variables are described below in Table IV. The drain-to-source current, normalized to the width of the gate, is given by

$$I_{ds} = qn_s(x)v(x) \tag{3.2}$$

where $v(x)$ is described by a two piece linear approximation as

$$v(x) = \begin{cases} \mu E(x), & E(x) < E_{crit} \\ v_{sat}, & E(x) \geq E_{crit} \end{cases} \tag{3.3}$$

The drain-to-source current and transconductance can be described in two regions: linear and saturation. In the linear region the current and transconductance are given by

$$I_{ds,lin} = \frac{\mu C_g}{L_g}\left[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}\right] \tag{3.4}$$

$$g_{m,lin} = \frac{\mu C_g}{L_g}V_{ds} \tag{3.5}$$

and in the saturation region

$$\begin{aligned} I_{ds,sat} &= v_{sat}C_g\left[\sqrt{(V_{gs} - V_T)^2 + (l_{crit}E_{crit})^2} - l_{crit}E_{crit}\right] \\ &\approx v_{sat}C_g(V_{gs} - V_T - l_{crit}E_{crit}) \end{aligned} \tag{3.6}$$

$$g_{m,sat} = v_{sat}C_g\frac{V_{gs}-V_T}{\sqrt{(V_{gs}-V_T)^2+(l_{crit}E_{crit})^2}} \approx v_{sat}C_g\ . \tag{3.7}$$

Table IV: Description of variables used in equations (3.1) – (3.7).

Variable	Description	Variable	Description
C_g	Gate capacitance per unit area	$v(x)$	Electron velocity as a function of distance from source electrode
d_{AlGaN}	Thickness of AlGaN layer	V_{ds}	Drain-to-source voltage
$E(x)$	Electric field as a function of distance from source electrode	V_{gs}	Gate-to-source voltage
E_{crit}	Critical electric field for velocity saturation	v_{sat}	Electron saturation velocity
$g_{m,lin}$	Transconductance in linear region	V_T	HEMT threshold voltage
$g_{m,sat}$	Transconductance in saturation region	x	Position between source and drain
I_{ds}	Drain-to-source current normalized to gate width	Δd	Distance of 2DEG from heterointerface
$I_{ds,lin}$	Drain-to-source current in linear region	ΔE_c	Conduction band discontinuity
$I_{ds,sat}$	Drain-to-source current in saturation region	ε	Dielectric constant between AlGaN and 2DEG
l_{crit}	Distance from source electrode at which E(x)=Ecrit	μ	Mobility at low electric fields
L_g	Gate length	σ_P	Net polarization charge at heterointerface
n_s	2DEG charge density	φ_B	Schottky barrier height at gate
q	Electron charge		

The uppermost layer in a GaN HEMT (SiN in Figure 3.1) is the passivation layer. The passivation layer is necessary to reduce the effect of current collapse, which is the drastic reduction of drain current as the frequency of operation increases above DC [4]. Figure 3.5 shows the reduction of current in the IV curves of a GaN HEMT. The DC current appears as a typical GaN HEMT, however, when pulsed IV curves are measured the current decreases dramatically as the width of the pulse is reduced. This effect is not fully understood but is widely attributed to dispersion due to surface traps. A sufficiently thick SiN passivation layer is used to reduce the effects of current collapse.

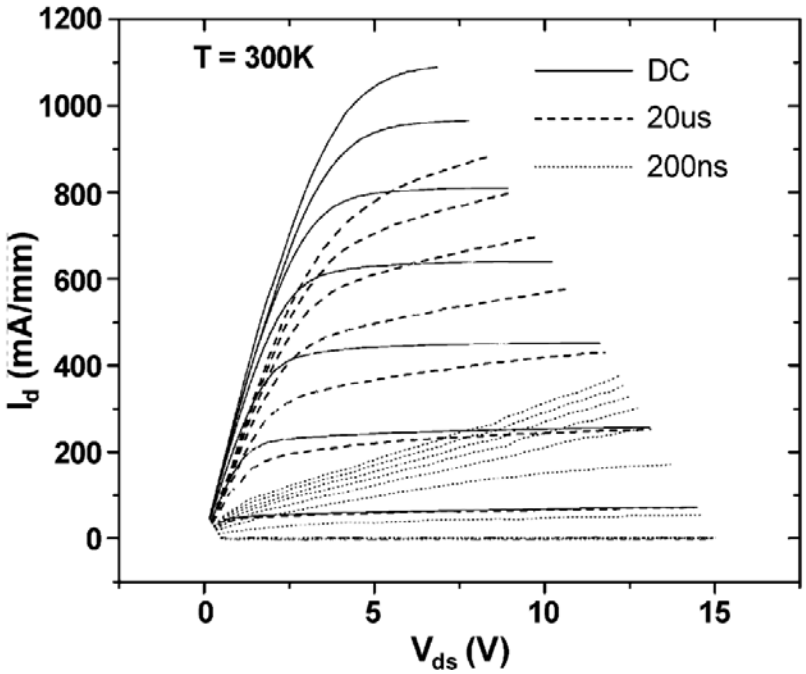


Figure 3.5: Depiction of current collapse in unpassivated GaN HEMT (reproduced from [4]).

3.3. Material & Device Comparison

In order to compare the GaN HEMT to other materials and transistor structures, Table V can first be used to compare material properties of GaN to several other common semiconductor materials [4]. This will be followed by a comparison of the GaN HEMT to several devices used in similar applications.

Some material benefits of GaN that can be observed from Table V include high band gap, high saturation velocity, and high breakdown voltage. These three values are comparable to those of 4H-SiC, however, GaN has the additional benefit of high electron mobility (almost three times higher than 4H-SiC). The benefits of these properties are revealed by observing Johnson's figure of merit (*JFOM*), which takes the product of the breakdown field and saturation velocity to show a material's high frequency power handling capabilities [29]. In Table V, *JFOM* is shown normalized to the value calculated

for silicon for ease of comparison. The value of *JFOM* for GaN is many times higher than those of Si and GaAs as well as being slightly larger than 4H-SiC. The significant advantage GaN has over 4H-SiC is the ability to be used in HEMT structures, whereas SiC is used primarily in bipolar junction transistors (BJT) or junction field effect transistors (JFET). GaN lacks the high thermal conductivity of SiC but can gain thermal benefits by utilizing SiC as a substrate material.

Table V: Material properties related to high frequency power performance (reproduced from [4]).

	Si	**GaAs**	**4H-SiC**	**GaN (bulk)**	**GaN (2DEG)**
E_g (eV)	1.1	1.42	3.26	3.39	3.39
n_i (cm^{-3})	1.5×10^{10}	1.5×10^{6}	8.2×10^{-9}	1.9×10^{-10}	1.9×10^{-10}
ε_r	11.8	13.1	10	9.0	9.0
μ_n (cm^2/V-s)	1350	8500	700	1200	2000
v_{sat} (10^7 cm/s)	1.0	1.0	2.0	2.5	2.5
E_{br} (MV/cm)	0.3	0.4	3.0	3.3	3.3
Θ (W/cm-K)	1.5	0.43	3.3~4.5	1.3	1.3
$JFOM = \frac{E_{br}v_{sat}}{2\pi}$	1	2.9	20	27.5	27.5

A major point of comparison for the HEMT device structure is the MESFET device. MESFETs were the power transistor of choice for high power/high frequency applications before the maturation of HEMT devices [10]. A MESFET differs from a HEMT in that Schottky barrier connections are used for gate, source, and drain connections. Below the gate electrode is a lightly doped semiconductor, typically GaAs, and the drain and source regions are highly doped GaAs. The two device types may be compared in terms of GaAs MESFET and GaAs HEMT. A factor-of-two improvement in mobility and operating frequency is made in HEMT devices versus MESFETS because

the Schottky and channel functions are separated by the confinement of mobile electrons in the 2DEG [10]. At low frequencies, the HEMT exhibits approximately 45% higher output power capabilities than the MESFET and, for increasing frequency, the MESFET output power drops rapidly in contrast to the HEMT [30].

In comparing a GaAs MESFET to a GaN HEMT, the higher power density of GaN allows for smaller devices and lower impedance matching ratios [4] [31]. A lower impedance matching ratio has the benefits of simpler matching networks and broader bandwidth. The GaAs MESFET has inherently higher linearity than the GaN HEMT; however, the GaN HEMT is conducive to predistortion implementations. This is due to the low parasitic losses of the GaN HEMT and because the output power compresses relatively gradually. The lower parasitic losses have the benefit of high efficiency operation in switched mode PA circuits or linear PAs with envelope tracking [31].

3.4. Devices Used

The modeling work described in this thesis was initially necessary because of collaboration between the C.S. Draper Laboratory and the Advanced Semiconductor Materials and Devices Group at MIT. The MIT group was producing GaN HEMT devices for PA design and fabrication by Draper. Additional GaN HEMT devices were purchased from Cree Inc. to test the modeling process on mature devices.

The target operating regime was 1-2 W around 2.5 GHz. The optimal devices size was found to be 500 μm gate-width with a 4 μm drain-to-source spacing. This was determined by modeling and simulating PA circuits as described in the following chapters. The modeling procedure will be described in chapter 4, and the PA design and fabrication procedure will be described in chapter 5.

Chapter 4. Modeling the GaN HEMT

4.1. Motivation

The need for a GaN HEMT device model arose through a project at the C. S. Draper Laboratory involving PA design and fabrication making use of custom GaN HEMT devices from the Advanced Semiconductor Materials and Devices Group at MIT. The goals of the PA project were centered on reducing the physical dimensions and achieving maximum efficiency in a 1-2 W S-band PA. The use of custom transistors requires a method to evaluate device performance in a quick and simple manner. By using an equivalent circuit model, device characteristics related to the desired PA performance may be identified and modified in simulation. This allows quick convergence of optimal device geometry and dimensions in the fabrication cycle. Figure 4.1 shows the design cycle in which the GaN HEMT devices are designed and fabricated, then by modeling the fabricated devices either a new mask may be designed or a PA may be designed and fabricated. This cycle is used to converge on optimally designed GaN HEMT devices to meet the given set of PA requirements.

The extraction of a small-signal model is useful for the immediate and approximate evaluation of a device's ability to achieve design goals. Some characteristics that can be observed from the small-signal model include maximum operating frequency, small-signal gain, and input and output impedances.

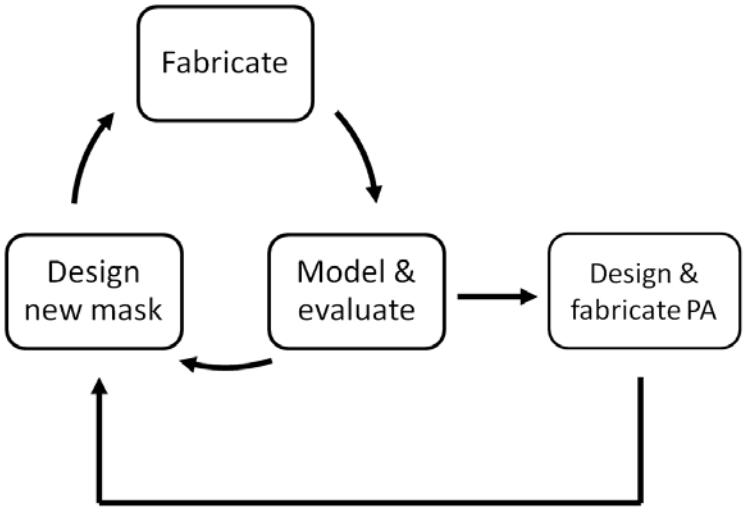


Figure 4.1: Block diagram of the GaN HEMT and PA design cycle.

Current-voltage characteristic measurements (IV curves) are also quite revealing about the performance of a device. From the IV curves it should be apparent what the maximum output power level may be as well as approximate load impedances to achieve specific output power levels [11].

A large-signal model is useful in the design of a PA as it allows nonlinear simulation of entire PA circuits. This allows the exploration and comparison of various PA architectures and the results they might achieve.

4.2. Available Models

There exists a multitude of transistor models for various uses, devices, and applications. Most transistor models can be divided into two groups: physics based or equivalent circuit models. A physics based model is developed by mathematically characterizing the underlying physics of a device structure and its constituent materials whereas an equivalent circuit model is developed by constructing an electric circuit based on standard components that behaves in a manner analogous to the behavior of the device

being modeled. Physics based models are typically used to further understand and explain a specific device structure and/or material and to find the limits of its performance based on physical quantities. An equivalent circuit model is useful in the design of circuits, and by basing the model parameters on measurements of specific devices it can achieve higher precision in terms of electrical properties in a designed circuit than a physics based model.

Some common physics based models of GaN HEMT devices include [32], [33], and [34], however, this work is focused on an equivalent circuit model. Commonly used GaN HEMT equivalent circuit models include the Angelov [35] [5] and EEHEMT [6] models. This work differs by focusing on the ease and speed of extraction for quick turnaround in the device/circuit design cycle as stated above and illustrated in Figure 4.1. The small-signal model presented here is based largely on models described in [36] and [9], which represent a fairly standard and commonly used small-signal HEMT model. A significant benefit of the extraction approach described in [36] is that the need to forward bias the Schottky gate is avoided, whereas other model parameter extraction techniques, such as [9] and [6], rely on forward biasing to extract the channel resistance. Forward biasing the gate could potentially damage a HEMT and to circumvent this need is beneficial.

The large-signal aspect of the presented model is based on [37]. Significant modifications have been made which will be described in the following section.

4.3. Model Development

As mentioned in the preceding section, this work presents a model based on the small-signal characterization of [36] (shown in Figure 4.2) and a modified and elaborated

version of the large-signal model presented in [37] (shown in Figure 4.3). The complete model presented in this work is shown in Figure 4.4 and the measurement setup to acquire all necessary measurements is shown in Figure 4.5. Descriptions of the model parameters are given in Table VI. In the models shown, grey boxes highlight the intrinsic HEMT (e.g. the components that model the dependent current source behavior of the transistor), while outside of the grey box is the extrinsic HEMT (e.g. source, drain, and gate electrode and interconnect parasitics). Development of the model will be described and a procedure will be given to extract necessary model parameters. This chapter will conclude with examples of modeling three distinct GaN HEMT geometries and observations about the devices based on modeling results.

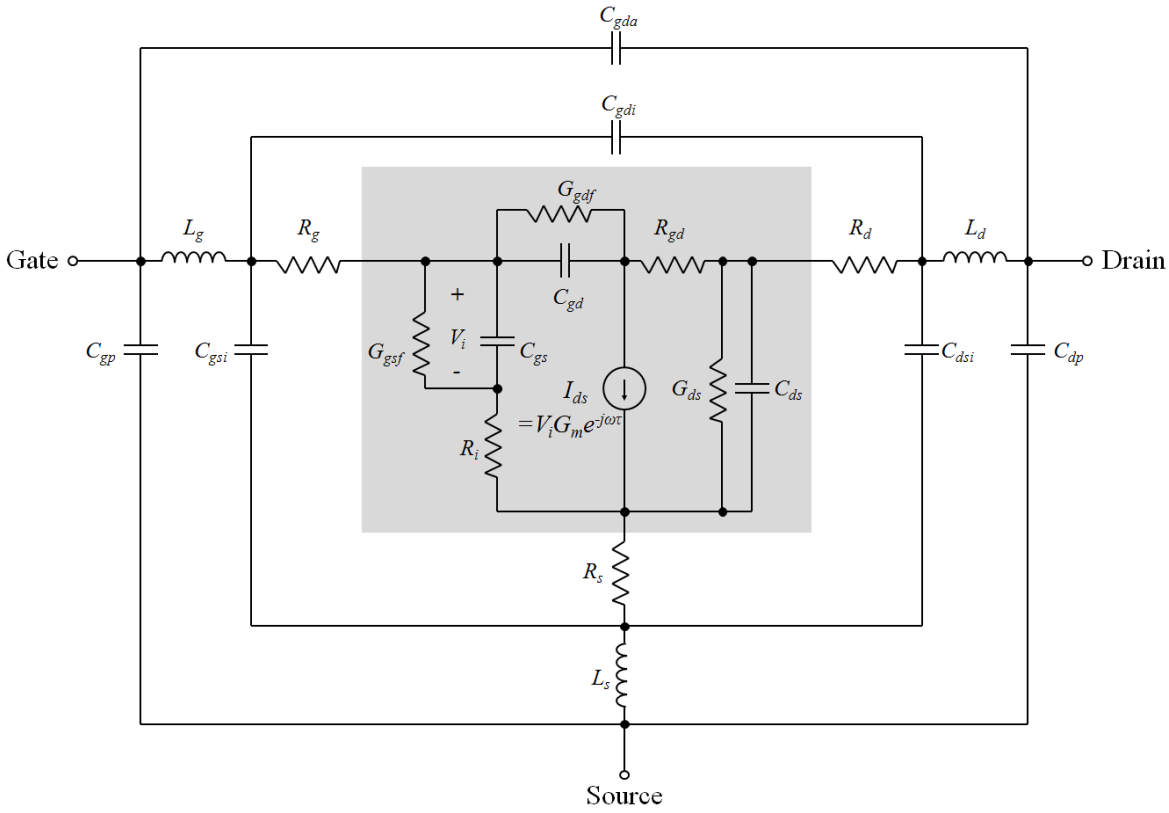


Figure 4.2: Small-signal model as described in [36].

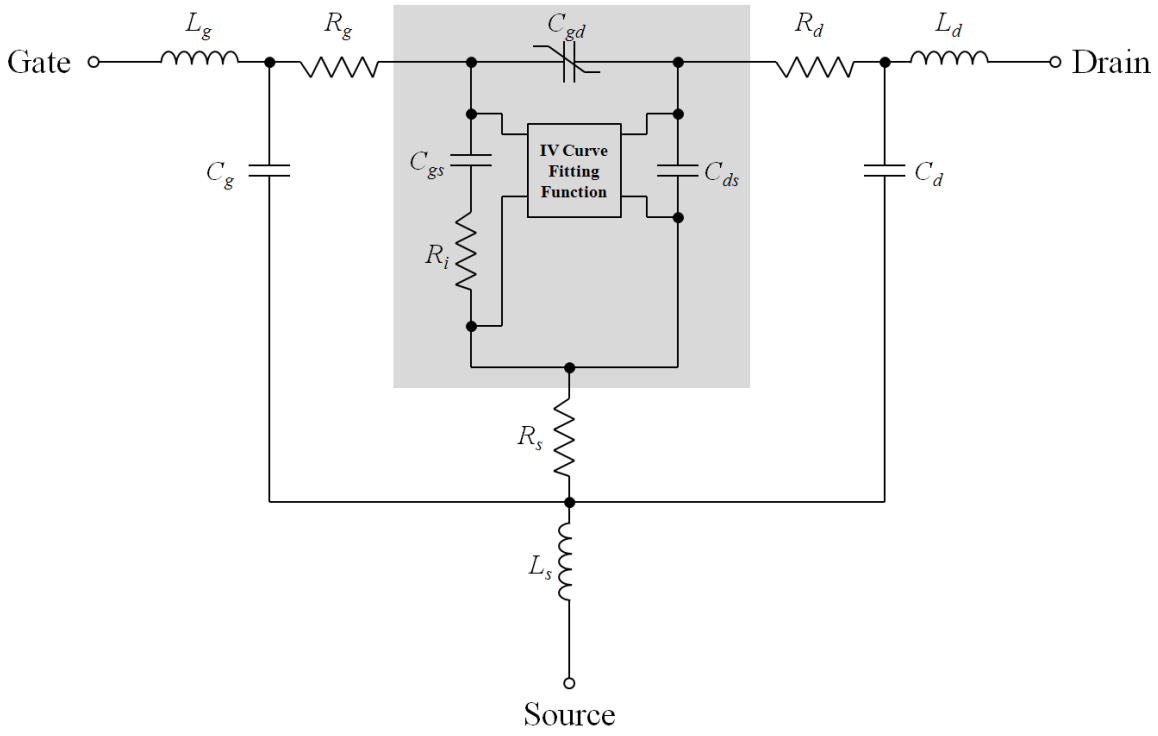


Figure 4.3: Large-signal model as described in [37].

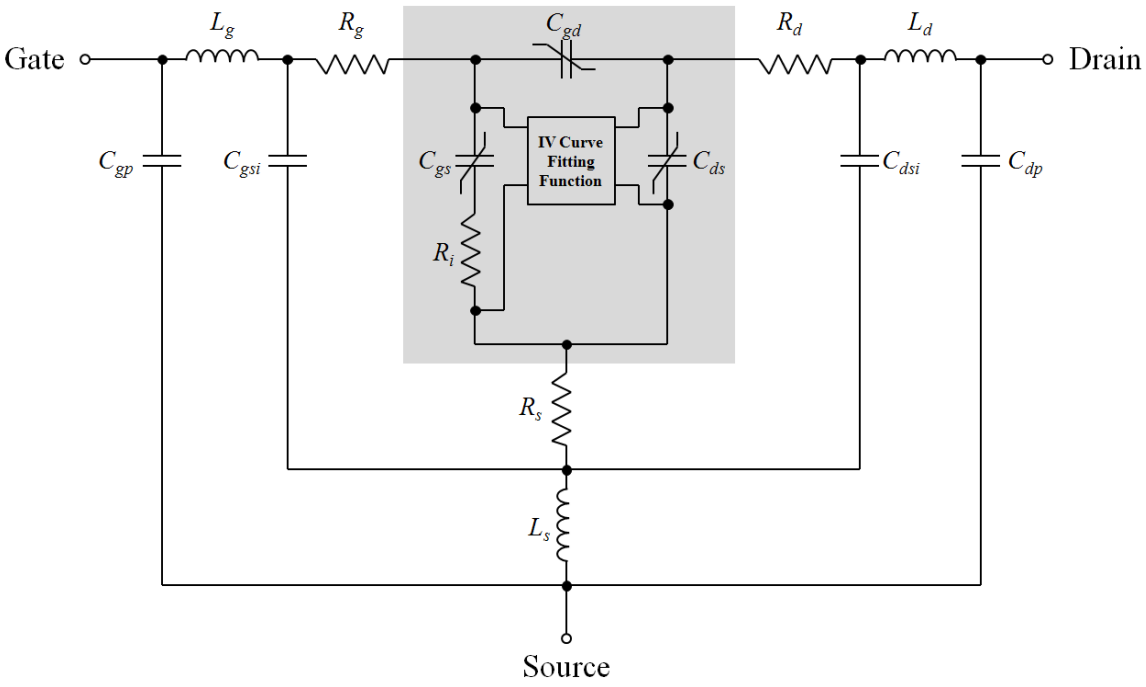


Figure 4.4: The large-signal model proposed in this thesis containing modifications of [36] and [37].

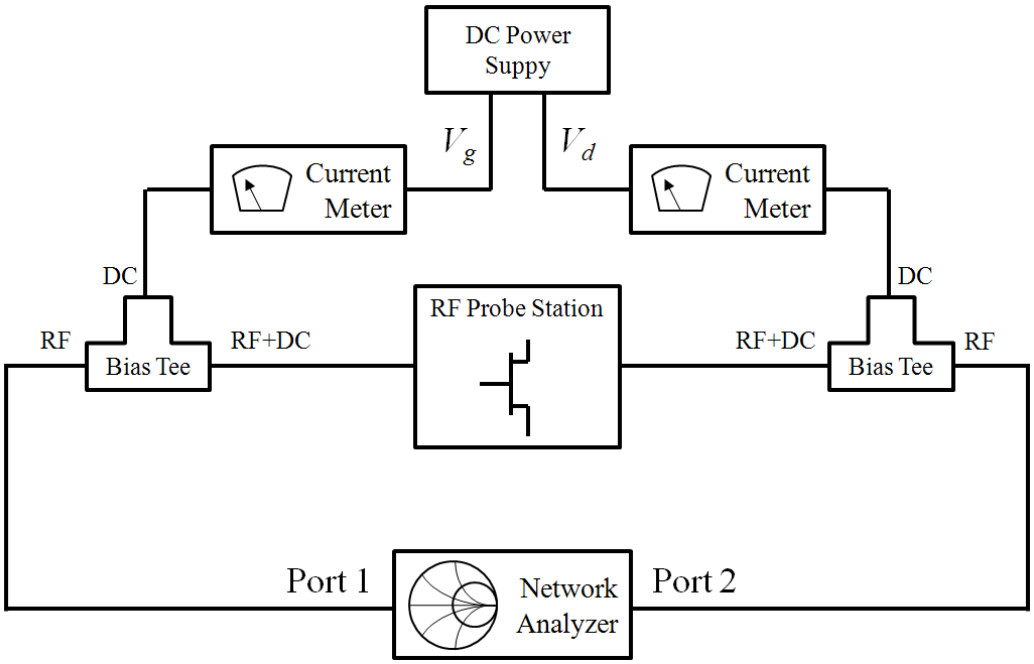


Figure 4.5: Measurement setup for model extraction procedure.

Table VI: Descriptions of model parameters.

Model Parameter	Description
R_g, R_d, R_s	Resistance of gate, drain, and source pads and electrode contacts
L_g, L_d, L_s	Inductance of gate, drain, and source pads
C_{gp}, C_{dp}	Capacitance of gate and drain pads
C_{gsi}, C_{dsi}	Capacitance due to gate and drain interelectrode parasitics
C_{gs}, C_{ds}, C_{gd}	Intrinsic capacitance from gate-to-source, drain-to-source, and gate-to-drain

4.4. Model Extraction

4.4.1. Small-signal Parameters

The model parameters presented in [36] are extracted from S-parameter measurements taken under three bias conditions: pinched, cold, and hot. Each bias

condition will be explained in the context of the parameter extraction procedure below with reference to the circuit in Figure 4.2.

The cold FET bias condition involves setting both V_{gs} and V_{ds} to 0 V. Under the cold bias condition the transistor channel is open but very little or no current is flowing. The equivalent circuit under cold bias is shown in Figure 4.6, where δZ_g, δZ_d, and δZ_s are correction terms describing intrinsic parameters and may be assumed to be sufficiency small as to be ignored. Pad capacitances may also be ignored and interconnection capacitances can be absorbed into the intrinsic capacitance values. It is possible to extract small-signal resistances, capacitances, and inductances from S-parameter measurements under these conditions. By making the assumptions described above and converting the S matrix to a Z matrix the following expression can be used.

$$Z_{11} = R_g + R_s + j\omega\left(L_g + L_s\right) + \frac{1}{j\omega}\left(\frac{1}{C_g} + \frac{1}{C_s}\right) \tag{4.1}$$

$$Z_{22} = R_d + R_s + j\omega(L_d + L_s) + \frac{1}{j\omega}\left(\frac{1}{C_d} + \frac{1}{C_s}\right) \tag{4.2}$$

$$Z_{12} = Z_{21} = R_s + j\omega L_s + \frac{1}{j\omega C_s}. \tag{4.3}$$

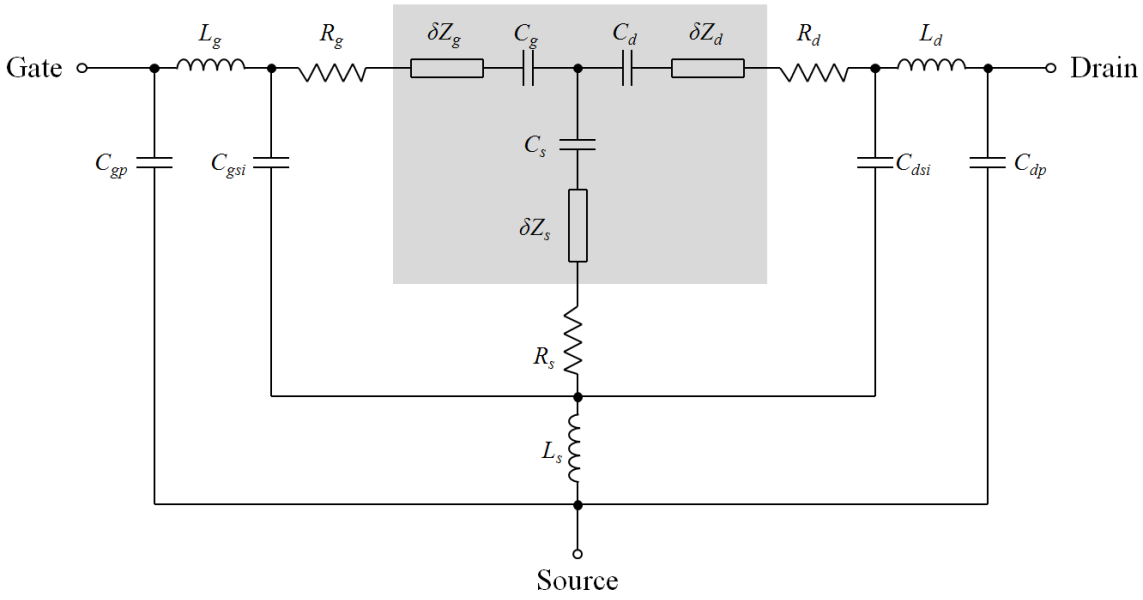


Figure 4.6: Equivalent circuit under cold bias condition.

Intrinsic capacitances and extrinsic inductances are extracted by modifying (4.1), (4.2), and (4.3) to the following expressions:

$$\mathrm{Im}(\omega Z_{11}) = (L_g + L_s)\omega^2 - \left(\frac{1}{C_g} + \frac{1}{C_s}\right) \tag{4.4}$$

$$\mathrm{Im}(\omega Z_{22}) = (L_d + L_s)\omega^2 - \left(\frac{1}{C_d} + \frac{1}{C_s}\right) \tag{4.5}$$

$$\mathrm{Im}(\omega Z_{12}) = \mathrm{Im}(\omega Z_{21}) = L_s\omega^2 - \frac{1}{C_s}. \tag{4.6}$$

By plotting these expressions versus ω^2 the inductance values may be extracted from the slopes of the lines and the capacitance values from the intercept points. This is illustrated in Figure 4.7 for a 2 mm gate width HEMT from Cree which will be discussed further below. These capacitance values, however, will be replaced later in the process by non-linear large-signal values.

The extrinsic resistance values are found in a similar manner using the cold FET measurements. The resistance values may be extracted by modifying (4.1), (4.2), and (4.3) to the expressions

$$\mathrm{Re}(\omega^2 Z_{11}) = (R_g + R_s)\omega^2 \tag{4.7}$$

$$\mathrm{Re}(\omega^2 Z_{22}) = (R_d + R_s)\omega^2 \tag{4.8}$$

$$\mathrm{Re}(\omega^2 Z_{12}) = \mathrm{Re}(\omega^2 Z_{21}) = R_s\omega^2 \tag{4.9}$$

which are plotted versus ω^2 and the resistance values are extracted from the slopes of the lines as shown in Figure 4.8.

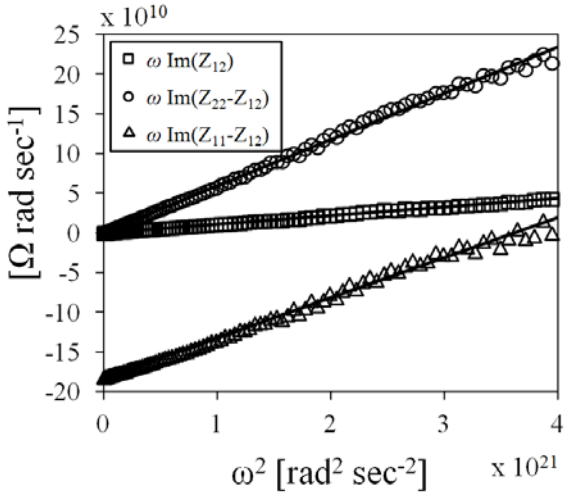


Figure 4.7: Estimation of inductance and capacitance from cold measurements.

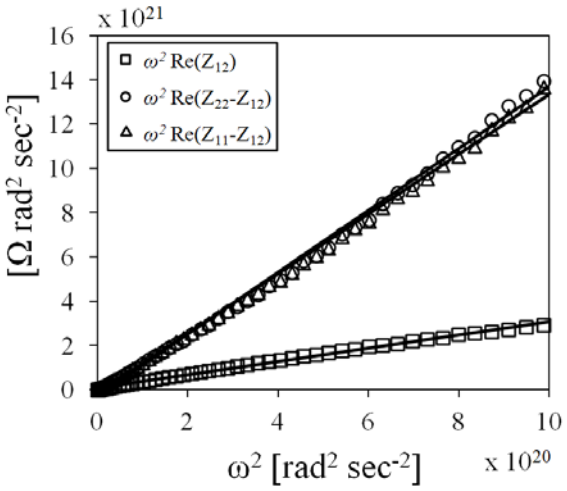


Figure 4.8: Estimation of resistance from cold measurements.

The pinched bias condition is such that $V_{gs} < V_P$ and $V_{ds} = 0$ V. When the HEMT is pinched off it can be seen as a π-network of capacitances at low frequencies (~500 MHz), as shown in Figure 4.9. By converting the S matrix to a Y matrix the following expressions can be written.

$$\mathrm{Im}(Y_{11}) = \omega\left(C_{gp} + C_{gsi} + C_{gs} + C_{gd}\right) \tag{4.10}$$

$$\mathrm{Im}(Y_{22}) = \omega\left(C_{dp} + C_{dsi} + C_{ds} + C_{gd}\right) \tag{4.11}$$

$$\mathrm{Im}(Y_{12}) = \mathrm{Im}(Y_{21}) = -\omega C_{gd}\ . \tag{4.12}$$

Since V_{ds} = 0 it can be assumed that the depletion layer under the gate is symmetric and that

$$C_{gs} = C_{gd}. \tag{4.13}$$

Also, because the gate and drain pads have the same geometry, it can be assumed that

$$C_{gp} = C_{dp}. \tag{4.14}$$

With the two additional empirical assumptions described in [36] and [38], respectively,

$$C_{dsi} = 3C_{dp} \tag{4.15}$$

$$C_{ds} = 12C_{dp}, \tag{4.16}$$

there are seven equations with seven unknowns, thus each capacitance in the π-network may be extracted.

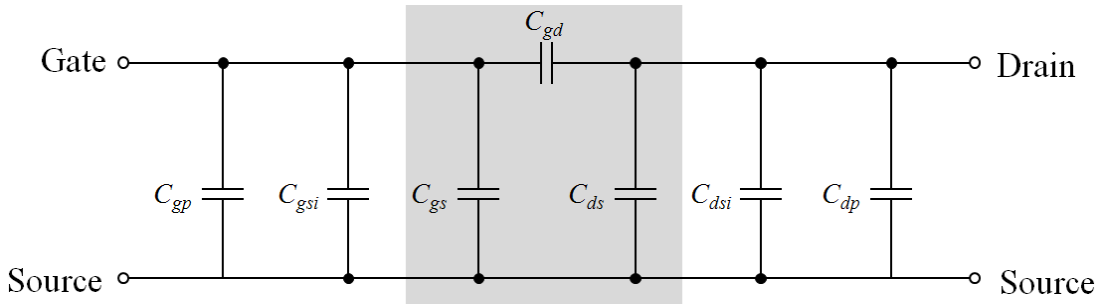


Figure 4.9: Equivalent circuit under pinched bias condition at low frequencies.

The hot measurements are used to extract the intrinsic small-signal parameters, most of which will be discarded and replaced by the large-signal model. The hot FET bias condition is such that the drain current is 50-100% of the maximum operating current. For example this may be V_{gs} = -2 V and V_{ds} = 10 V. These parameters are worth extracting for the purpose of ensuring the model parameters make sense, however, since R_i is the only parameter that is needed for the proposed model its extraction will be the only one described here.

Before extracting intrinsic parameters, the effects of the extrinsic parameters must be accounted for. This accounting is done by de-embedding the extrinsic parameters, which is accomplished in a manner described in detail in Appendix X as modified from [9]. After de-embedding the extrinsic parameters the resulting Y-parameter matrix is used to extract R_i.

$$\mathrm{Re}(Y_{11}) = R_i {C_{gs}}^2 \omega^2. \tag{4.17}$$

Using the value of C_{gs} from the pinched measurements, (4.17) is simply solved for the value of R_i.

4.4.2. Large-signal Parameters

The large-signal behavior of the HEMT is modeled by a current source and three nonlinear capacitances that vary with the instantaneous voltages across them, as shown in Figure 4.4. The modeling procedure is a modified version of that seen in [37] (schematic shown in Figure 4.3) where fitting functions for I_g, I_d, and C_{gd} were proposed. As explained below, the model proposed here includes fitting additional capacitances, modification of the capacitance fitting function, and the omission of I_g modeling.

For the purpose of this model, I_g was found to be small enough that it had no noticeable effect on the model's performance. The nonlinear current source, I_d, models the DC drain current characteristics of a GaN HEMT based on a standard set of DC IV curves. It uses the fitting function:

$$I_{ds} = \begin{cases} \dfrac{I_{ds0}}{1 + (\delta V_{ds} + \lambda V_{gs}) I_{ds0}} & V_g > V_p \\ \dfrac{V_{ds}}{R_{off}} & V_g \leq V_p \end{cases} \tag{4.18}$$

$$I_{ds0} = \beta (V_{gs} - V_p)^Q \tanh(\alpha V_{ds}). \tag{4.19}$$

V_{ds} and V_{gs} are control voltages and V_p is the device's pinch off voltage. The parameter α determines the voltage, V_{ds}, at which the current begins to saturate and β is a simple scaling parameter [39]. The parameters δ and λ describe the decrease in I_{ds} for high V_{ds} and V_{gs} values and the parameter Q describes the non-square law behavior observed in HEMTs [40] [37]. When the device is pinched-off, R_{off} represents the drain-to-source resistance. As described in chapter 3, there is a difference between the measured values of DC IV curves and pulsed IV curves. Although the operation of a PA has more in

common with pulsed IV curves, in a properly passivated device, the only significant difference occurs in the high power region of the IV curves (large current at high V_{ds}) which is a region largely avoided in PA transients.

The large-signal behavior of intrinsic capacitances were modeled by extracting small-signal capacitance values, using pinched S parameter measurements as described in section 4.4.1, with the HEMT biased at various values equivalent to the instantaneous voltages seen in large-signal PA operation. An example of these values is shown in Table VII. The approach is discussed in [37] and was elaborated on and modified significantly for this work by altering the fitting function and including additional nonlinear capacitance modeling for C_{gs} and C_{ds}.

Table VII: Example bias voltages for extraction of nonlinear capacitances.

V_{ds} (V)	V_{gs} (V)	$V_{dg} = V_{ds} - V_{gs}$ (V)
0	-6 – 0	0 – 6
0 – 20	-6	6 – 26

The nonlinear gate-to-drain capacitance, C_{gd}, was found to behave differently from one device to another. As a result new fitting functions were developed for each device. The empirical function

$$C(v) = a + b\tanh\big((v - v_0) + c\big) \tag{4.20}$$

was found to provide a suitable fit for one device type. a, b, c, and v_0 are empirical fitting parameters and v is the voltage across the capacitor. Equation (17) was a good fit for C_{gs}, with respect to V_{gs} as well. C_{ds} varied only slightly and was left as the constant determined in the small-signal fitting procedure. For another device type, the fitting function

$$C(v) = a + \frac{b}{c + (v - v_0)^2} \tag{4.21}$$

was used for fitting C_{gd} and (4.17) was used for fitting C_{gs}. Examples of these fitting functions are shown in Figure 4.10 and examples of extracted values using the fitting functions are shown in the following section.

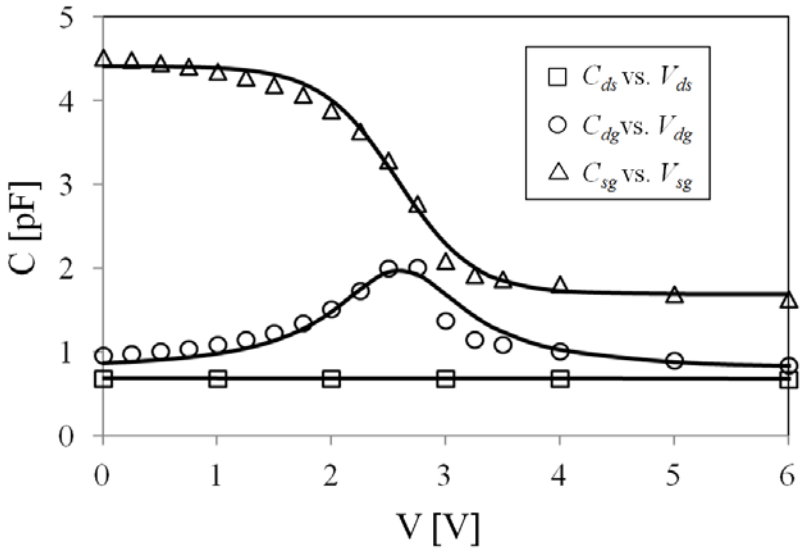


Figure 4.10: Extracted capacitance values and fitting functions. C_{ds} maintains a constant value, C_{dg} is fit using (4.21), and C_{sq} is fit using (4.20).

A final optimization of nonlinear current and capacitance model parameters was performed in the CAD software Agilent ADS to incorporate the large-signal elements into the context of the extrinsic parameters modeled earlier. This is done because otherwise the IV characteristics of the HEMT would account for the extrinsic resistances twice (once in fitting to the DC IV curves and once within the small-signal model). Also the extrinsic capacitances would be accounted for twice in a similar manner.

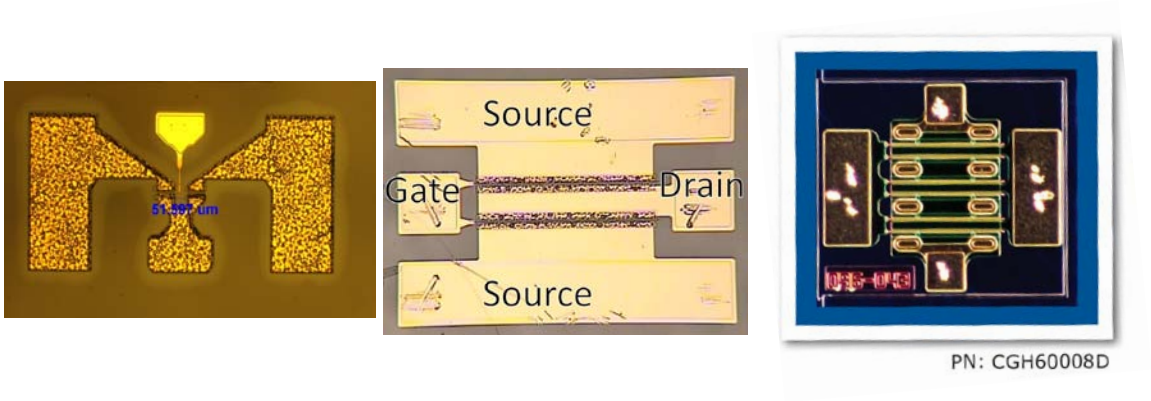
4.5. Modeling Examples

The described modeling procedure has been applied to several GaN HEMT devices of three different geometries. Figure 4.11 shows photographs of the three geometries. The devices in Figure 4.11 (a) and (b) are 500 μm gate-width devices designed and fabricated at MIT and are referred to as T-gate and U-gate, respectively. Figure 4.11 (c) shows a 2 mm gate-width Cree HEMT, CGH60008D, which was modeled and used to design and fabricate a PAs to demonstrate the validity of the model.

Table VIII shows typical extracted small-signal model parameters of the three device geometries. The small-signal performance of the model versus measured values for the Cree HEMT are shown in Figure 4.12 (cold bias condition), Figure 4.13 (pinched bias condition), and Figure 4.14 hot bias condition). The markers shown in the figures indicate 2.5 GHz, the emphasized frequency of the fitting procedure.

The nonlinear capacitance values extracted from S parameter measurements are shown in Figure 4.15 along with the resulting fitting functions.

Figure 4.16 shows a comparison of the measured DC IV curves to the fitting function described above. The curves shown are from the Cree HEMT and values of V_{gs} range from -1 V to -3.5 V in 0.5 V steps. Emphasis was placed on the low V_{ds} values area of the IV curves because this region represents the region of operation of a switching PA.



(a) (b) (c)

Figure 4.11: Geometries of three device types modeled. (a) MIT 500 µm T-gate, (b) MIT 500 µm U-gate, and (c) Cree 2 mm CHG60008D.

Table VIII: Typical extracted small-signal parameter values for three HEMT geometries.

Device Type	MIT – T (500 µm)	MIT – U (500 µm)	Cree (2 mm)
R_g **(Ω)**	10	16	1
R_d **(Ω)**	3	4	1
R_s **(Ω)**	2	2	0.25
R_i **(Ω)**	1	2	3
L_g **(pH)**	44	10	21
L_d **(pH)**	51	49	33
L_s **(pH)**	0	0	11
C_{gp} **(fF)**	6	6	41
C_{dp} **(fF)**	6	6	42
C_{gsi} **(fF)**	0	0	571
C_{dsi} **(fF)**	18	18	125
C_{gs} **(fF)**	1360	1000	4264
C_{ds} **(fF)**	70	74	589
C_{gd} **(fF)**	32	27	861

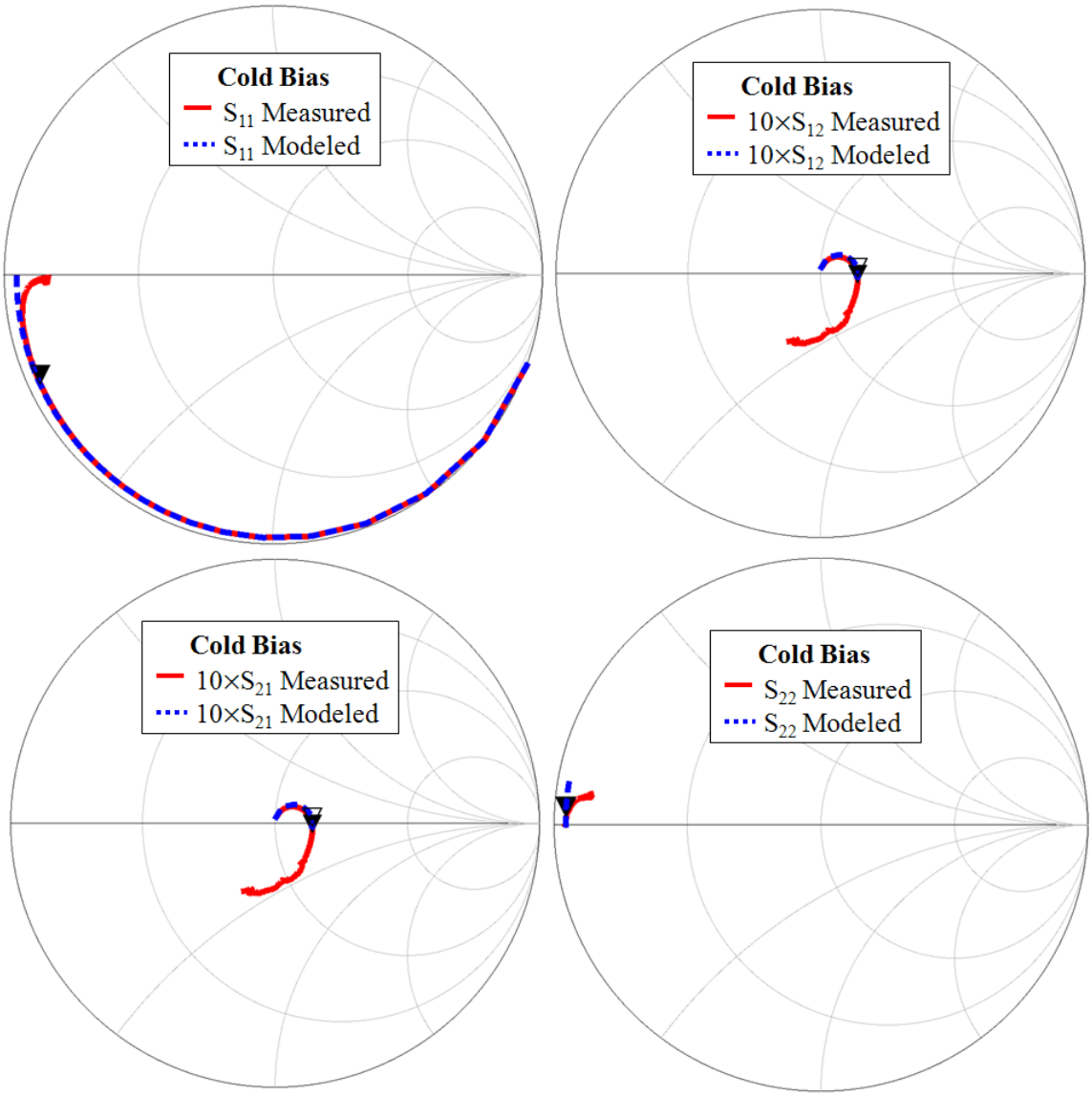


Figure 4.12: Cree HEMT small-signal measurements vs. model under cold bias condition.

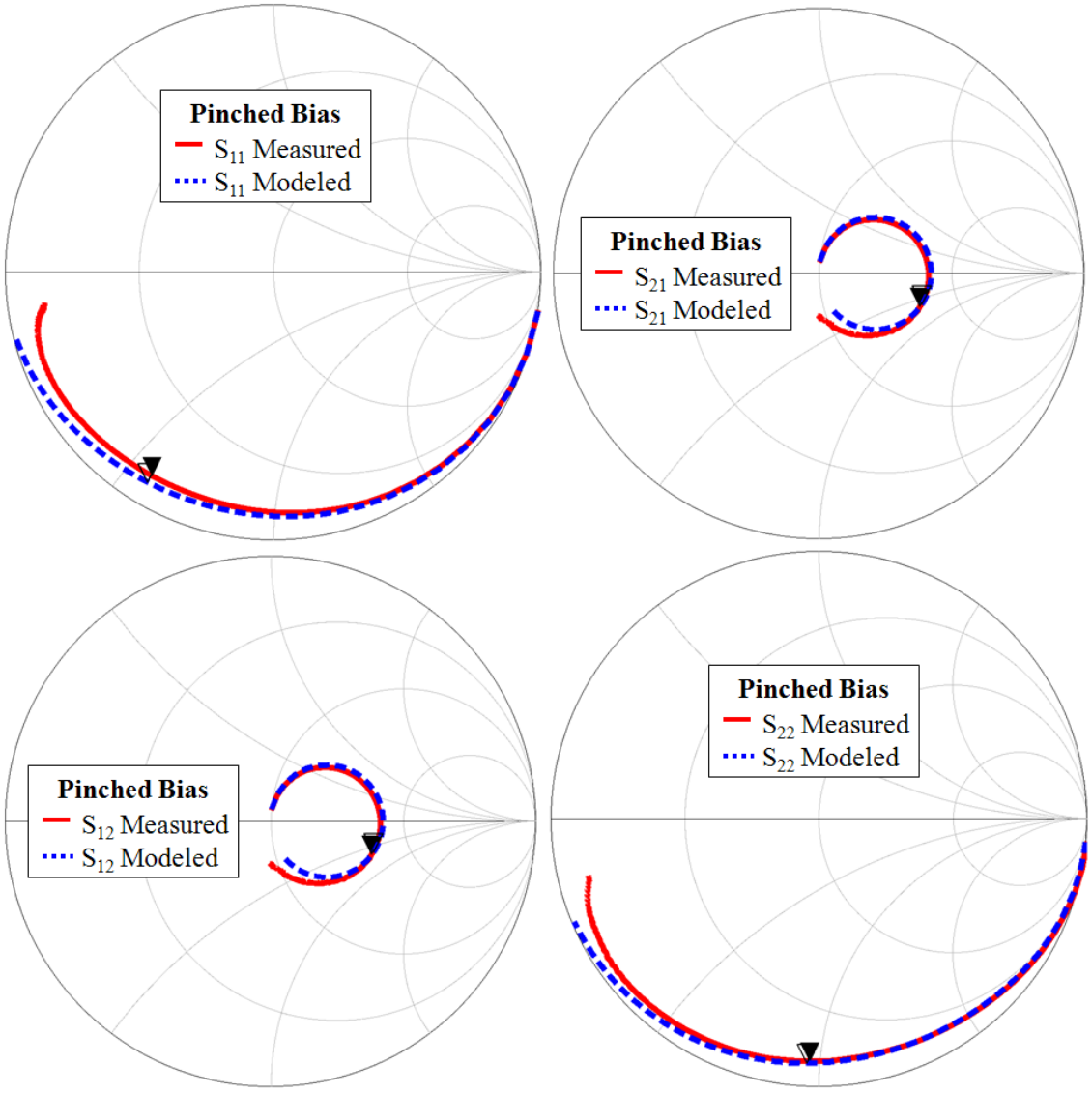


Figure 4.13: Cree HEMT small-signal measurements vs. model under pinched bias condition.

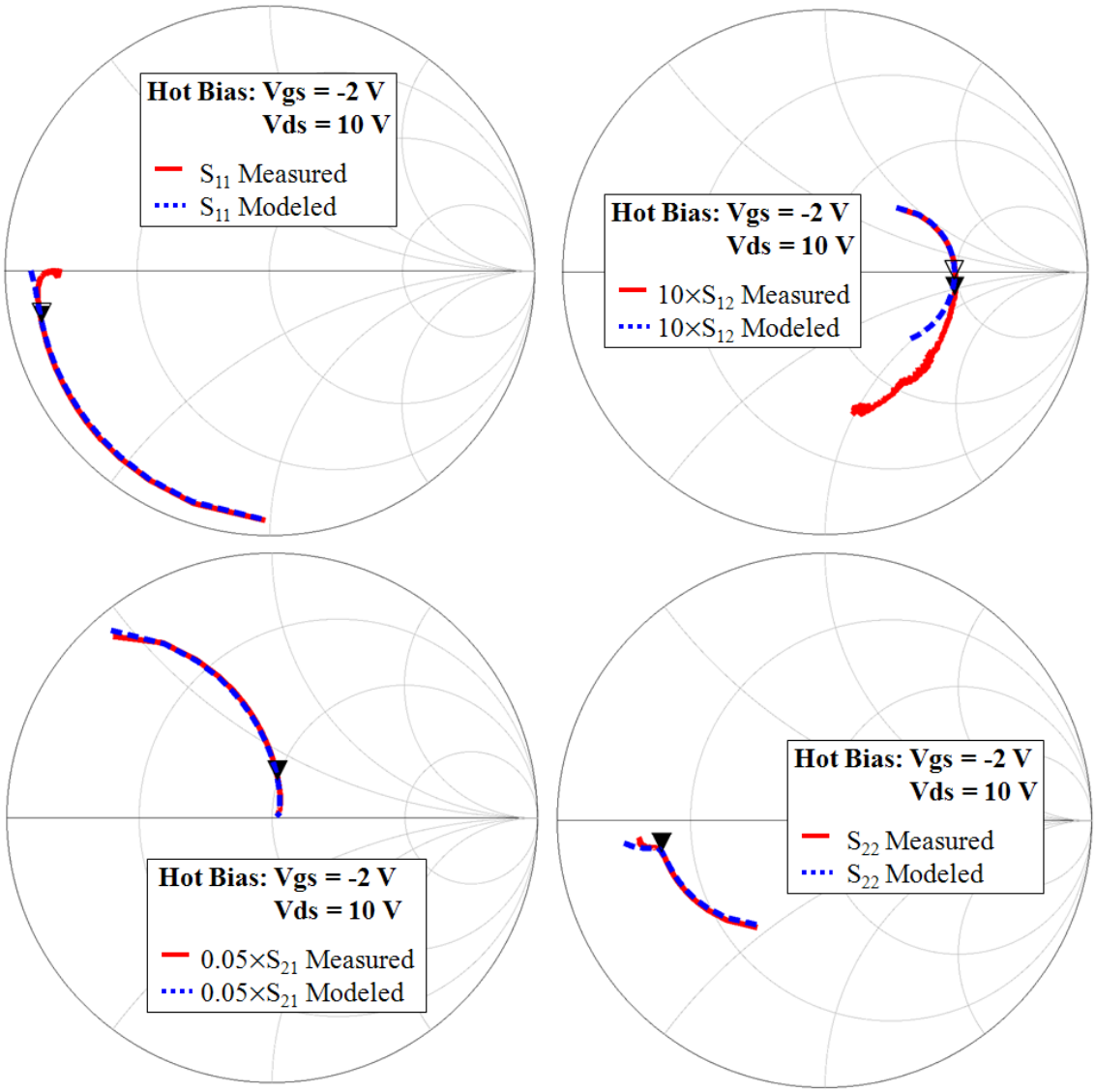
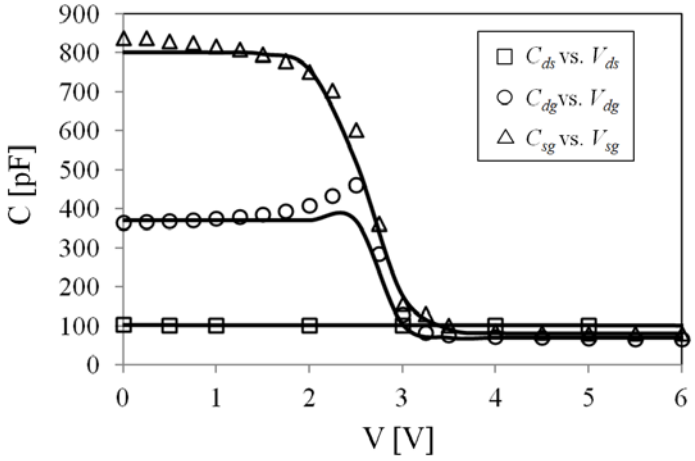
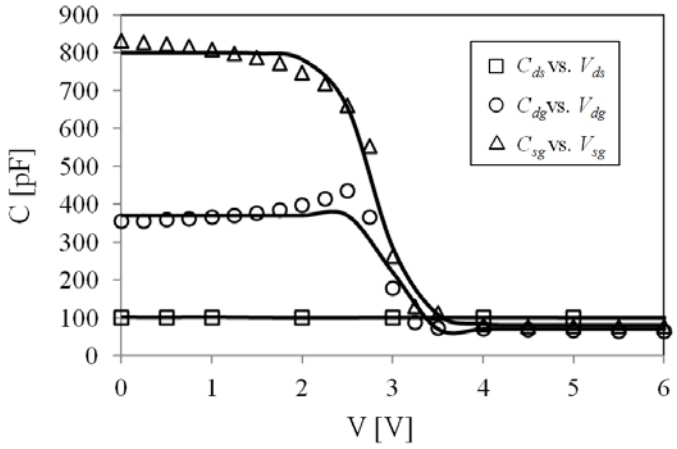


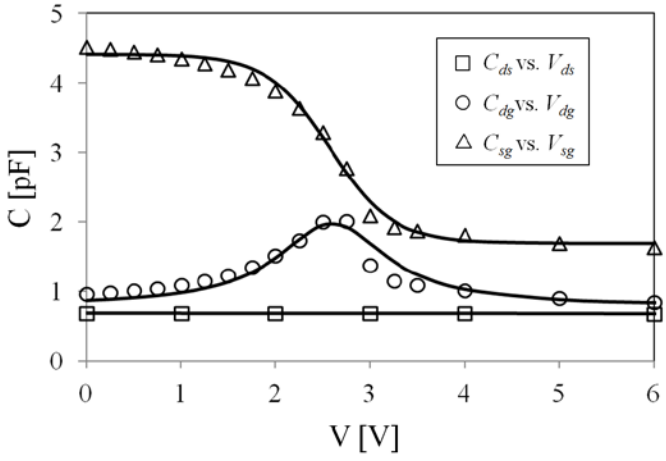
Figure 4.14: Cree HEMT small-signal measurements vs. model under hot bias condition, V_{gs} = -2 V and V_{ds} = 10 V.



(a)



(b)



(c)

Figure 4.15: Extracted nonlinear-capacitance values and fitting functions for three HEMT geometries. (a) MIT 500 µm T-gate, (b) MIT 500 µm U-gate, and (c) Cree 2 mm CHG60008D.

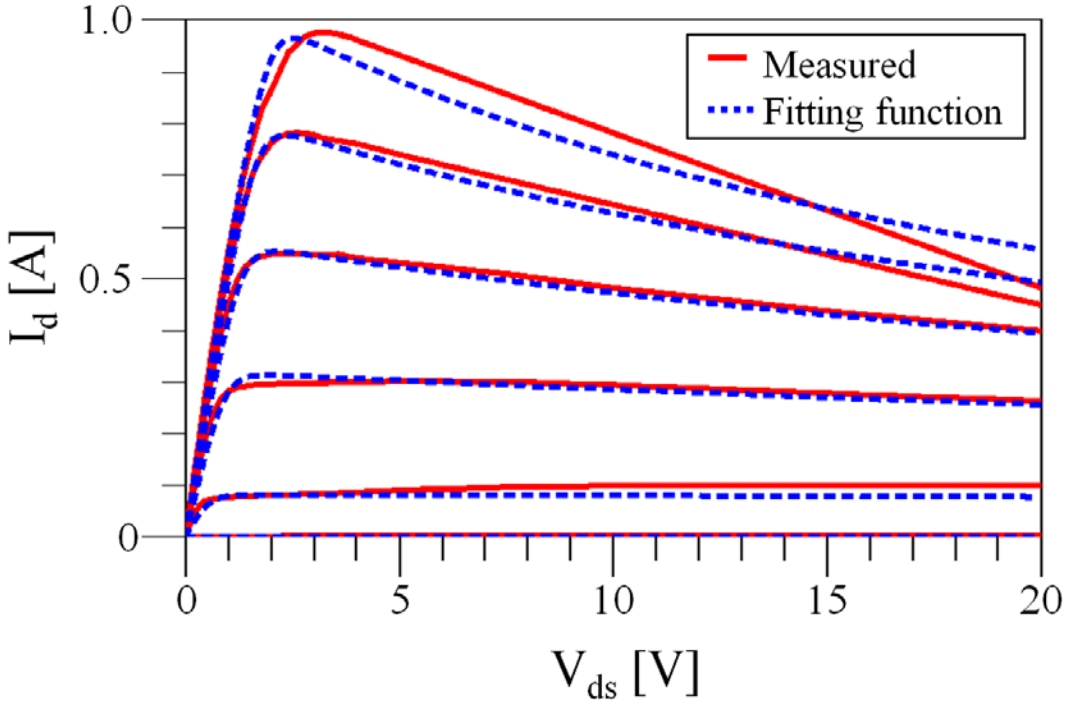


Figure 4.16: DC IV curves measured and from fit (using (4.18) and (4.19)) of 2 mm Cree HEMT.

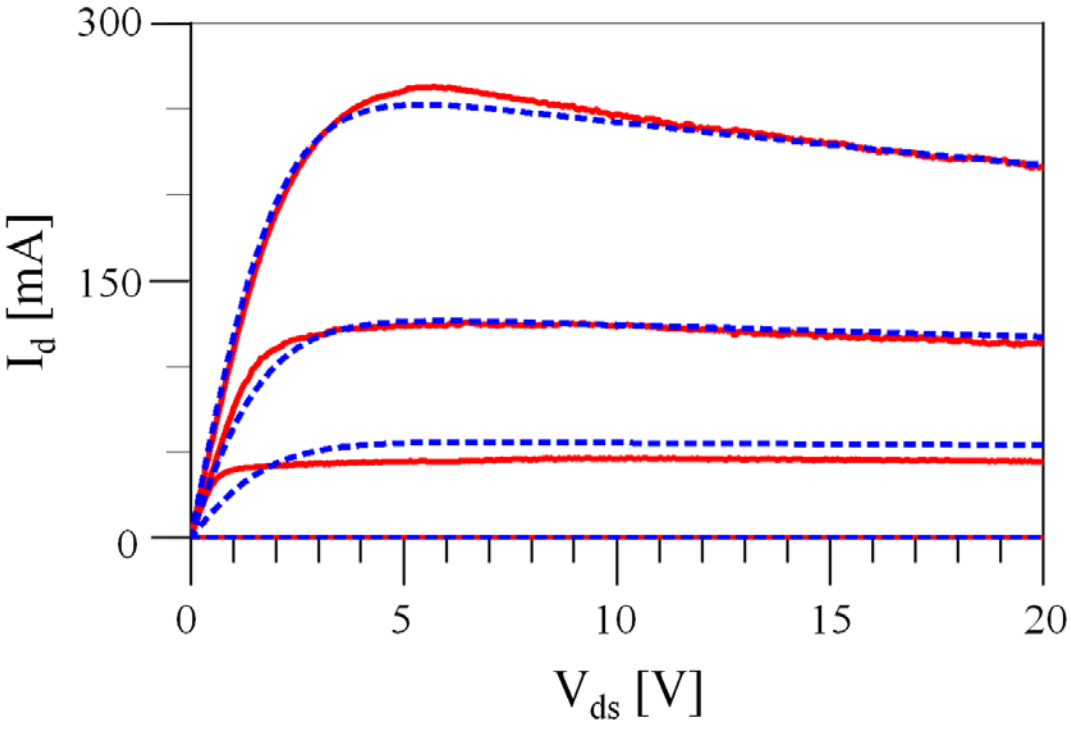


Figure 4.17: DC IV curves measured and from fit (using (4.18) and (4.19)) of 500 µm MIT devices.

Chapter 5. PA Design & Model Verification

5.1. Introduction

Validation of the model was accomplished by designing, fabricating, and testing PA circuits based on simulations utilizing the large-signal model. The initial motivation for the modeling effort was to aide in the design of a high efficiency switching PA at 2.5 GHz with 1-2 W peak output power. Through the development of the model it seemed likely that the model would also work well in a linear PA regime. Two PAs were designed and fabricated: one operating in class AB and one operating in class E. Both PA circuit were designed using the Cree CGH60008D GaN HEMT device modeled above in chapter 4. This chapter describes the design, fabrication, and measurement of these two PAs. An analysis and discussion of the PA results is found in chapter 6, where the model simulations are compared to measurements of the fabricated PA circuits.

By demonstrating the validity of the large-signal model in class AB and class E operation, the model is demonstrating a capacity to describe the essential behaviors of all single stage PA classes described in chapter 2.2 and thus the architectures described in chapter 2.3 as well. This makes the described model useful in the evaluation of the modeled device in a broad array of PA circuits and systems.

An overview of the PA design procedure is shown in as a flowchart in Figure 5.1. The procedure begins with choosing a bias point from the transistor IV curves. From there load/source-pull simulations are performed using the large-signal model to determine input and output impedance values to achieve desired PA performance. The determined impedance values are used as reference values when designing input and output matching networks using ideal passive component models. The ideal networks are

then used as references to design matching networks using modeled passive components, substrate, and interconnecting metal traces. ADS Momentum software is used to layout the circuit as well as perform EM simulations as the final step before fabricating and testing the PA circuit. These steps will be discussed in further detail below.

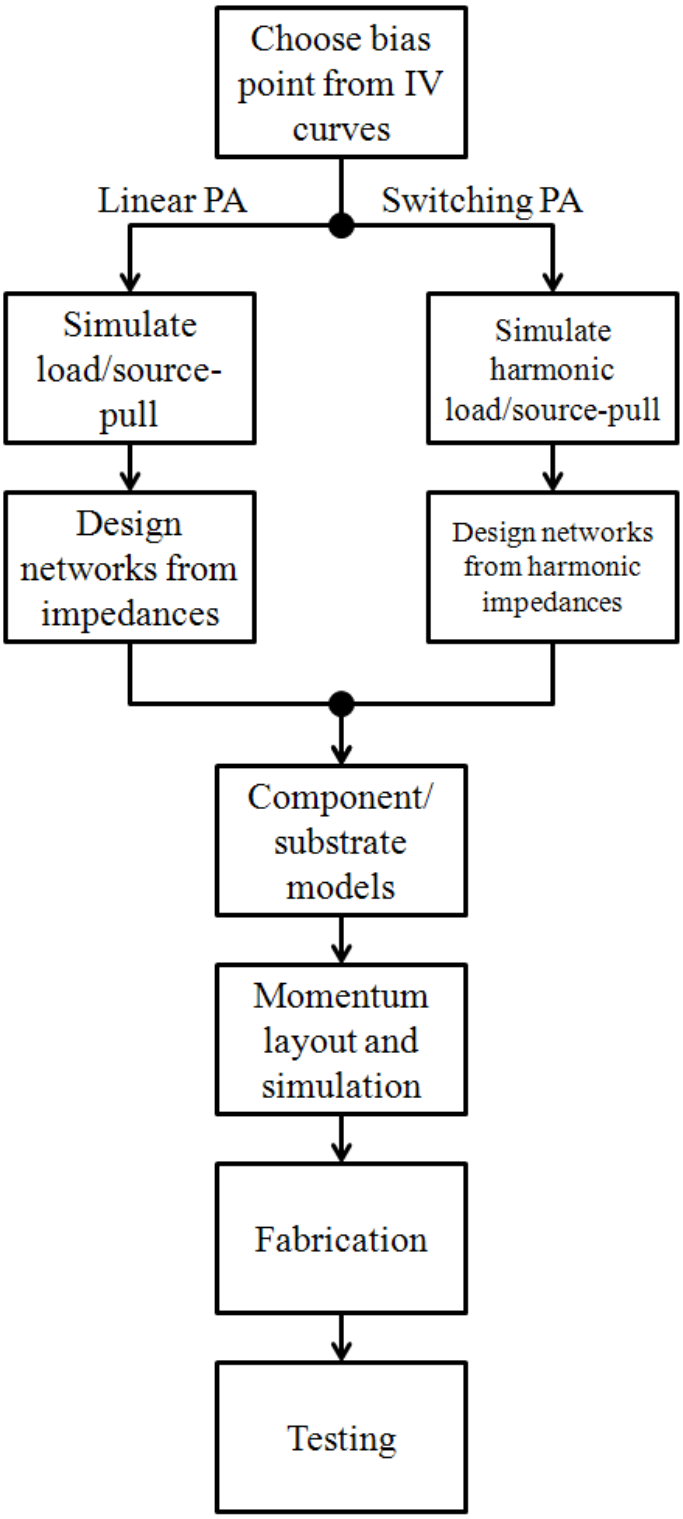


Figure 5.1: Flowchart of PA design procedure.

5.2. Linear PA

5.2.1. Design Procedure

The design of a class AB PA began with inspection of the DC IV curves. From the IV curves, the approach described in [11] was used to select a bias point and estimate the load impedance using load-line analysis. An initial bias point for a class A PA can be chosen using

$$P_{out} = \frac{V_{dc}\frac{I_{max}}{2}}{2} = \frac{V_{dc}I_{dc}}{2}, \tag{5.1}$$

where P_{out} is the desired fundamental output power, V_{dc} is the DC drain supply voltage, I_{max} is the maximum transient drain current, and I_{dc} is the DC drain current. Equation (5.1) can be rewritten as

$$I_{dc} = \frac{2P_{out}}{V_{dc}} \tag{5.2}$$

to determine the bias current level for some given output power and drain supply voltage. In this case the drain bias voltage was chosen to be 15 V and the output power was chosen as 1 W, resulting in a class A bias current, I_{dc}, of 133 mA. From the IV curves shown in Figure 5.2 an estimated gate bias voltage can be chosen as –2.4 V for a 1 W class A PA using the Cree HEMT. To adjust this bias point for class AB operation the gate bias is reduced to some value between –2.4 volts and the pinch off voltage of the HEMT (in this case -3.0 V). The value chosen was -2.9 V.

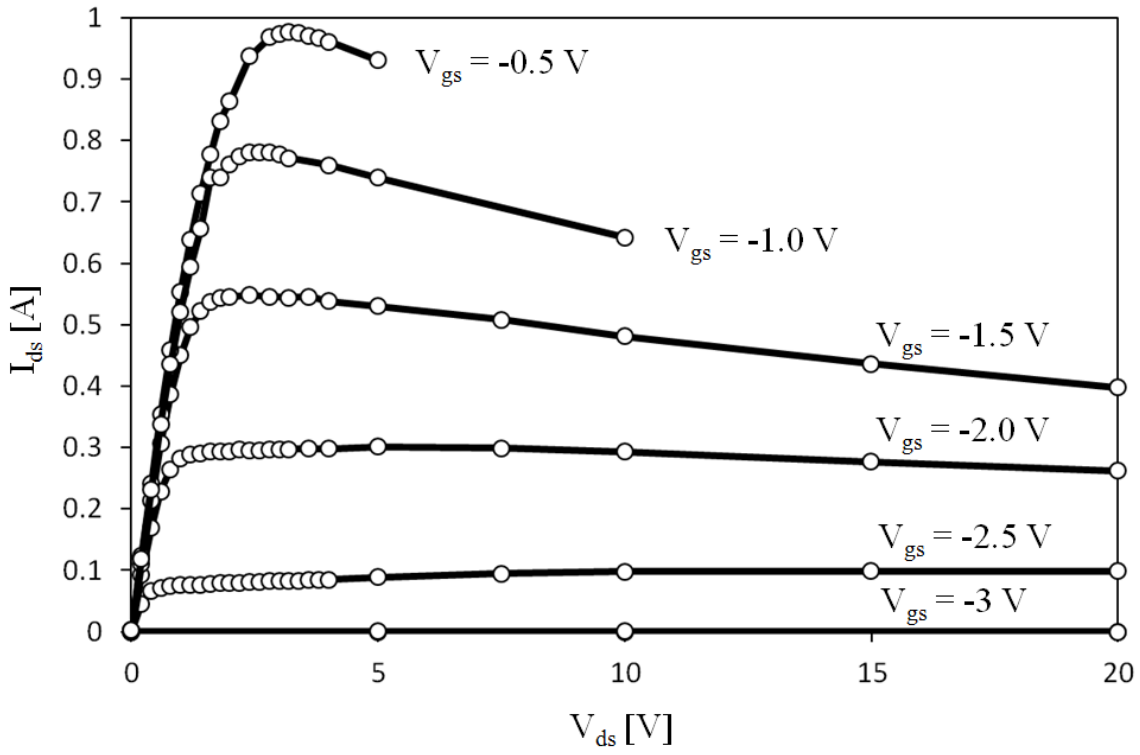


Figure 5.2: measured IV curves of Cree HEMT.

A load/source-pull simulation was performed using the large-signal model describe in chapter 4 in the computer aided design software Agilent Advanced Design System (ADS) [11]. The load-pull procedure was performed under a variety of gate bias voltages and for various input power levels to converge on a load impedance that gives the desired performance.

With the input and output impedance values determined by the load/source-pull simulation as references, input and output matching networks were designed using ideal passive components in ADS. For the input network a low-pass impedance transform was used to achieve the input impedance 5.3-j4.3 Ω and a high-pass impedance transform was used on the output to achieve the output impedance 12.6+j36.1 [41]. Figure 5.3 shows the PA circuit; Figure 5.4 shows the gain, fundamental output power, and PAE of the PA

circuit; and Figure 5.5 shows the harmonic power when the PA is operating at maximum PAE.

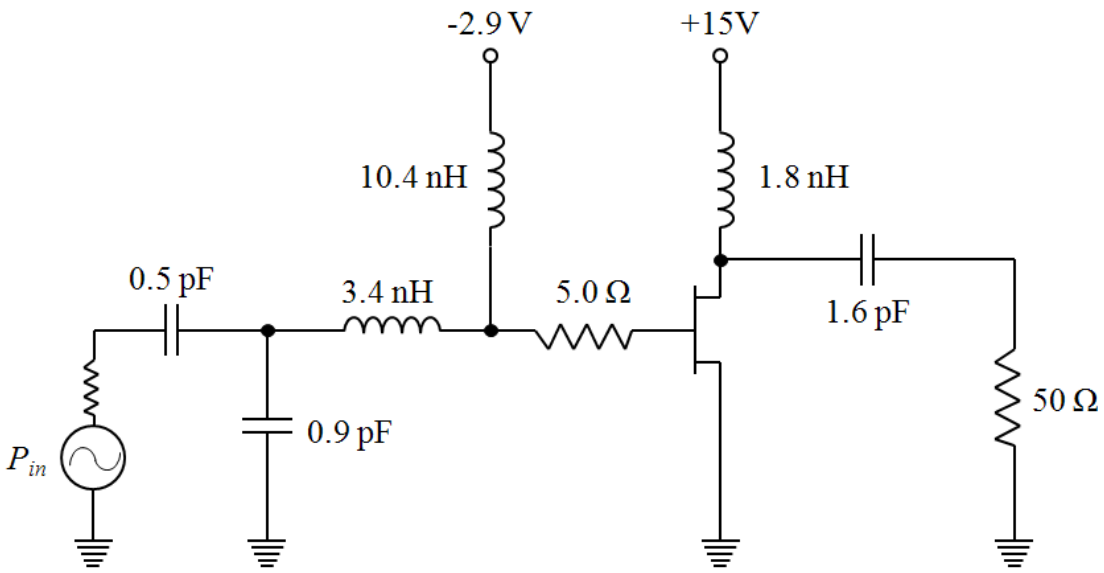


Figure 5.3: Class AB PA circuit schematic using ideal passive component models.

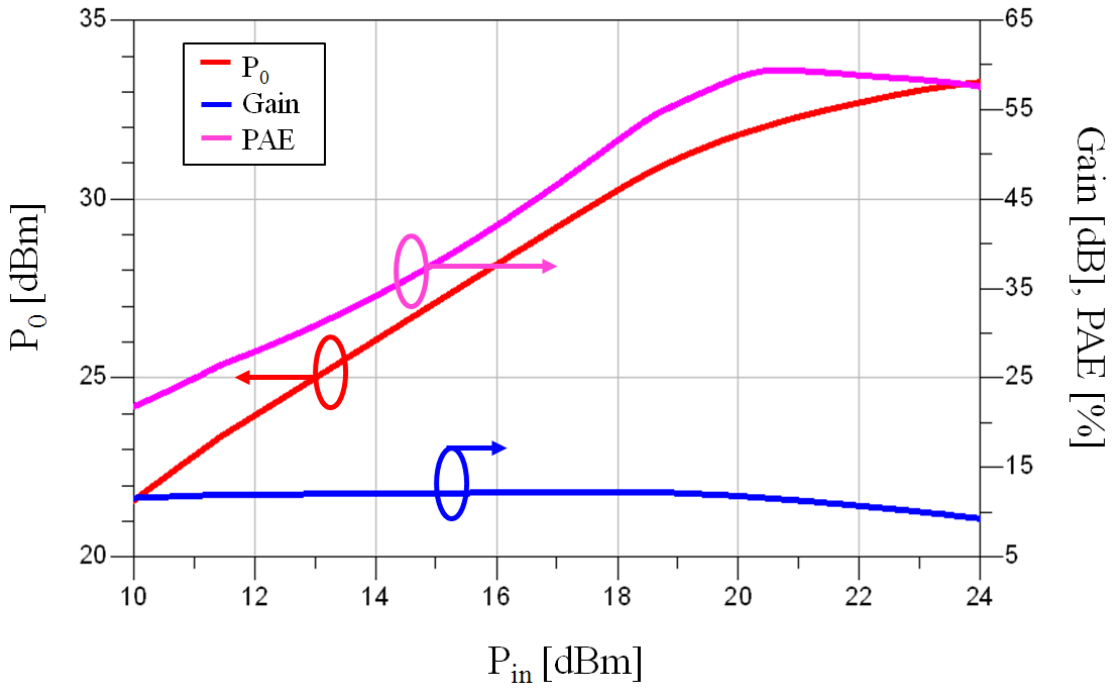


Figure 5.4: Simulation results of class AB PA with ideal component models.

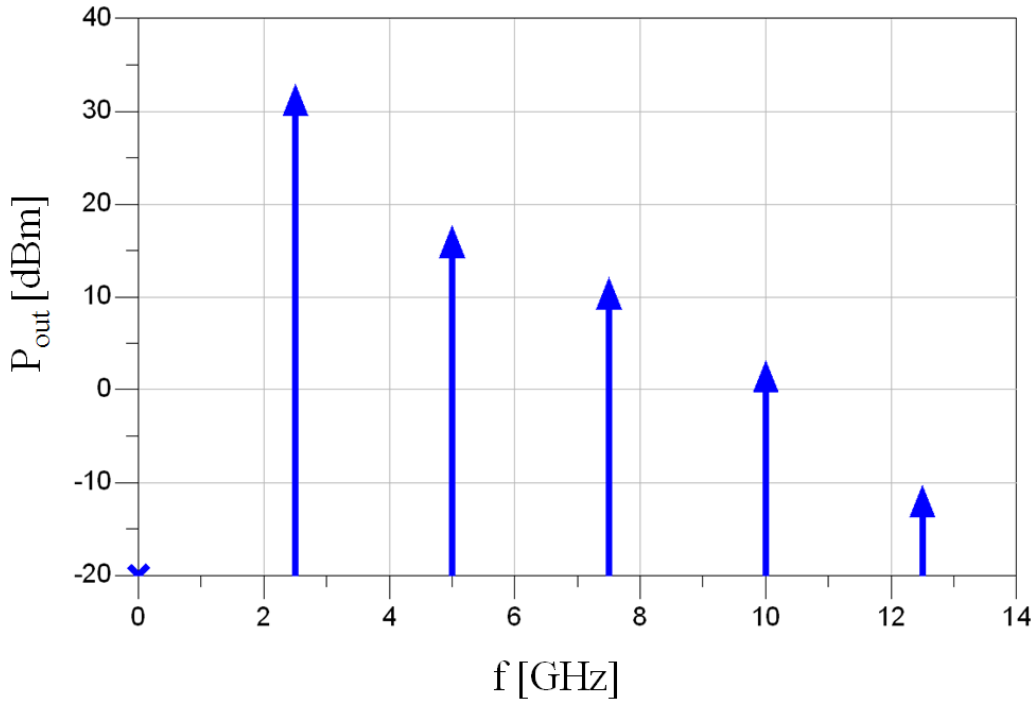


Figure 5.5: Class AB simulation of harmonic power at maximum PAE with ideal component models.

From the input and output networks realized using ideal passive components the next step was to use more realistic component models (resistor and capacitor models by Modelithics and inductor models by Coilcraft). In addition to these passive component models was the inclusion of metal trace interconnects and substrate models. The substrate used was TMM-13i by Rogers Corp., which is a 15 mil thick dielectric with dielectric constant 12.85 and 0.7 mil thick conductor with conductivity 5.69×10^7 S/m [42].

At this point it was necessary to plan the overall dimensions of the PA circuit board and the position of RF and DC connectors. This will be shown below when the circuit layout is described. With the inclusion of parasitics of the interconnect traces and modeled passive components, it was necessary to adjust component values and make subtle changes to the input and output network architectures.

The resulting circuit schematic including the modeled components, layout traces, and substrate is shown in Figure 5.6 and the simulated results are shown in Figure 5.7 and Figure 5.8.

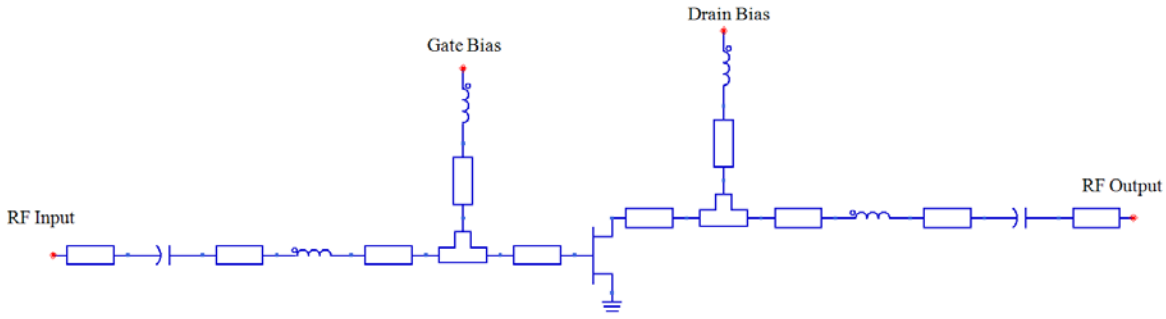


Figure 5.6: Class AB PA circuit schematic including modeled passive components, substrate, and metal interconnects.

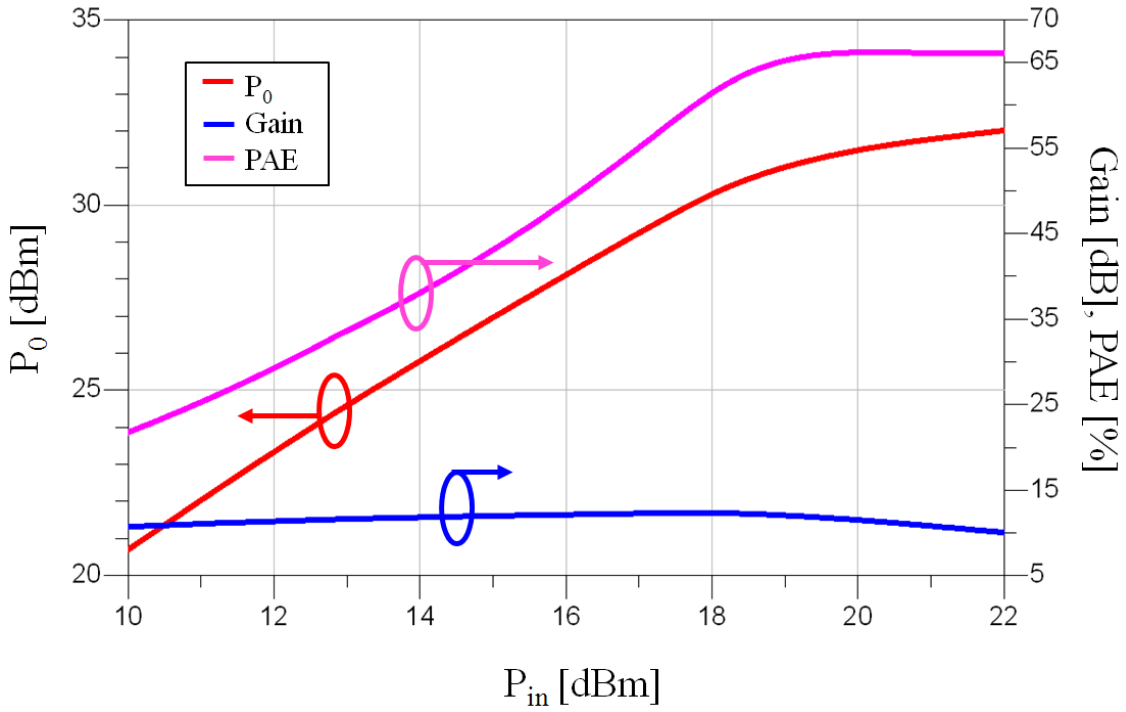


Figure 5.7: Simulation results of class AB PA with modeled components, substrate, and interconnects.

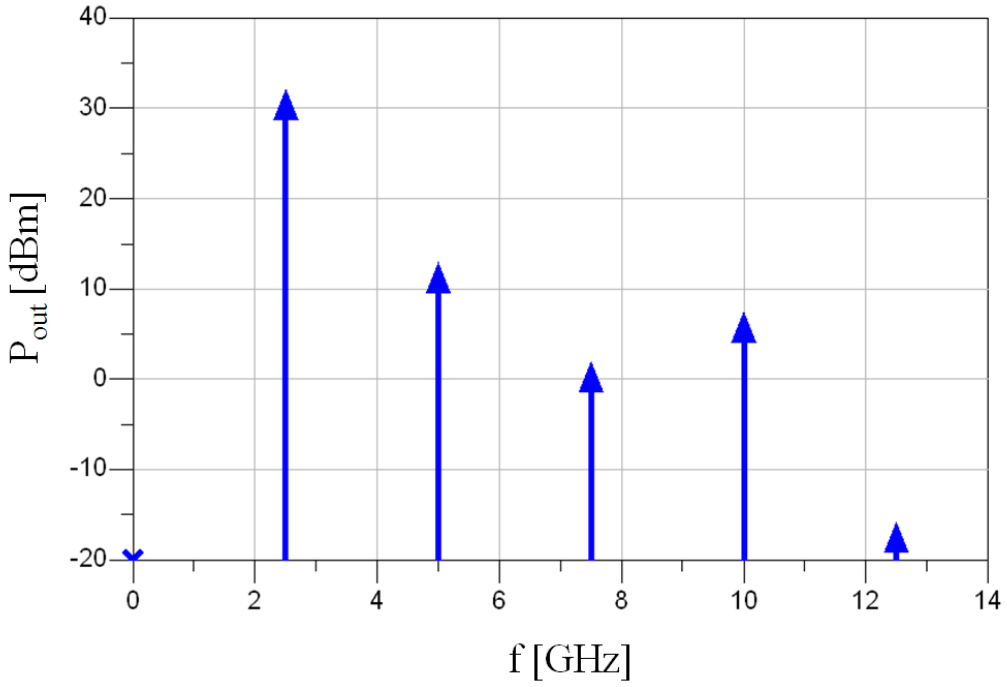


Figure 5.8: Class AB simulation of harmonic power at maximum PAE with modeled components, substrate, and interconnects.

The schematic level simulation of modeled passive components, interconnect traces, and substrate was used as a starting point to layout the circuit. Layout was accomplished using Agilent ADS Momentum, which also functions as an electromagnetic (EM) simulator. EM simulation is the last step before fabrication so it is essential to include as much detail about the final circuit as possible. The layout of this PA circuit is shown in Figure 5.9. The final EM simulation includes the parasitic effects of the via-connected grounded source pad, DC bypass capacitors, and a finite ground plane. The Momentum EM simulation was used to extract an S-parameter network in which all circuit components are attached to metal traces by individual ports. This results in a large S-parameter matrix (in this case 32 ports), which is used in circuit simulation with the passive component models described above.

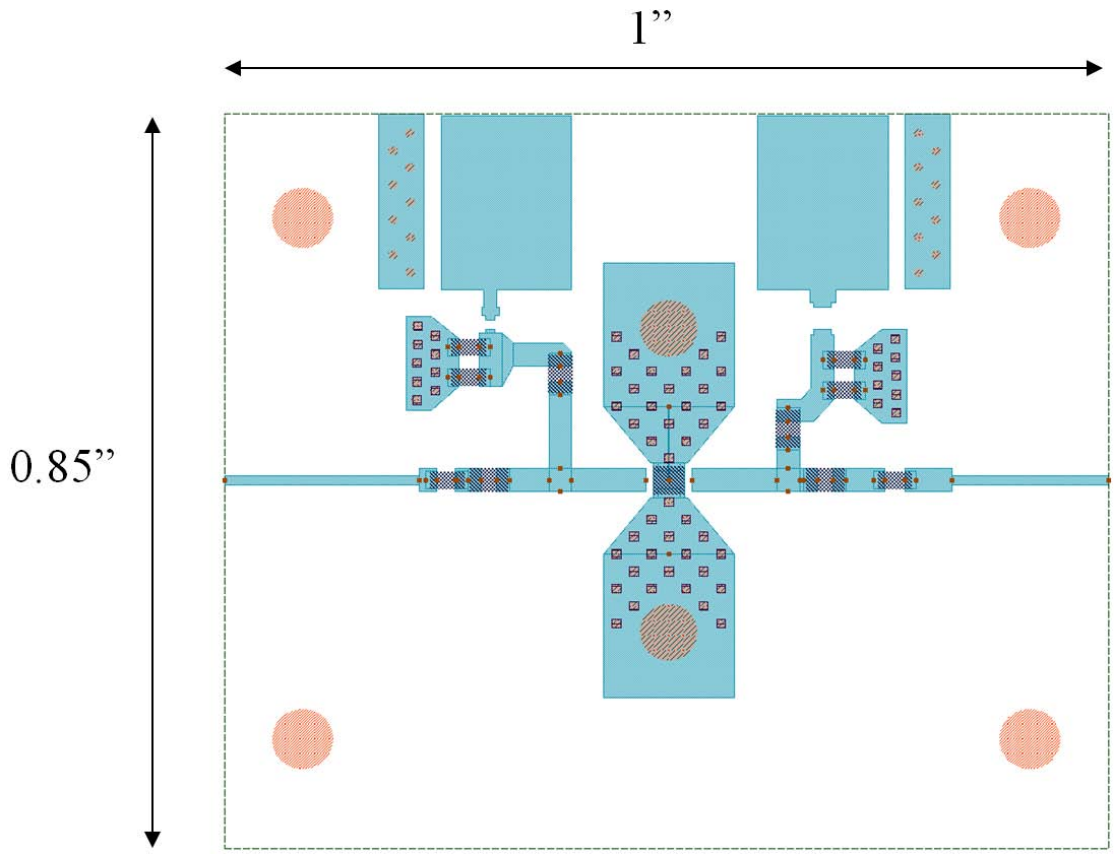


Figure 5.9: Class AB PA circuit layout.

A simulation of the PA circuit with the included layout EM simulation is shown in Figure 5.10 and the power spectrum at P_{1dB} is shown in Figure 5.11.

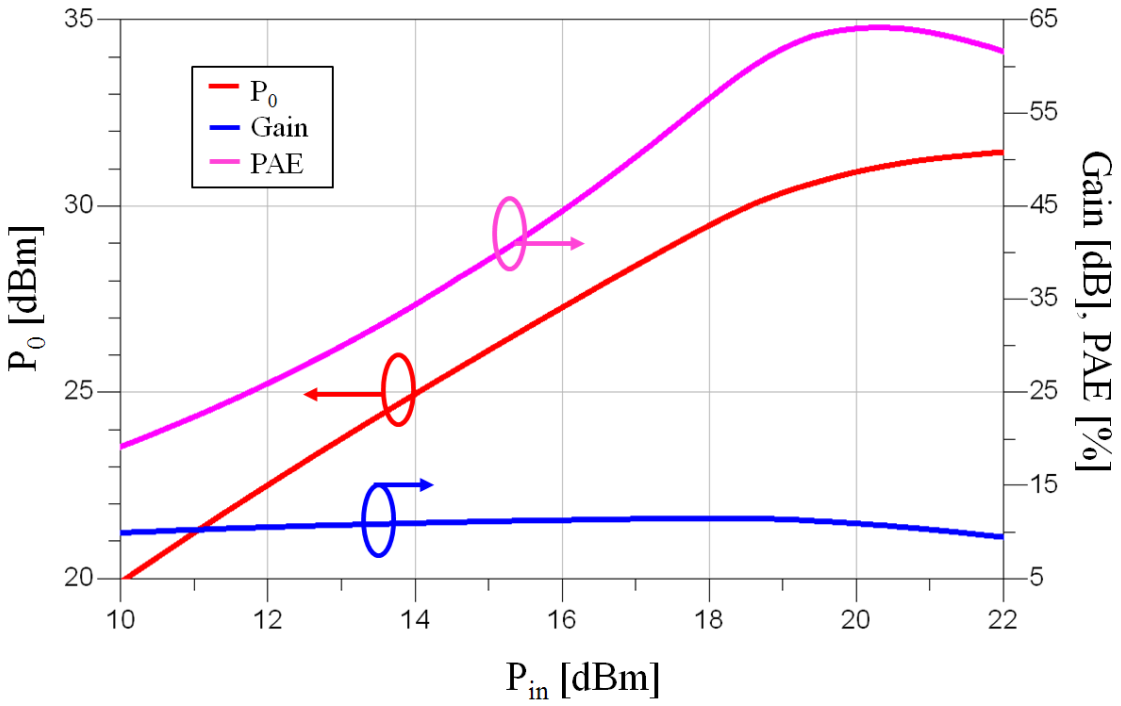


Figure 5.10: Simulated performance of Class AB PA including EM simulation.

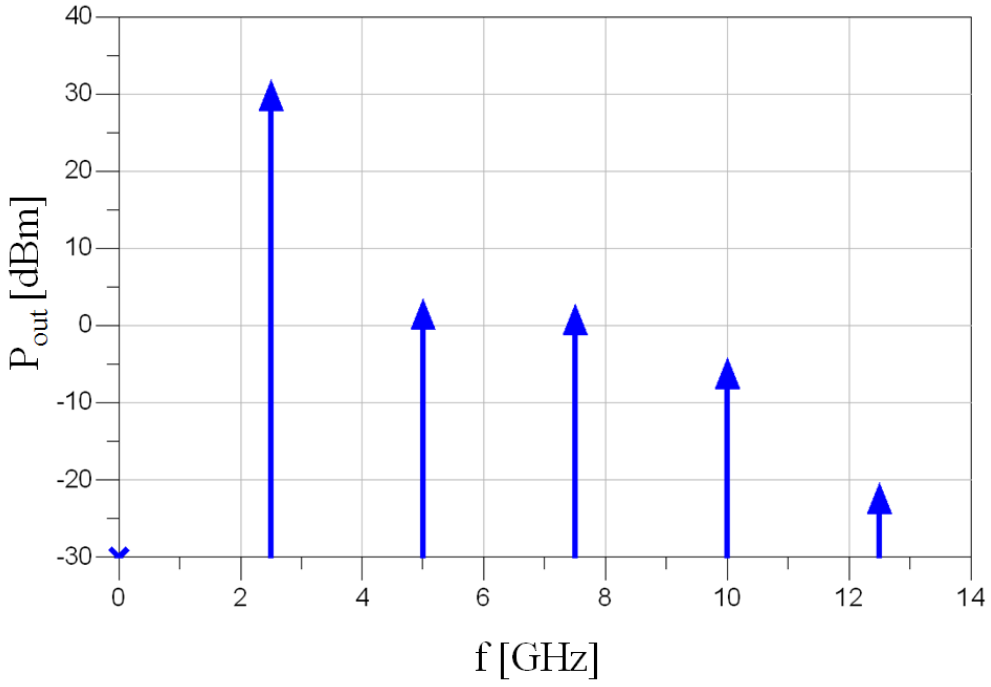


Figure 5.11: Class AB simulation of harmonic power at maximum PAE including EM simulation.

5.2.2. Fabrication Procedure

The PA was fabricated on TMM-13i substrate using 0402 surface-mount passive components and a Cree CGH60008D GaN HEMT connected by 1 mil diameter gold bond-wires. An assembly drawing and a bill-of-materials are shown in Figure 5.12 and Table IX respectively. A photograph of the fabricated PA is shown in Figure 5.13. The PA is mounted on a ¼" brass block for mechanical stability and heat sinking purposes.

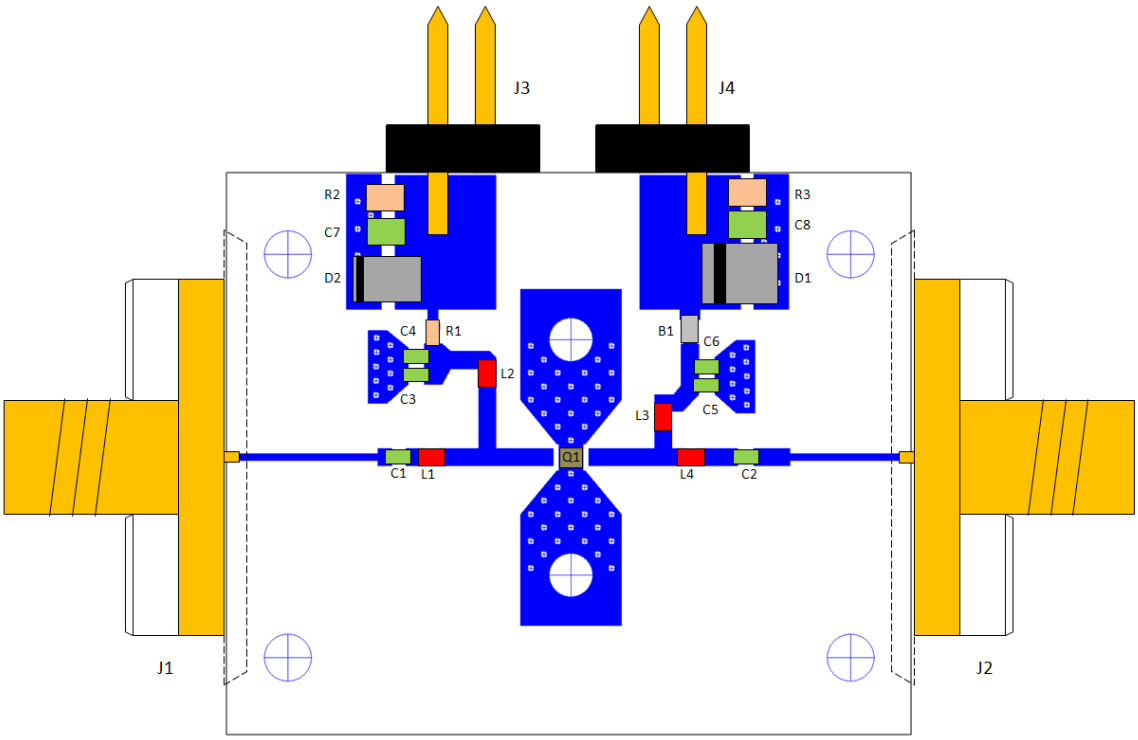


Figure 5.12: Assembly drawing of class AB PA.

Table IX: Bill-of-materials for class AB PA

Component Designator(s)	Component Type	Component Value	Manufacturer / Vendor	Part Number
B1	Ferrite Bead	33 Ohm	Murata	BLM18PG330SN1D
C1	Capacitor	0.8 pF	Murata	GRM1555C1H0R8
C2	Capacitor	6.8 pF	Murata	GRM1555C1H6R8
C3,C4,C5,C6	Capacitor	33.0 pF	Murata	GRM1555C1H33
C7, C8	Capacitor	0.01 uF	Panasonic	EJC-1VB1H103K
D1	Zener Diode	30 V	Micro Commercial Co.	SMBJ5363B-TPMSCTZ
D2	Zener Diode	10 V	Micro Commercial Co.	3SMAJ5925B-TPMSCT

J1, J2	SMA Jack	N/A	Midwest uWave	SMA-5530-15-TAB-02
J3, J4	2 Pin Header	N/A	Sullins	PZC36SAAN
L1	Inductor	2.4 nH	Coilcraft	0402HP-2N4XJLU
L2	Inductor	20 nH	Coilcraft	0402HP-20NXJLU
L3	Inductor	1 nH	Coilcraft	0402HP-1NXJLU
L4	Inductor	2 nH	Coilcraft	0402HP-2NXJLU
Q1	GaN HEMT	N/A	Cree	CGH60008D
R1	Resistor	33 Ohm	Panasonic	ERJ-2RKF33R0X
R2, R3	Resistor	1 kOhm	Panasonic	ERJ-2RKF1004X
S1, S2	Ground Contact	N/A	Spira Shield	MS-03-NC
	Brass Screw	0-80 x ¼" RH	McMaster-Carr	
	SS Screw	2-56 x ¼" PH	Midwest uWave	
	Brass Block	N/A	DL Shop	

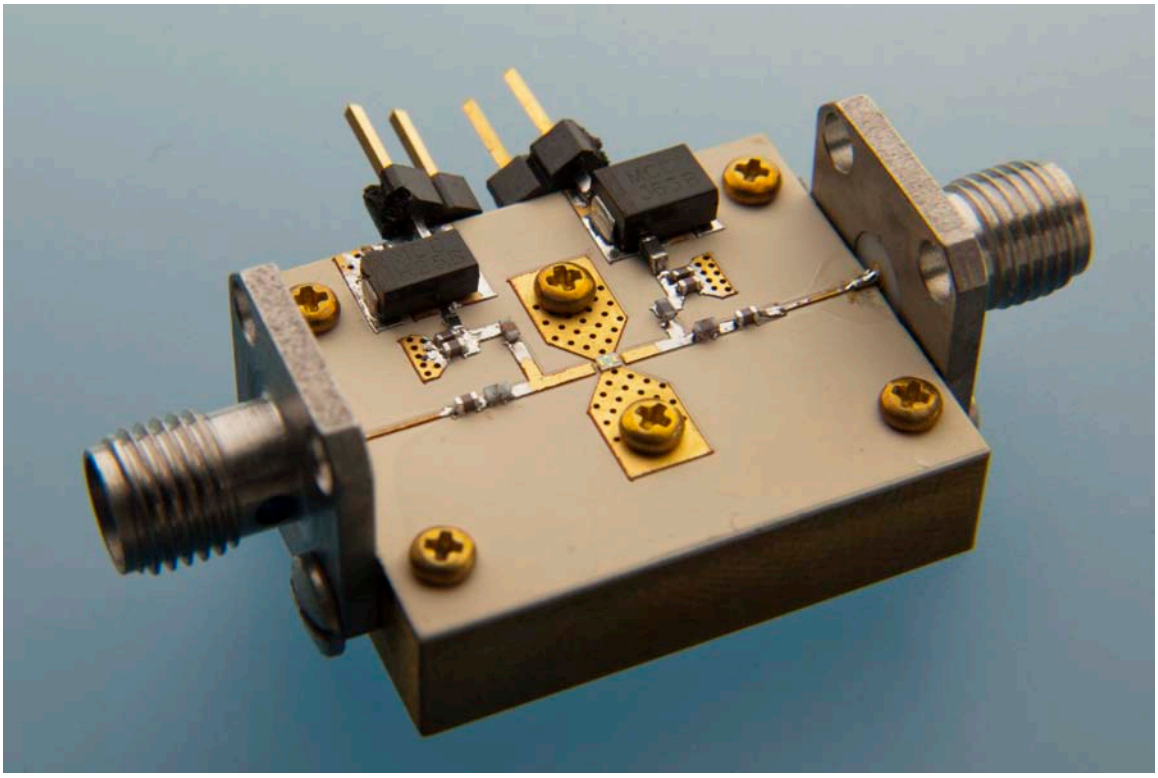


Figure 5.13: Photograph of the fabricated class AB PA

5.2.3. Test Setup & Procedure

The output power, gain, power spectrum, and PAE measurement test setup is shown in Figure 5.14. An RF signal generator, Agilent N5182A, with a 2.5 GHz continuous wave signal was fed into a Mini-Circuits ZQL-2700MLNW+ 25 dB

preamplifier stage. From there a power meter, Agilent E4417A, is coupled at 16 dB attenuation and calibrated to show the power level at the input of the PA. A spectrum analyzer, Agilent E4405B, was coupled at 16 dB attenuation to the output signal to observe the spectrum at the PA output. The output of the PA is fed into the Agilent power meter to measure the output power level. The gate and drain bias voltages, V_g, and V_d, are realized using a DC power supply, GW Instek PST-3202. The measured power, gain, and PAE performance of the PA is shown in Figure 5.15 and the power spectrum at P_{1dB} is shown in Figure 5.16.

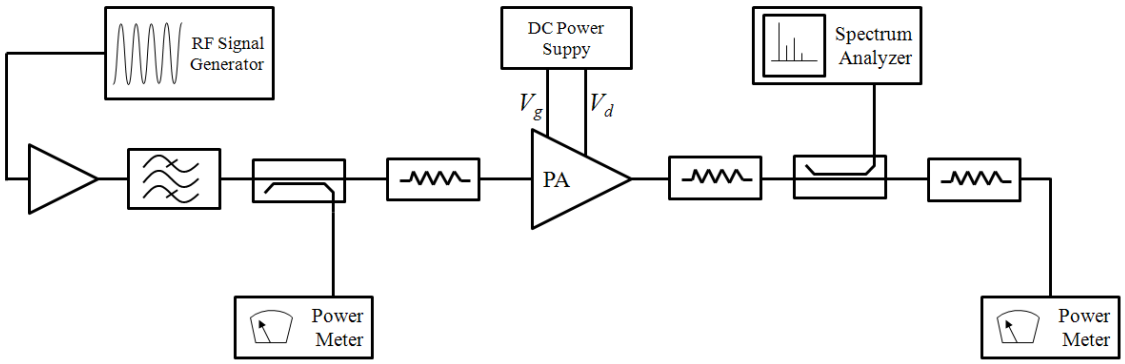


Figure 5.14: PA test setup for power, gain, PAE, and output spectrum.

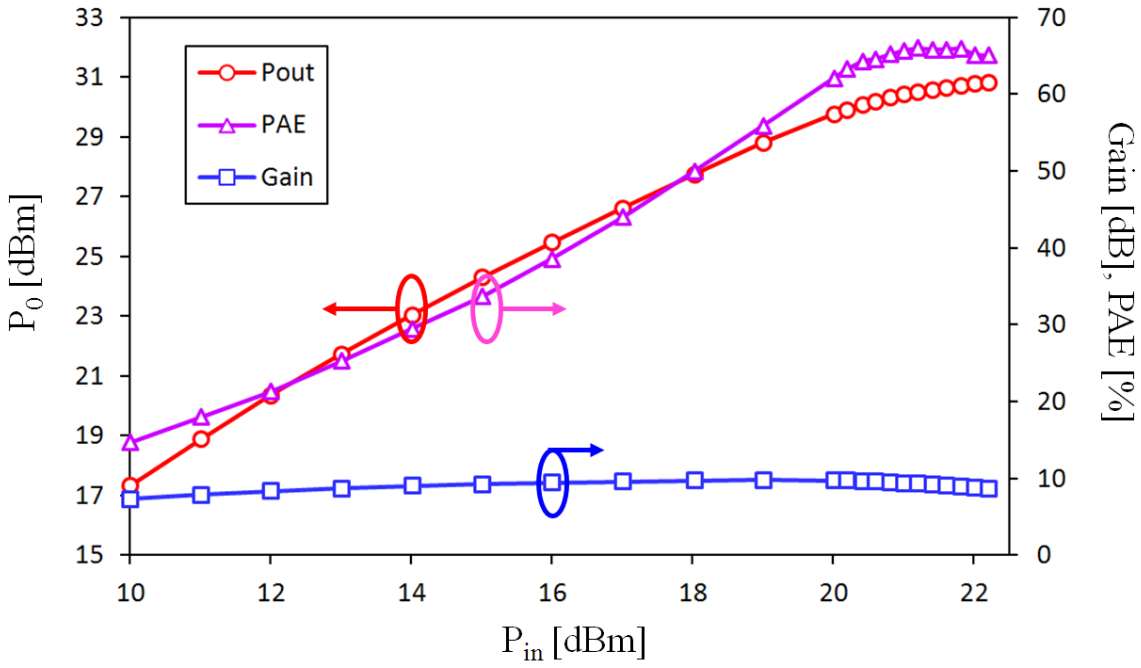


Figure 5.15: Measured performance of Class AB PA.

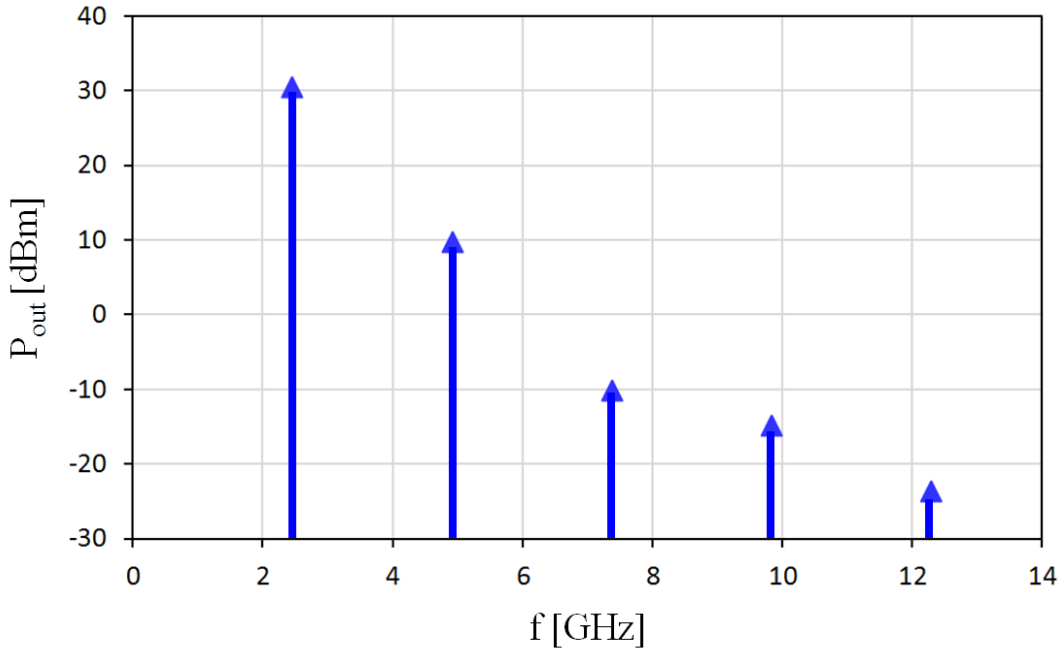


Figure 5.16: Measured harmonic power at maximum PAE of class AB PA.

5.2.4. Test Results

Some adjustment in frequency and gate bias was necessary to achieve proper performance from the fabricated PA. Peak performance was measured at a frequency of 2.45825 GHz versus the simulated frequency of 2.5 GHz, with a gate bias voltage of -3.0 V versus the simulated -2.9 V.

The output power, gain, and PAE measurements are shown plotted against simulated values in Figure 5.17 and Figure 5.18. The harmonic power at P_{1dB} measured versus simulated is shown in Figure 5.19. These results will be discussed in greater detail in the following chapter.

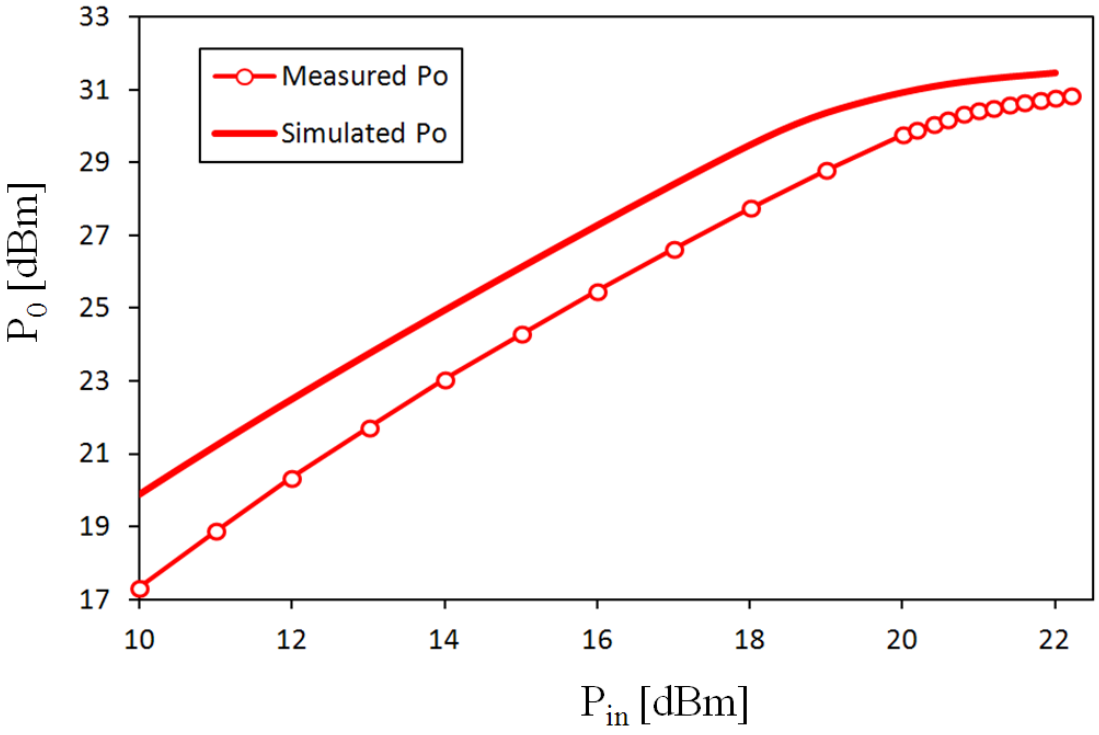


Figure 5.17: Class AB PA fundamental output power measured vs. simulated.

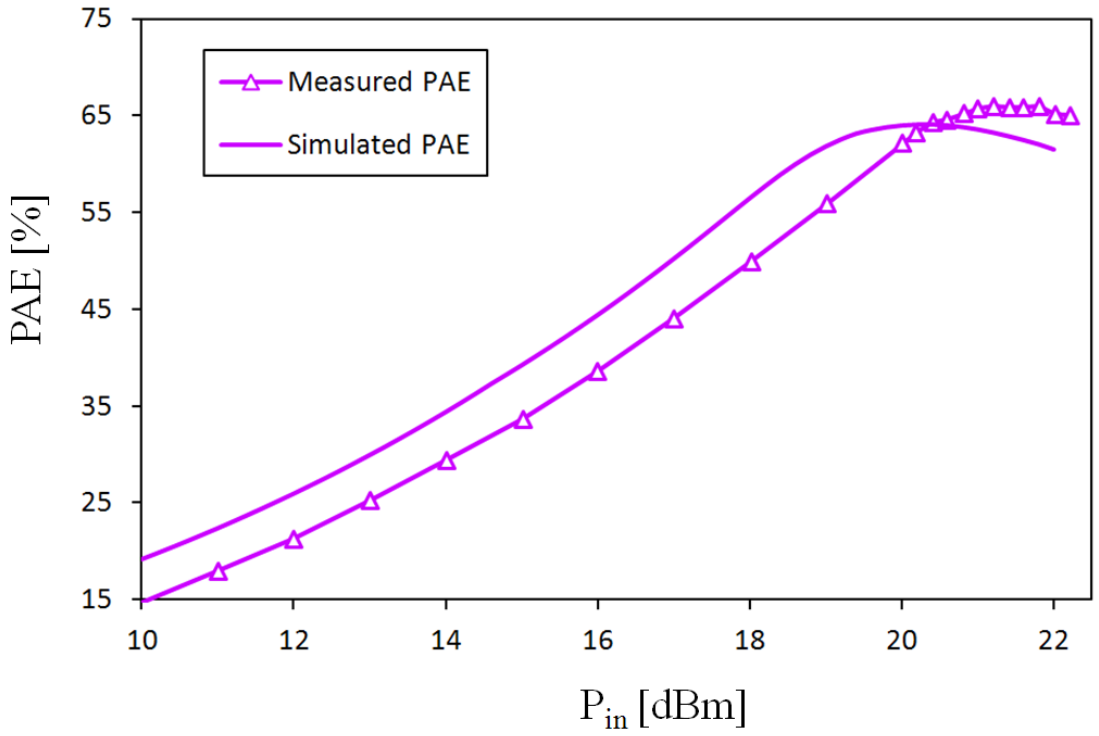


Figure 5.18: Class AB PA PAE measured vs. simulated

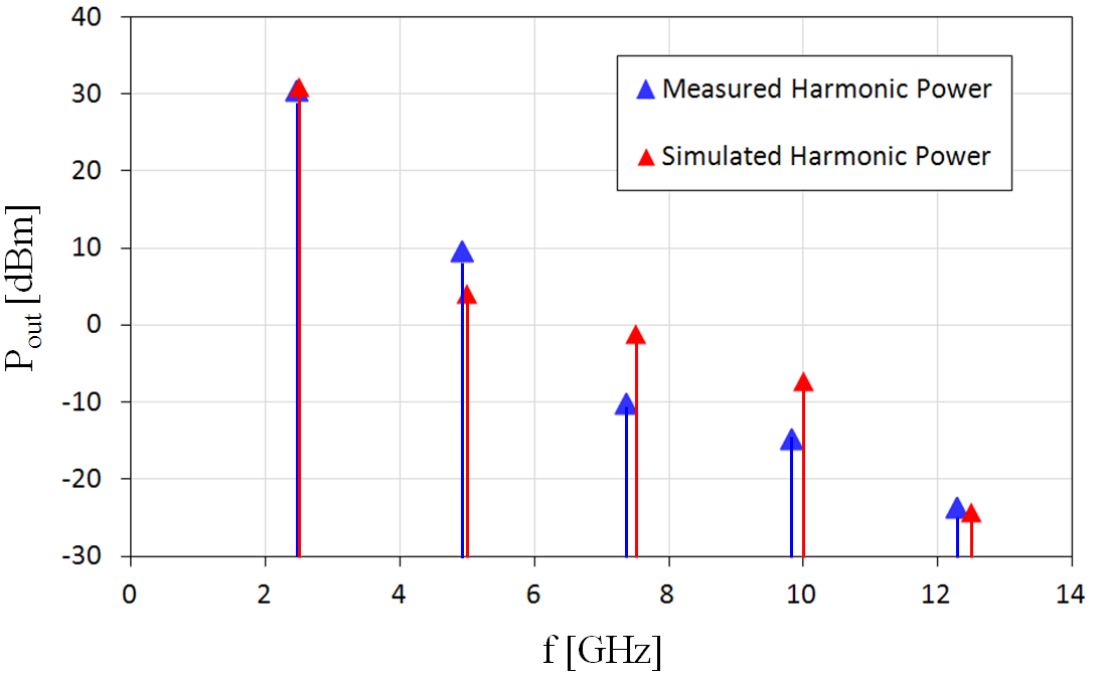


Figure 5.19: Class AB PA harmonic output power measured vs. simulated.

5.3. Switching PA

Design of a switching PA involved a similar procedure to the linear PA described above. A bias point was chosen and a load/source-pull simulation was performed, but unlike the linear PA design, a *harmonic* load/source-pull was performed thus shaping the output and input waveforms to achieve class E performance. From the harmonic load/source-pull data, harmonic matching networks were designed and beyond this point the same procedure as above was performed.

5.3.1. Design Procedure

A harmonic load/source-pull simulation was performed using the large-signal model of the Cree GaN HEMT CGH60008D describe in chapter 4 in ADS. The load/source-pull procedure was performed up to the fourth harmonic under a variety of gate bias voltages in the range near -3.5 V and for various input power levels to converge on harmonic load and input impedances that produce the desired performance.

A gate bias voltage of -3.3 V with an input power of 18 dBm resulted in 31.9 dBm output power, 13.9 dB of gain, and 81% PAE. These simulation results will be repeated at the end of this section in order to compare simulated results to measurements of the fabricated PA circuit. The harmonic impedance values determined by the load/source-pull procedure are shown in Table X.

Table X: Class E harmonic impedances determined by load/source-pull simulation.

Harmonic Impedance	Z_0	Z_2	Z_3	Z_4
Load-pull (Ω)	10.1+*j*40.2	-*j*45.8	*j*71.4	-*j*571.5
Source-pull (Ω)	10+*j*0.9	*j*2.2	*j*107.2	*j*71.4

From the impedances determined by the load/source-pull procedure, harmonic output and input networks were designed. These networks were designed by first matching the fundamental impedance then adjusting the matching element values to achieve impedance matches at the fundamental and first harmonic simultaneously. This process was repeated up to the fourth harmonic impedance.

When designing a harmonic matching network the load/source-pull results are leveraged to determine the accuracy required in matching impedances at specific harmonic frequencies. The PA circuit simulation can be set to sweep a specific harmonic impedance value and observe the effect on the PA performance. By iterating this process the designed matching networks are the result of the trade-off between the ideal harmonic impedance values giving maximum PA performance and the impedances that are achievable in a realistic impedance matching circuit.

The designed input and output matching networks are shown in the schematic in Figure 5.20 and the simulated performance resulted in 32.0 dBm output power, 14.0 dB of gain, and 81.5 % PAE.

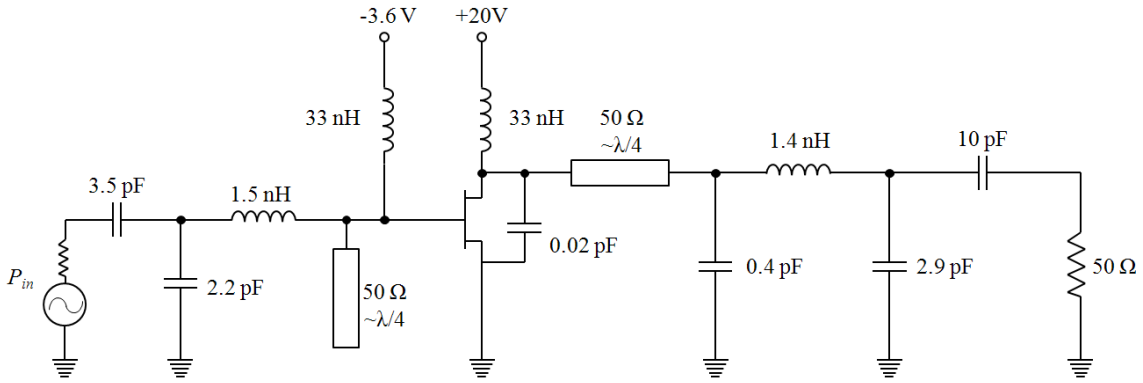


Figure 5.20: Class E PA circuit schematic using ideal passive element models.

Figure 5.21 shows the harmonic load-pull impedances (indicated by hexagons) and S_{11} of the output matching network (line with triangle markers indicating harmonics to be matched). Figure 5.22 shows the input matching network versus the harmonic source-pull impedances. The results of the trade-offs described above are seen in differences between load/source-pull impedance values and harmonic impedances realized by the matching networks of Figure 5.20 as shown in Figure 5.21 and Figure 5.22.

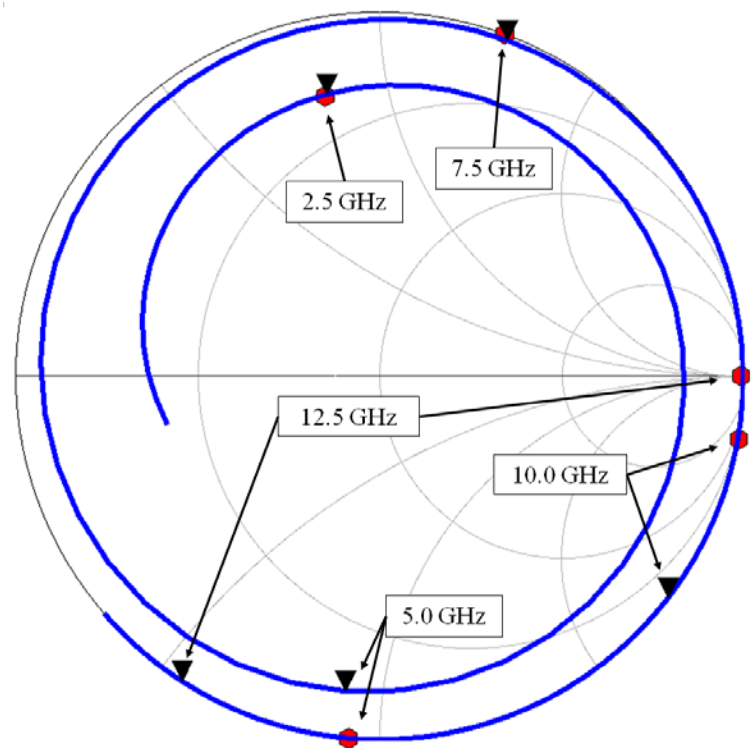


Figure 5.21: S_{11} of harmonic output matching network vs. load-pull impedances.

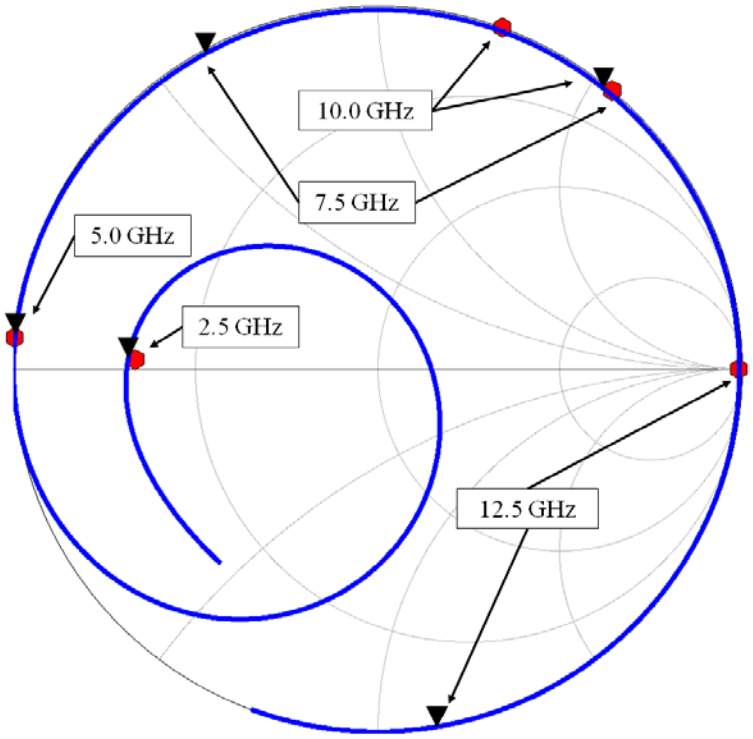


Figure 5.22: S11 of harmonic input matching network vs. source-pull impedances.

The ideal input and output matching networks were redesigned using passive component models as described above in section 5.2. There was an iterative process of observing PA performance as a function of each impedance to determine the trade-off between the desired impedances and the impedance realizable using discrete component values and modeled parasitics.

The matching networks with modeled passive components and substrate are shown in Figure 5.23 and the simulated performance resulted in 33.12 dBm output power, 15.12 dB of gain, and 72.0 % PAE. The PAE was reduced significantly from the PA circuit with ideal passive elements because of the discrete values available to match impedances as well as parasitic losses in modeled components and substrate.

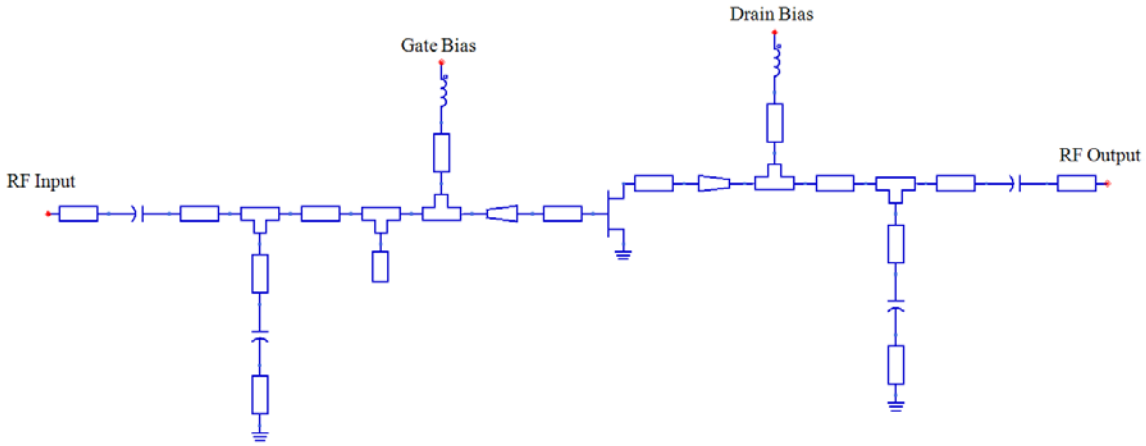


Figure 5.23: Class E PA circuit schematic using modeled passive elements and substrate.

The circuit was laid out and an EM simulation was performed to verify performance of the circuit topology and component values and gate bias were adjusted to achieve maximum performance. The layout of the PA is shown in Figure 5.24 and the simulated performance resulted in 33.3 dBm output power, 15.8 dB of gain, and 70.0 % PAE.

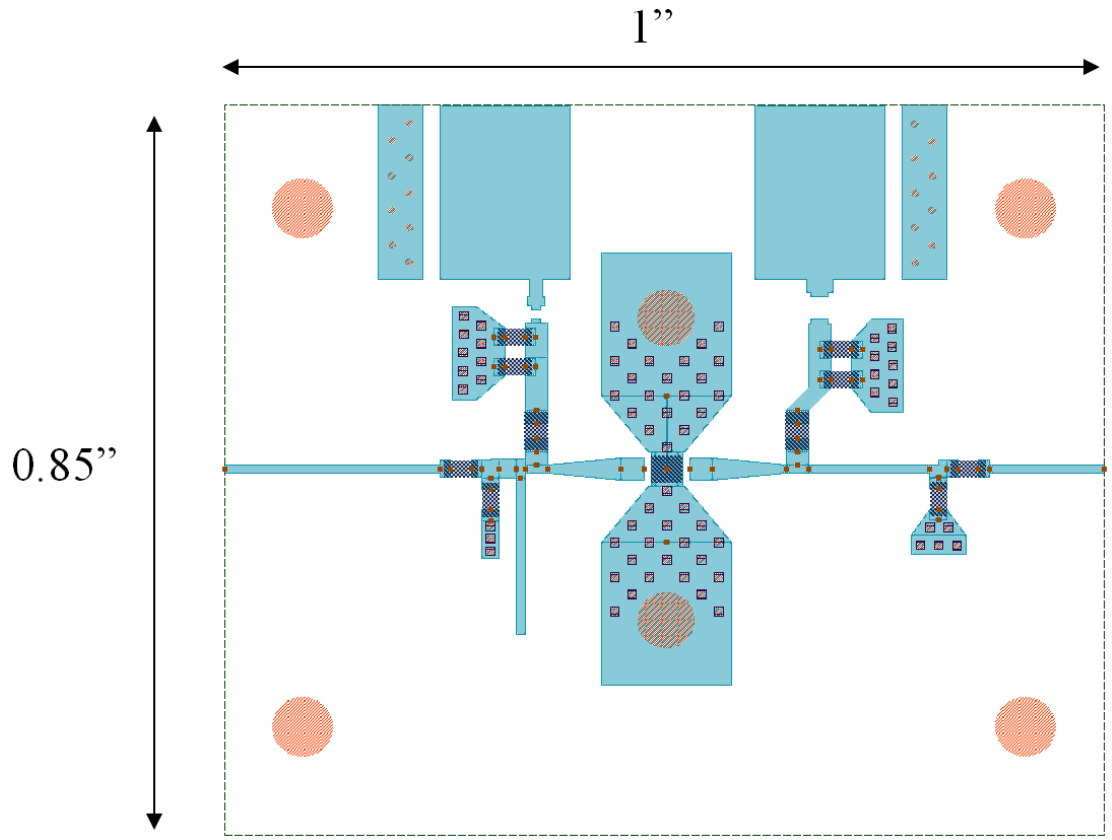


Figure 5.24: Class E PA circuit layout.

5.3.2. Fabrication Procedure

The class E PA was also fabricated on TMM-13i substrate using 0402 surface-mount passive components and a Cree CGH60008D GaN HEMT connected by 1 mil diameter gold bond-wires. An assembly drawing and a bill-of-materials are shown in Figure 5.25 and Table XI respectively. A photograph of the fabricated PA is shown in Figure 5.26. Similar to the class AB PA above, the class E PA is mounted on a ¼” brass block for mechanical stability and heat sinking.

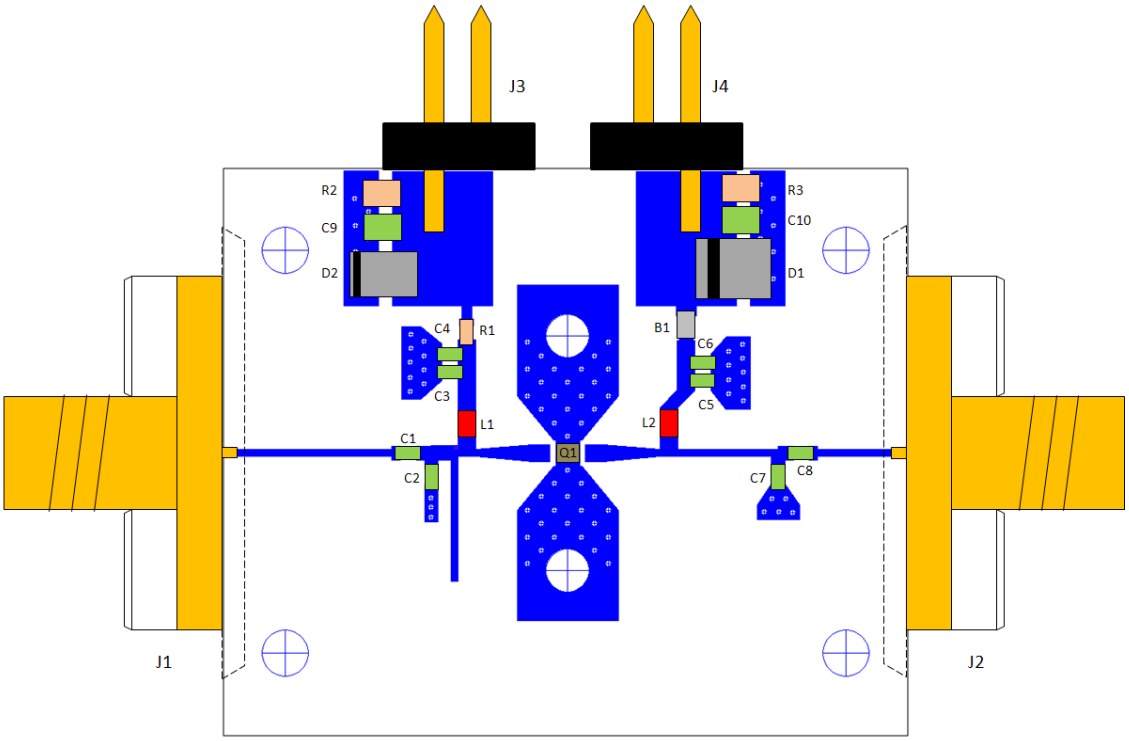


Figure 5.25: Assembly drawing of class E PA.

Table XI: Bill-of-materials for class E PA.

Component Designator(s)	Component Type	Component Value	Manufacturer / Vendor	Part Number
B1	Ferrite Bead	33 Ohm	Murata	BLM18PG330SN1D
C1	Capacitor	0.8 pF	Murata	GRM1555C1H0R8
C2	Capacitor	1.5 pF	Murata	GRM1555C1H1R5
C3,C4,C5,C6	Capacitor	33.0 pF	Murata	GRM1555C1H33
C7	Capacitor	1.5 pF	Murata	GRM1555C1H1R5
C8	Capacitor	10 pF	Murata	GRM1555C10H0R9
C9, C10	Capacitor	0.01 uF	Panasonic	EJC-1VB1H103K
D1	Zener Diode	30 V	Micro Commercial Co.	SMBJ5363B-TPMSCTZ
D2	Zener Diode	10 V	Micro Commercial Co.	3SMAJ5925B-TPMSCT
J1, J2	SMA Jack	N/A	Midwest uWave	SMA-5530-15-TAB-02
J3, J4	2 Pin Header	N/A	Sullins	PZC36SAAN
L1	Inductor	33 nH	Coilcraft	0402HP-33NXJLU
L2	Inductor	10 nH	Coilcraft	0402HP-10NXJLU
Q1	GaN HEMT	N/A	Cree	CGH60008D
R1	Resistor	33 Ohm	Panasonic	ERJ-2RKF33R0X
R2, R3	Resistor	1 kOhm	Panasonic	ERJ-2RKF1004X
S1, S2	Ground Contact	N/A	Spira Shield	MS-03-NC
	Brass Screw	0-80 x ¼” RH	McMaster-Carr	
	SS Screw	2-56 x ¼” PH	Midwest uWave	
	Brass Block	N/A	DL Shop	

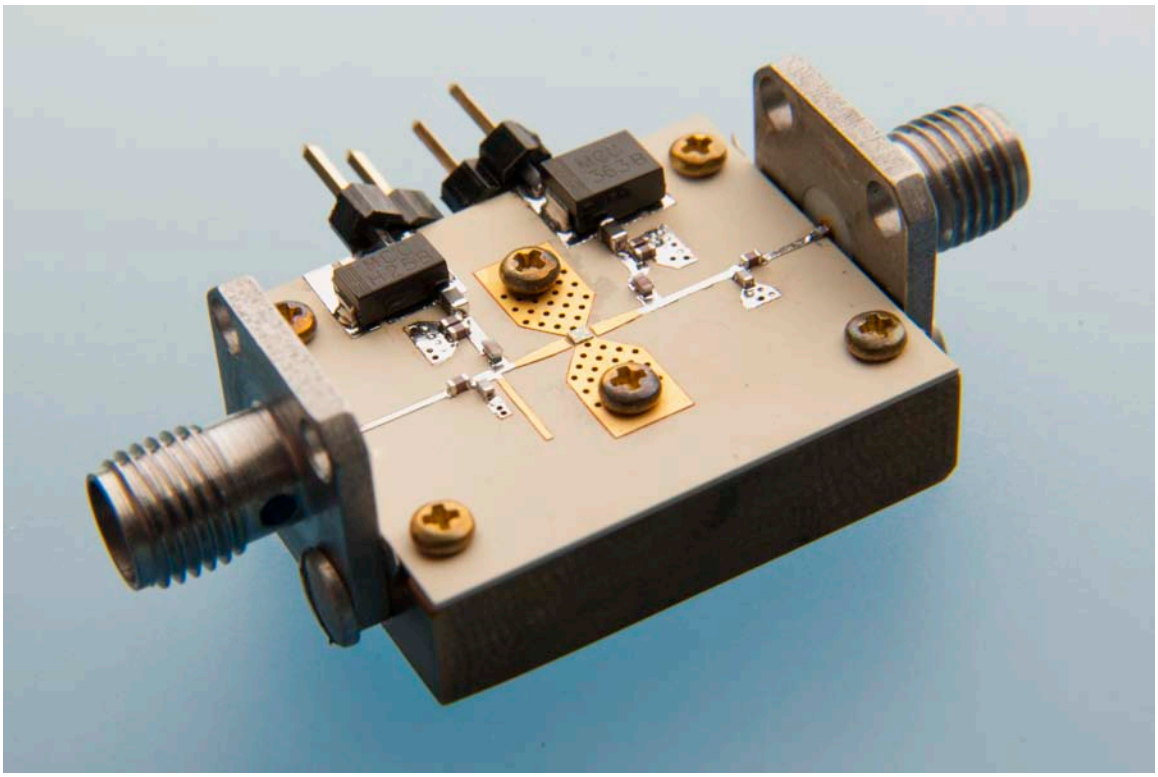


Figure 5.26: Photograph of the fabricated class E PA.

5.3.3. Test Results

Some adjustment in frequency and drain bias was necessary to achieve optimal performance from the fabricated PA. Peak performance was measured at a frequency of 2.62 GHz versus the simulated frequency of 2.5 GHz. Peak PAE was measured at a drain bias voltage of 12 V versus the simulated 20 V and peak output power was measured at the simulated bias voltage of 20 V.

The output power, PAE, and gain measurements are shown, along with simulated values, in Table XII. These results will be discussed in greater detail in the following chapter.

Table XII: Comparison of class E PA performance from simulation to measured results.

	P_0 (dBm)	Gain (dB)	PAE (%)
Ideal impedances	31.9	13.9	81.0
Ideal matching networks	32.0	14.0	81.5
Modeled passives	33.1	15.1	72.0
EM simulation	33.3	15.8	70.0
Measured (best PAE)	30.1	10.6	64.4
Measured (best P_0)	33.2	13.0	52.7

Chapter 6. Conclusion

6.1. Discussion of Results

6.1.1. PA Measurements vs Simulations

Results from the class AB and class E PAs that were designed and fabricated based on the model described in this thesis were shown in the previous chapter and are repeated here in Figure 6.1, Figure 6.2, and Figure 6.3 for the class AB PA and in Table XIII for the class E PA.

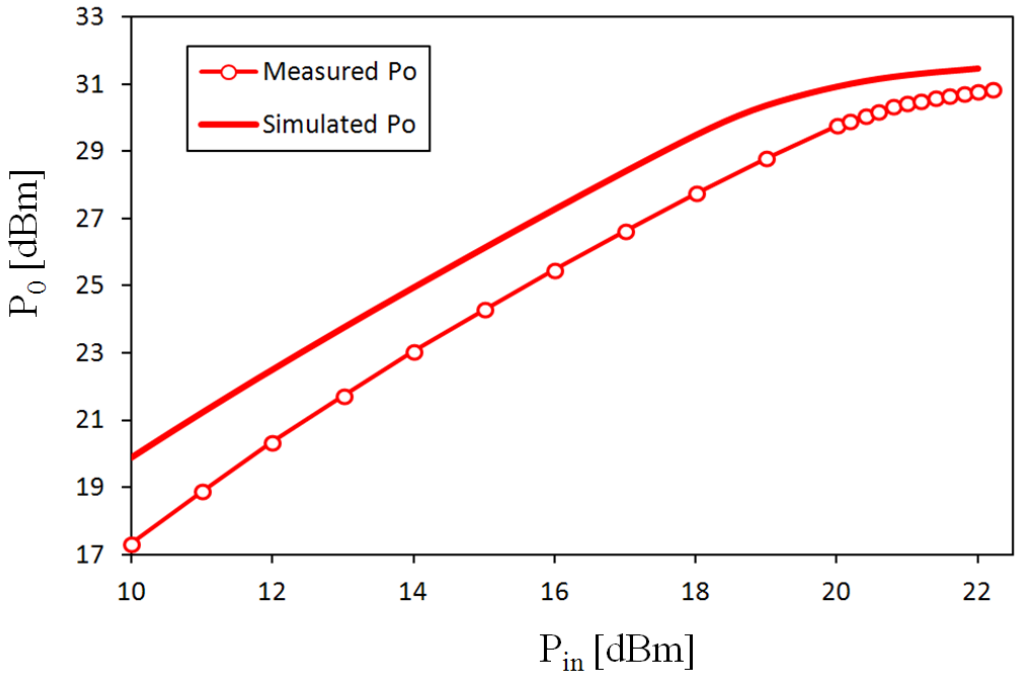


Figure 6.1: Class AB PA Pout measured vs. simulated.

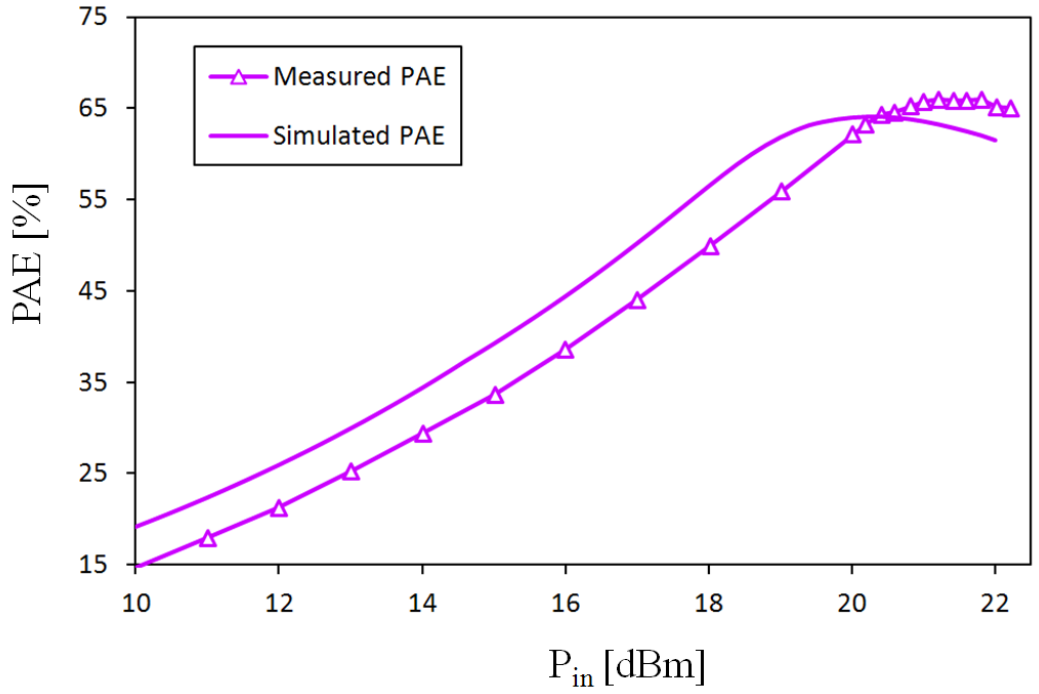


Figure 6.2: Class AB PA PAE measured vs. simulated

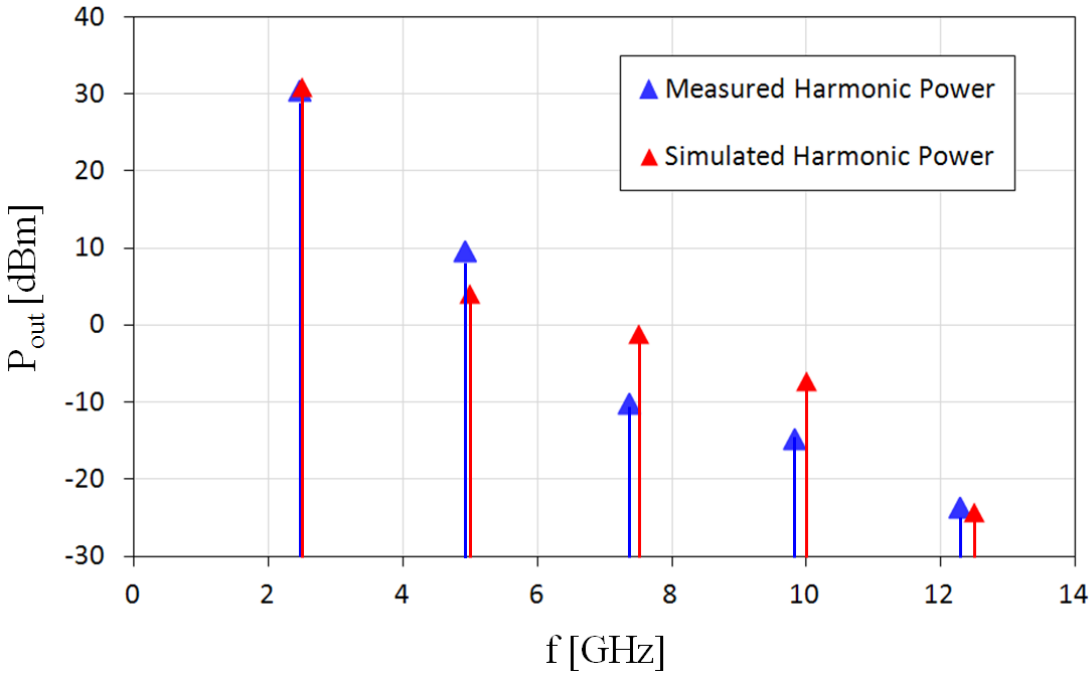


Figure 6.3: Class AB PA harmonic output power measured vs. simulated.

Table XIII: Comparison of class E PA performance from simulation to measured results.

	P_0 (dBm)	Gain (dB)	PAE (%)
Simulation (original)	33.3	15.8	70.0
Measured (best P_0)	33.2	13.0	52.7
Measured (best PAE)	30.1	10.6	64.4
Simulation (best PAE)	28.9	9.4	62.7

Table XIV and Figure 6.4 show a measure of the accuracy of the model by comparing simulated values to measured values in terms of percent error of the simulated values using the formula [43]

$$\%\ error = \left|\frac{simulated - measured}{measured}\right| \times 100\% \ . \tag{6.1}$$

For the class E PA, the best agreement between simulation and measurement, in terms of output power, was measured at the simulated bias point and is referred to as "best P_0." The best agreement in terms of PAE was measured at a bias condition, V_{ds} = 12 V versus the original 20 V, referred to as "best PAE." Percent error is shown comparing best PAE to both the original simulation and a simulation performed at the V_{ds} = 12 V bias point.

Table XIV: Percent error of simulated values vs. measured values of class AB and class E PA circuits.

Amplifier	Frequency	V_{gs}	V_{ds}	P_0	PAE	Gain
Class AB	1.70 %	3.33 %	0.00 %	1.07 %	1.54 %	21.0 %
Class E (best P_0)	4.58 %	0.00 %	0.00 %	0.30 %	32.8 %	21.5 %
Class E (best PAE vs. original sim.)	4.58 %	0.00 %	66.7 %	10.6 %	8.70 %	49.1%
Class E (best PAE vs. best PAE sim.)	4.58 %	0.00 %	0.00 %	4.00 %	2.64 %	11.3 %

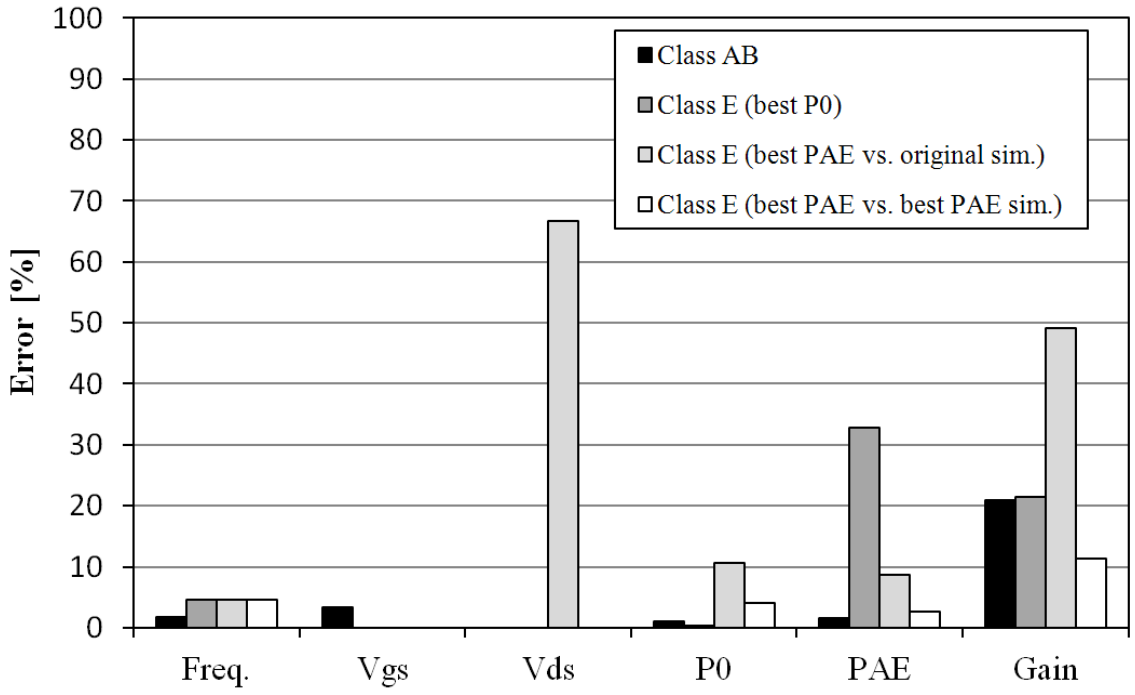


Figure 6.4: Percent error of simulated values vs. measured values of class AB and class E PA circuits.

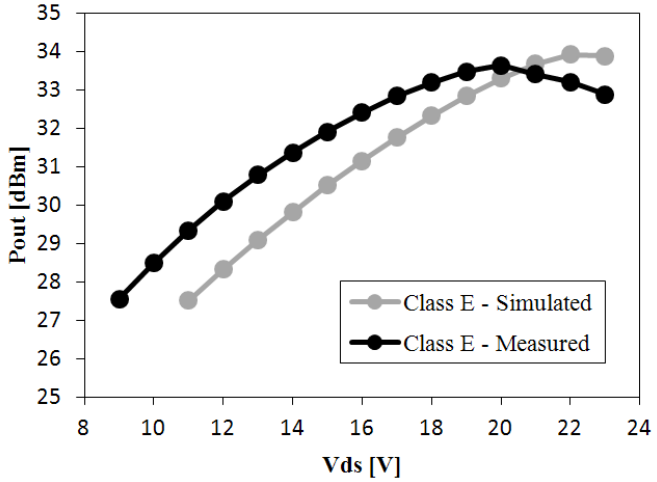
For the class AB PA, the frequency and V_{gs} values reflect the tuning that was necessary to get closest agreement between measurement and simulation. The values of P_0, PAE, and gain were compared at the output power that produced maximum PAE measured.

The most significant difference seen in the class AB PA is gain. It should be noted, however, that the difference of 20-25% gain in previous PA designs when using a commercial large-signal model such as the model provided by Cree Inc. In comparison to that, the 21.0% error reported here is within the expected design limits. A similar observation may also be made about the gate bias voltage. Threshold voltage of HEMT devices is typically variable from one device to another and adjusting the gate bias in a PA circuit is common practice [26].

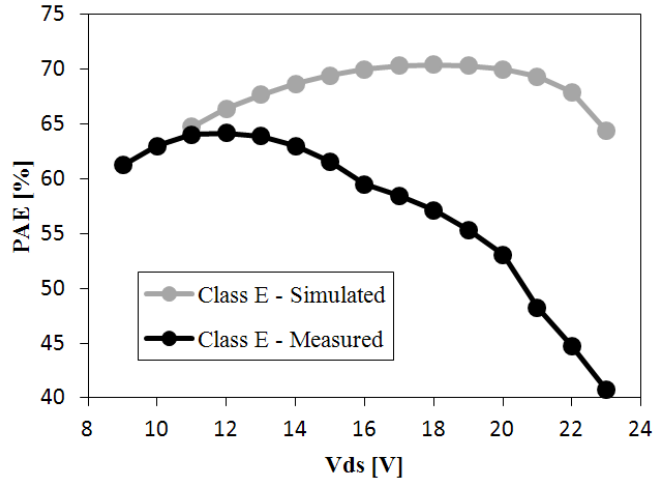
Obtaining meaningful results for the class E PA was difficult due to instability issues. In hindsight, the model does show instability during stability analysis simulations; however, these instabilities are not expressed in typical harmonic balance large-signal simulations and thus went unnoticed during the design procedure.

Comparison is further complicated by the knowledge that the gate threshold voltage is variable from one device to another and PA gain may be in error by 20-25% between simulation and measurements as described above. Figure 6.5 shows a comparison of peak measured (a) power, (b) PAE, and (d) drain efficiency performance of the class E PA to simulations performed for a variety of drain bias voltages. This is shown because the fabricated PA displayed maximum PAE at a drain supply voltage of 12 V versus the design point of 20 V and the trend holds true for the output power as well. Similar plots are shown for the class AB PA in Figure 6.6. By comparing the figures of class E and class AB measurements and simulations it is possible that the class E performance discrepancy is resulting from a number of possible sources. The issue is complicated by the inability to measure the impedances presented to the HEMT in the fabricated circuit in order to compare those values to the simulated impedances.

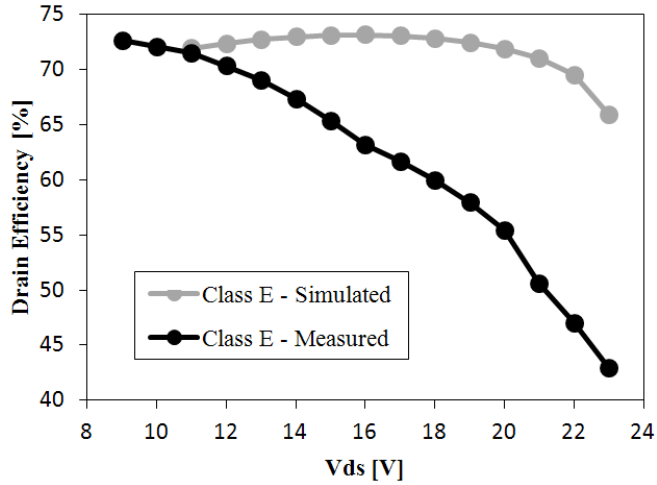
Some possibilities of the discrepancy include inaccuracies in the nonlinear capacitance modeling and inaccuracies in the input and/or output matching networks in the fabricated circuit. Inaccurate capacitance modeling would affect the upper harmonic behavior of the PA and impact the optimal waveform shaping thus preventing high efficiency operation. The same can be said about inaccuracies in the matching networks; the sensitivity of impedance will increase with frequency, thus making the upper harmonics more sensitive.



(a)

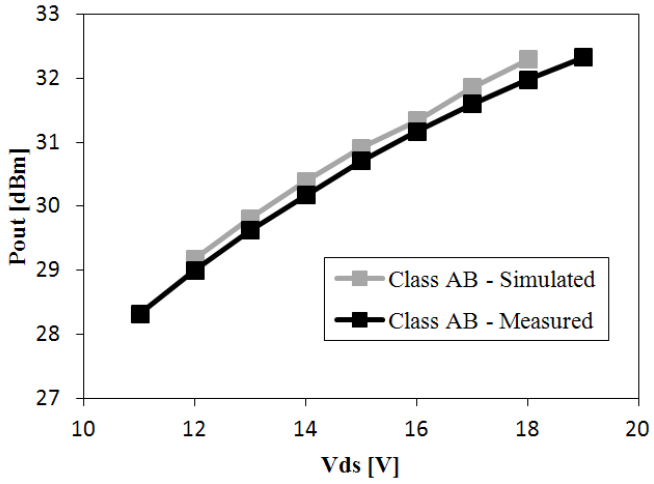


(b)

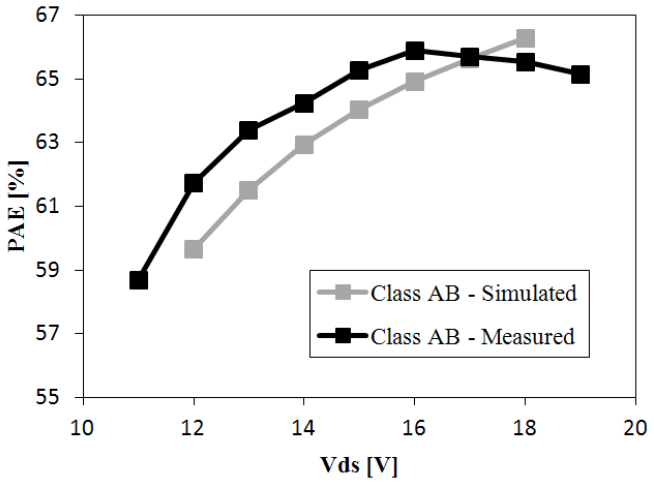


(c)

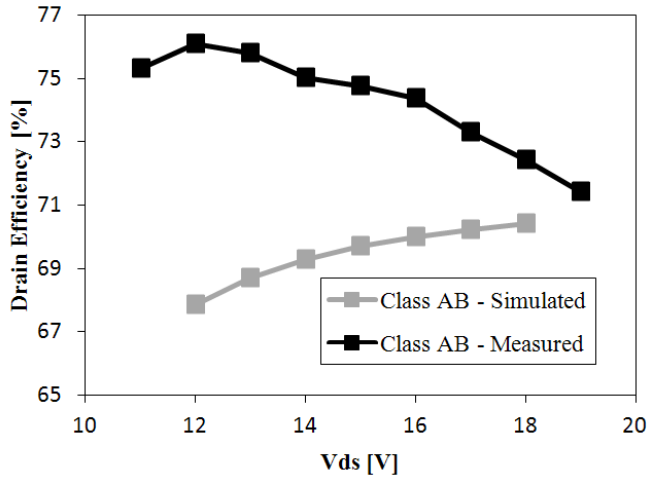
Figure 6.5: Class E performance (measured and simulated) vs. supply voltage ,V_ds.



(a)



(b)



(c)

Figure 6.6: Class AB performance (measured and simulated) vs. supply voltage ,Vds.

6.1.2. Comparison of modeled HEMTs

From the values in Table XV, the small-signal parameter values confirm the relative size difference between the MIT and Cree devices. The Cree HEMT being four times larger is observed in the parasitic resistances which are roughly four times smaller due to increased surface area of the gate, drain, and source electrodes. The increased area also causes the capacitance to be roughly four times larger. Inductances should be roughly the same because the gate, drain and source pads are comparably sized.

Table XV: Typical modeled small-signal parameter values.

Device Type	MIT – T (500 μm)	MIT – U (500 μm)	Cree (2 mm)
R_g **(Ω)**	10	16	1
R_d **(Ω)**	3	4	1
R_s **(Ω)**	2	2	0.25
R_i **(Ω)**	1	2	3
L_g **(pH)**	44	10	21
L_d **(pH)**	51	49	33
L_s **(pH)**	0	0	11
C_{gp} **(fF)**	6	6	41
C_{dp} **(fF)**	6	6	42
C_{gsi} **(fF)**	0	0	571
C_{dsi} **(fF)**	18	18	125
C_{gs} **(fF)**	1360	1000	4264
C_{ds} **(fF)**	70	74	589
C_{gd} **(fF)**	32	27	861

Evidence of the large device size is seen in the IV curves as well. Currents in the Cree HEMT are roughly four times larger than in the MIT devices because the Cree

devices are four times larger. This is shown in Figure 6.7 where IV curves for a typical 500 μm MIT U-gate device are overlaid with a typical 2 mm Cree device.

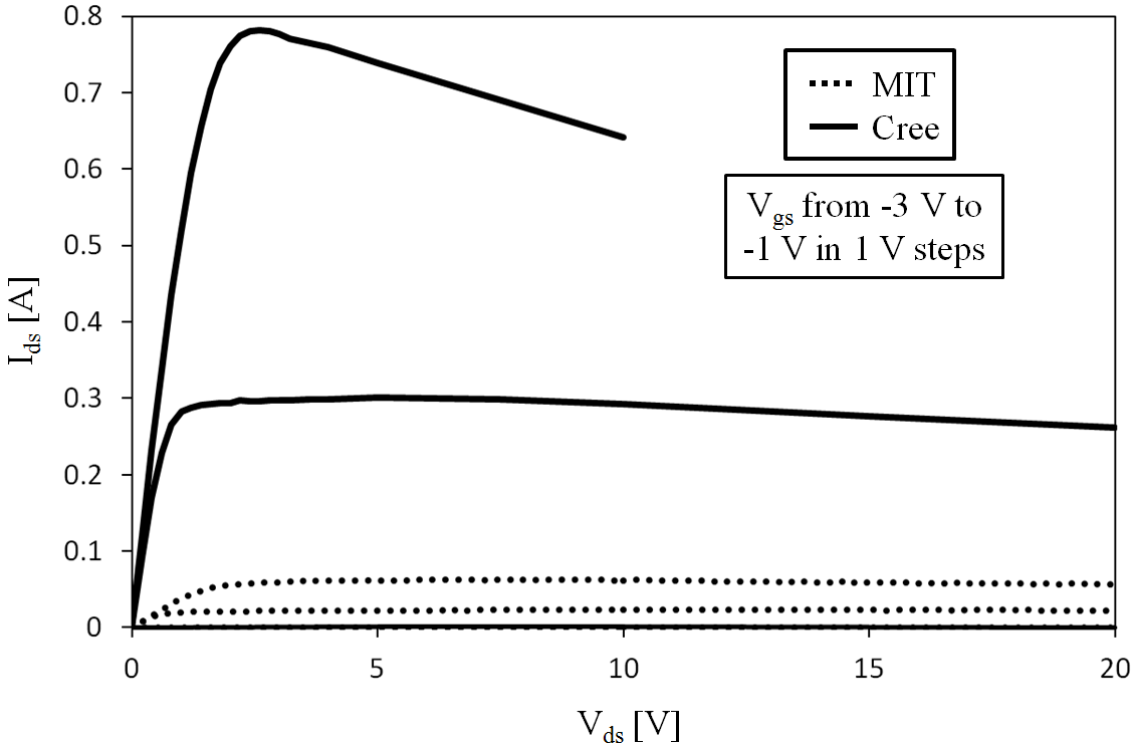


Figure 6.7: Comparison of IV curve measurements of MIT and Cree GaN HEMTs.

6.1.3. Relating to Other Work

By demonstrating the validity of the large-signal model in class AB and class E operation, the model is demonstrating a capacity to describe the essential behaviors of all single stage PA classes as described in chapter 2.2 and thus in the architectures described in chapter 2.3. This makes the described model useful in the evaluation of the modeled device in a broad array of PA circuits and systems.

The data in Table XVI (repeated from Table III in chapter 2) includes the PAs of this work, described in chapter 5, as well as other GaAs and GaN HEMT PAs described

in recent literature. The measured results from the class AB PA are shown and both the simulated and measured values are shown for the class E PA to illustrate the discrepancy between the modeled and measured performance of the PA with respect of other reported PAs. Figure 6.8 shows a P_{out} versus PAE plot using the values from Table XVI.

Table XVI: Summary of recent GaAs and GaN HEMT PA work.

Reference	Technology	Class	Drain Supply [V]	Pout [dBm]	PAE [%]	f [GHz]	Gain [dB]	Year
[13]	GaAs	A	4	23.5	40	25	11	2012
[14]	GaAs	A	8	34	37.1	3.5	28	2008
[15]	GaAs	A	9	24	29	2.4	40	2007
[16]	GaAs	A	8	38.1	24	14	10.5	2007
[17]	GaAs	AB	5	33	35	5.8	14	2006
[18]	GaN	B	20	36	34	8	9	2003
[19]	GaN	D	10	39	65	2.35	10	2009
[20]	GaN	E/F	30	40	73.1	2.14	14.3	2011
[21]	GaN	F	28	36	66	2.7	13.8	2011
[22]	GaN	F	25	33.4	71.4	5.8	10	2010
[23]	GaN	F	42.5	42.3	85	2	13	2007
[24]	GaAs	F	5	19	68	2	14	2005
This work (measured)	GaN	AB	15	30.5	65.7	2.5	9.3	2012
This work (simulated)	GaN	E	20	31	70	2.5	10	2012
This work (measured)	GaN	E	12	30.1	64.4	2.6	10.6	2012

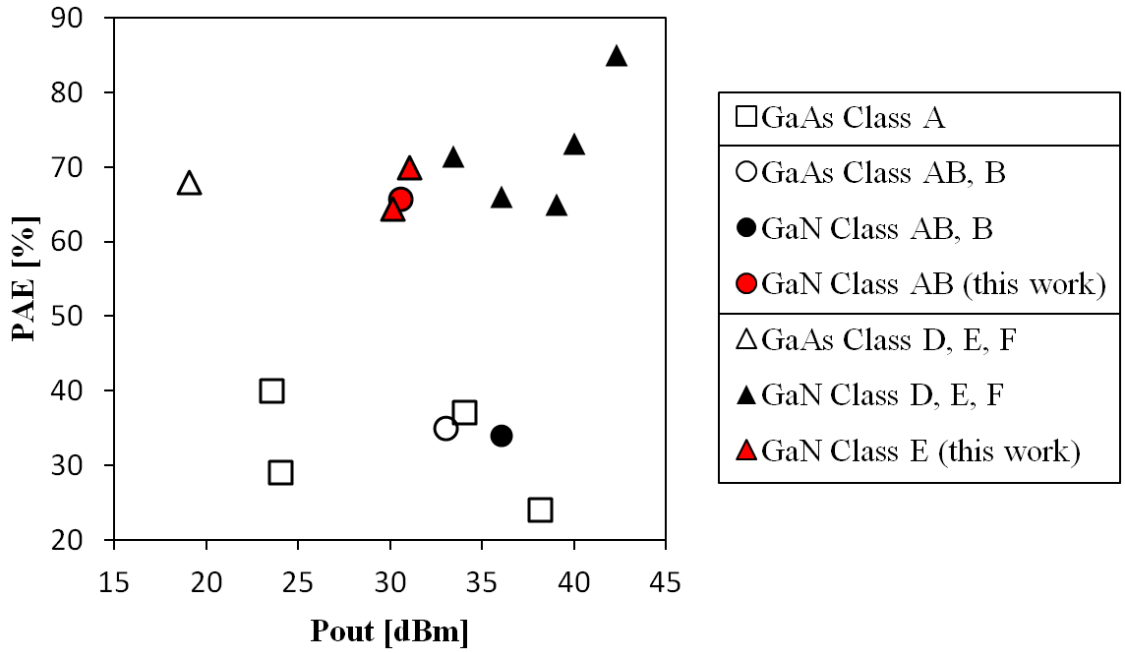


Figure 6.8: Summary of recent GaAs and GaN HEMT PA PAE vs. output power.

From plotted output power and PAE shown in Figure 6.8, this work can be seen as bridging the gap between the strengths of GaAs and GaN by using GaN at relatively lower output power levels but maintaining its ability to achieve high efficiency. Further PA design with appropriately sized GaN HEMT devices should be able to continue the trend shown and achieve very high efficiency at power levels suitable for commercial mobile handset applications.

6.2. Future Work

6.2.1. Modeling

Additional switching PA design with increased attention to stability issues would lead to more straight forward verification of the model.

Without sacrificing the simplicity of the model described, additional work could be done to improve the model accuracy. The results of the PA design described in this thesis could be used as a first iteration and the model could be tuned to reflect the discrepancies between modeled PA circuits and measurements of the fabricated circuits. The drawback to this approach is the long time delays and cost involved in PA fabrication. The use of a hardware harmonic load/source-pull measurement setup would be beneficial to quickly iterate the tuning of model parameters to improve the agreement between simulation and measurements.

6.2.2. GaN HEMT

The timeline of the work described in this thesis was prohibitive to completing PA design cycles using the GaN HEMT devices produced at MIT due to setback in device fabrication and testing. By finalizing and verifying the model described using the mature and reliable Cree HEMT devices, the next step would be to model the MIT devices and design PA circuits for the purposes of varying the performance of those devices in PA circuits.

Additional PA design work could also be performed to further demonstrate the benefits of GaN HEMT devices in the 1-2 W S-band range by designing more complex architectures as described in chapter 2. It would also be beneficial to design PA circuits to operate in commercial modulation schemes, thus demonstrating real-world benefits of GaN HEMT devices.

6.3. Summary

This thesis described a quick and simple large-signal modeling approach for GaN HEMT devices. The model is tailored for use in 1-2 W S-band PA circuits. This was done

in order to advance research in this operating regime by enabling quick turnaround (device fabrication, model extraction, circuit design) in order to evaluate and use custom GaN HEMT devices in circuits. With such a rapidly extracted simple model, optimal GaN HEMT designs could be converged upon, at which point a more sophisticated model could be used requiring longer extraction time and more expensive procedures.

The entire model is extracted from standard small-signal S-parameter measurements and DC IV curves using an RF probe station, as opposed to additional temperature measurement equipment and custom test fixtures as described in [5]. This model has the additional benefit of avoiding the need to forward bias the gate junction, as described by [9].

Both the devices and their models were demonstrated by the design, fabrication, and testing of both a class AB and a class E PA, which were described and shown to possess properties of many standard PA classes used in a variety of PA architectures. The described PAs were shown to occupy a design region relatively untouched by both GaAs and GaN HEMT PAs in terms of output power and PAE.

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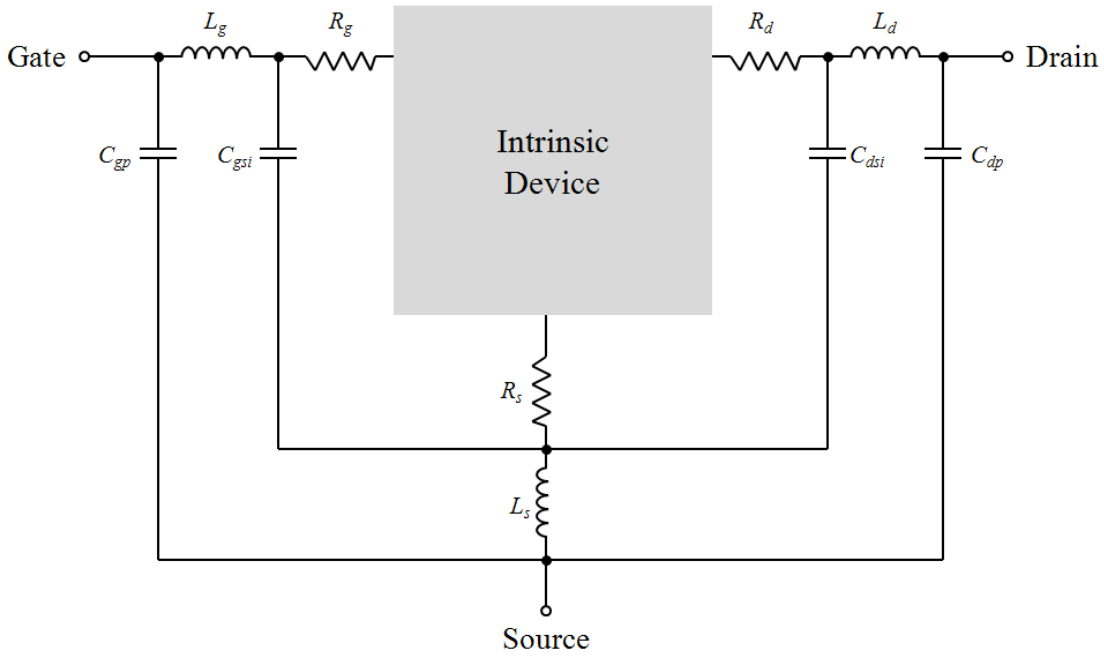
Appendix A. Intrinsic Extraction Procedure

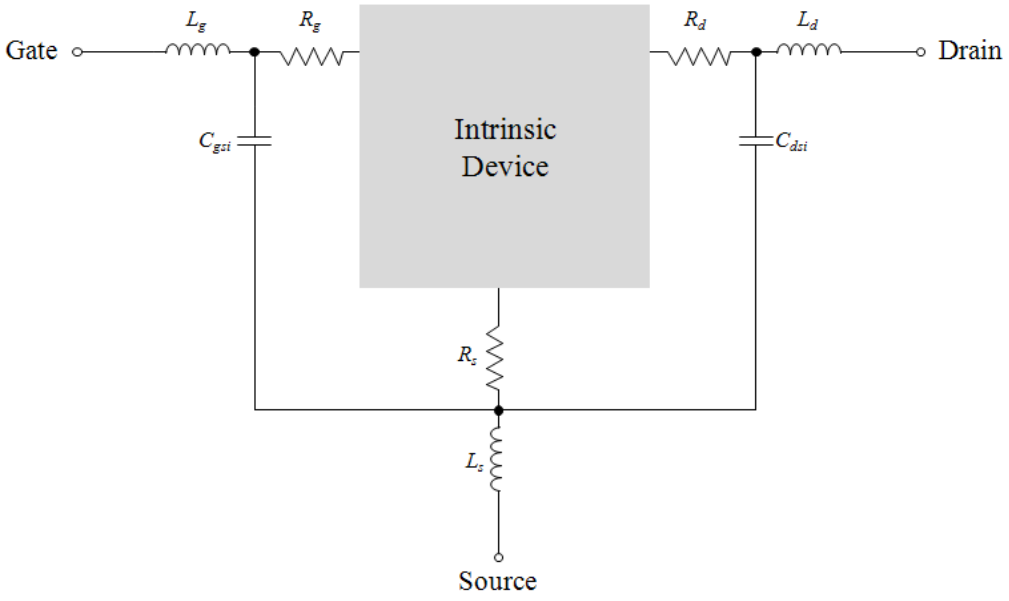
This appendix describes the extraction of the intrinsic device from measured S-parameters as described in [9]. The measured S-parameters describe both the extrinsic and intrinsic device.

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$



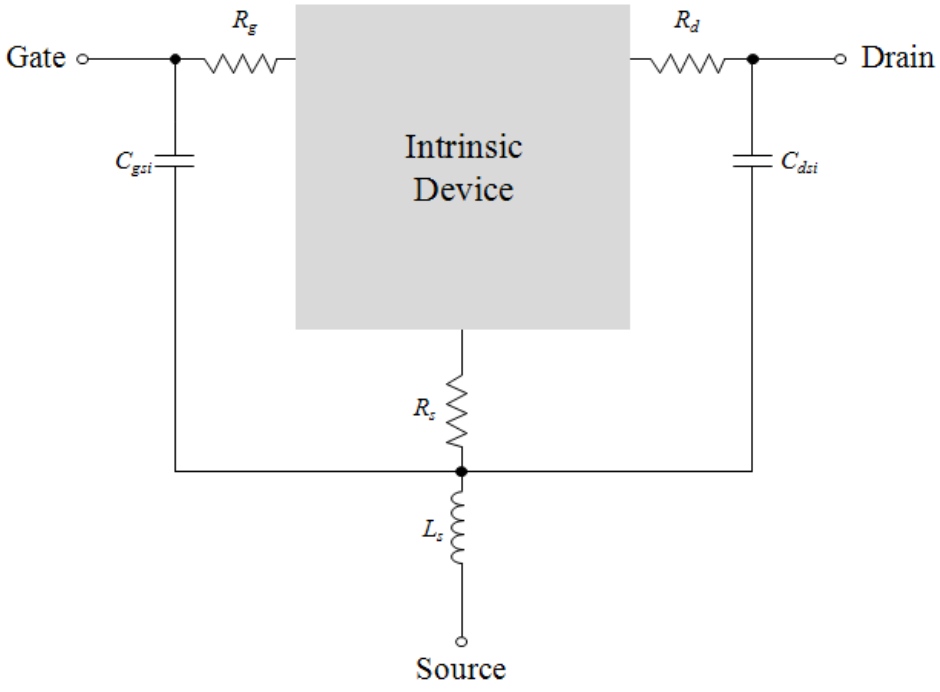
By converting the S-parameters to Y-parameters using the method described in most textbooks on the topic of microwaves, such as [44] or [41], then performing the following operations, C_{gp} and C_{ds} may be removed from the measurements.

$$\begin{bmatrix} Y_{11}\text{-}j\omega C_{gp} & Y_{12} \\ Y_{21} & Y_{22}\text{-}j\omega C_{dp} \end{bmatrix}$$



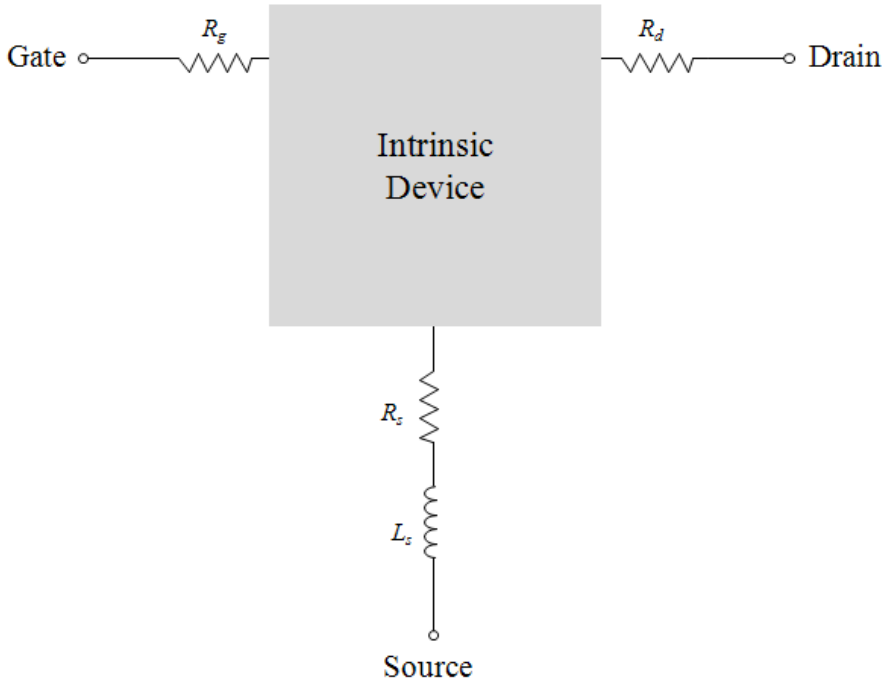
The resulting Y-parameter matrix may be converted to a Z-parameter matrix and the following operations will remove L_g and L_d from the measurements.

$$\begin{bmatrix} Z_{11}\text{-}j\omega L_g & Z_{12} \\ Z_{21} & Z_{22}\text{-}j\omega L_d \end{bmatrix}$$



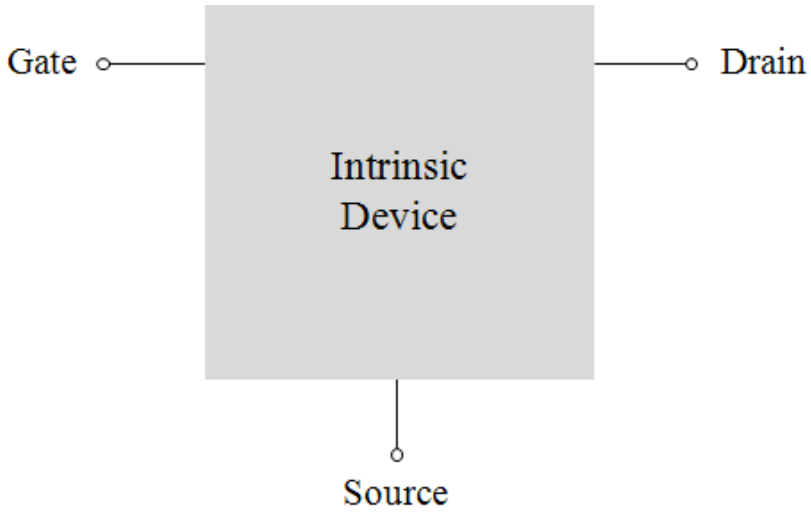
The resulting Z-parameter matrix is converted to a Y-parameter matrix and the following operations will remove C_{gsi} and C_{dsi} from the measurements.

$$\begin{bmatrix} Y_{11}\text{-}j\omega C_{gsi} & Y_{12} \\ Y_{21} & Y_{22}\text{-}j\omega C_{dsi} \end{bmatrix}$$



Converting the resulting Y-parameter matrix to a Z-parameter matrix and performing the following operations will result in a Z-parameter matrix describing only the intrinsic device.

$$\begin{bmatrix} Z_{11}\text{-}R_s\text{-}R_g\text{-}j\omega L_s & Z_{12}\text{-}R_s\text{-}j\omega L_s \\ Z_{21}\text{-}R_s\text{-}j\omega L_s & Z_{22}\text{-}R_s\text{-}R_d\text{-}j\omega L_s \end{bmatrix}$$


Gate
Drain
Intrinsic
Device
Source