Aerosol Jet Deposited Conductors and Dielectrics for Rapid Fabrication of Heterogeneous Electronic Systems

Submitted By
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IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF
MASTER OF SCIENCE IN MECHANICAL ENGINEERING

School of Engineering
Tufts University
Medford, Massachusetts
May 2016
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Abstract

This thesis describes a new method of rapid manufacturing complex printed circuit boards (PCB) using aerosol jet deposition of both conductors and insulators. A process for the rapid manufacturing of complex multilayer circuit boards, specifically a transceiver circuit, with commercial off-the-shelf (COTS) integration is demonstrated leveraging the aerosol jet printing system. This research provides a method for making a system-on-a-chip circuit on a variety of substrates with novel integration methods while minimizing spatial and geometric interference to the broader device. A unique manufacturing process was developed for non-embedded components which involves the building up of the circuit around the system's microprocessor. This technique, in conjunction with board redesign, could be employed to eliminate the need for conductive epoxy attachment of COTS components. The transceiver circuit and its microprocessor, based off a commercially available circuit, were successfully programmed and the program executes. The radio frequency (RF) matching network proved more challenging to produce. Dielectric thickness consistency appears to be a primary issue in the implementation of the RF network.

To the best of the researchers’ knowledge, this research is novel in that it is the multilayer circuit with the most functional capability that has been built using aerosol jet printing technology. The fabrication process for the board, including component placement, has been streamlined to take approximately 10-12 hours. Improvement of board fabrication yield, currently around 25%, is under investigation. Multiple possible strategies are available to improve yield. In this work, we demonstrate a proof of concept functional prototype. The work was extended to the evaluation of long-term reliability and applicability to other non-planar geometries including a MEMS acoustic array.
Acknowledgements

First I would like to thank my family for supporting me throughout my educational career. Their moral and financial support made it possible for me to get my BS and MS degrees from Tufts University. There are also countless teachers, professors, mentors and friends throughout the years that have helped guide me down research oriented path I have ended up on. Specifically I would like to thank Robert White for taking me on as a Summer Scholar. That opportunity opened I lot of doors for me that I am very grateful for. I would also like to thank Brian Smith for hiring me as an intern and starting me down the path towards my master’s degree. I can’t even fathom how much of his time I have taken with my sporadic questions throughout the week. Without his and Rob’s guidance along with the support of Draper, I don’t know if I would have sought out an advanced degree. I am very glad I did. There were also several other Draper affiliated people I would like to thank for their crucial contributions to the research. First I would like to thank Yen Wah, who always was willing to help me no matter how busy she was. It is no exaggeration to say she was fundamental to the success of my research. I would also like to thank Pat Barry and Jon Obrien for extensive contributions to the testing and the RF redesign of the modules I built respectively. Matt Griffin also greatly contributed with assisting with the creation of the initial transceiver circuit design. Last but not least, I would like to thank Abbie Spencer and Else Vedula for all the technical and moral support in respect to using the Optomec.
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Table 6.9: The failure of the silver modules on the polyimide is detailed in this table. As can be seen, all the silver structures fail under the weakest tape. It is important to note that the adhesive failure appears to be between the polyimide film and the SiO$_2$ substrate and not the silver/polyimide interface.

Table 6.10: The failure of the CNT modules on polyimide is detailed in this table. Once again complete failure is observed when tested with the weakest tape. It is important to note the adhesive failure appears to be between the polyimide and the SiO$_2$ substrate and not the CNT/polyimide interface.
1 Introduction

This thesis describes a new method of rapid manufacturing complex printed circuit boards (PCB) using aerosol jet deposition of both conductors and insulators. One of the fundamental advantages this process provides is the creation of flexible circuits, which are not confined to two-dimensional planes. These 3D circuits can conform to a vast array of surfaces allowing circuit integration into locations not suited for planar circuits. Specifically, this research will provide a method to making a system-on-a-chip (SOC) circuit on a variety of substrates with novel integration methods. This fits well into the recent research phenomenon deemed “the internet of things.” By advancing the manufacturing capabilities for a system that can measure and transmit data, one can integrate such circuits with minimal spatial and geometric interference to the broader device. For example, a SOC can be printed directly onto a carrying device so that it takes data from that device and broadcasts the information.

Another potential ramification of this research is the reduction of the design and fabrication cycle for a PCB. As Macdonald et. al. state, “The traditional electronics manufacturing procedure to prototype electronics was to implement bread board prototypes and to accept the inherent delays that come with the normal process of electronics manufacturing, possibly weeks or even months” [1]. Therefore the design cycle can take anywhere from weeks to a year depending on factors such as board complexity. As such, the design process is hindered through caution since there is only one shot at producing a successful board per design cycle. The introduction of additive manufacturing to this process may allow for rapid design enhancements thus allowing for more radical feature integration.

A further benefit of the thesis research is the creation of a process for which the material subsets can be varied. This can have implications for a wide variety of material sensitive applications. For example, many metal conductors are not biocompatible with the human body. The developed process allows for the substitution of these metals with more biocompatible conductors. Other benefits can be
obtained through different materials’ intrinsic properties. For example non-metallic conductors such as carbon nanotubes can make x-ray invisible circuits for technology protection applications. This research helps to broaden the scope of applications for “the internet of things” with flexible circuitry and integration. The use of aerosol jet technology is also leveraged for a sensor packaging application. Lastly rapid ageing data was taken to determine the long-term viability of these inks.

1.1 The Growing Niche for Printed Electronics

Traditionally, printed circuit boards (PCBs), sensors and their constituent components are fabricated through batch fabrication processes including sputtering, evaporating, or plating metals, photolithography and etching. Although these processes are well defined after many years of implementation, they have inherent shortcomings. For example, traditional fabrication is an intrinsically 2-D and planar process. Another shortcoming is the wasted material used for these batch subtractive processes. Many R&D applications are interested in a single digit number of devices, not the dozens to thousands and even millions traditional methods create.

The lead-time for traditional devices can also be problematic. This long lead-time hinders the innovation process as it gives the engineer one shot to make a functional device. This constrains the designer to conservative design rules, resulting in slow advances in technology.

Microelectronics is a growth market, open for new manufacturing methods. As Hon et. al. comment, “There is a trend for modern products to become more multifunctional and compact, with a higher expectancy of quality and reliability and a shorter life-cycle. There are increasing pressures to reduce materials content, energy consumption during manufacture, and to present a smaller carbon footprint to meet the requirements of sustainable development” [2]. This can also be observed in the market data for additive manufacturing (AM) processes as shown in Figure 1.1. As can be observed from the figure, the last five years show a quadrupling of revenue [3]. These problems with the traditional microfabrication process leaves a niche that printed electronics has begun to fill.
Printed electronics are electronics built from selective deposition or etching on a substrate. This technology is a subset of additive manufacturing that fundamentally requires integrating at least two disparate materials (conductor and insulator), which is a bigger challenge than much of the AM market that focuses on single material optimization. Instead of the entire surface being covered in a material then partially removed (“subtractive”), selective material deposition only uses material where it is needed (“additive”). This method also has implications beyond material conservation. Printed electronics can be employed to achieve flexible electronic systems since most of these methods are less sensitive to surface topology than the 2D methods of traditional microfabrication. In a review of flexible electronics, Nathan et. al. state, “Reduced cost, large area, roll-to-roll, and flexible systems, such as low-cost flexible displays, require conformal, distributed, and integrated functionality, which is hitherto unavailable from more traditional brittle material and device platforms” [4]. The ability of conformal printing massively expands the potential market for printed electronics.
In the same review, industries interested in flexible devices include healthcare, the automotive industry, energy management devices, electronics for hostile environments and wireless systems [4]. For example in healthcare, biosensors could simplify and expedite the diagnosis process. As Nathan et. al. state, “As with lab-on-a-chip (LOC) applications, these thin films will become a key component of our approach to next-generation healthcare. Heat distribution in the body, sweat content, and frequency or postural pressure on part of the body can all reveal vital information on pathological symptoms or recovering stages... LOC is one of the most important microsystems for next-generation healthcare, with promising applications in microanalysis, drug development, diagnosis of illness and disease” [4]. Additive manufacturing can help achieve these goals by printing flexible electronics using diverse end-product compatible materials and substrates.

Printed electronics continue to grow in market space as their application potential is realized. The 3-D printing industry, including printed electronics technology, is evolving rapidly with over a $3 billion market in 2013 [5]. As Singh et. al. write, “The organic electronics roadmap identifies organic and printed electronics market to exceed $300 billion in the next 20 years” [6]. This massive expansion indicates the growing niche printed electronics is beginning to fill and underscores their potential relevance to solving many problems across a plethora of industries.

1.2 Aerosol Jet for Rapid Manufacturing of SOC

An aerosol jet printed transceiver circuit was printed for this research. This circuit has system-on-a-chip (SOC) capabilities, which makes it pertinent to a variety of applications. The multilayer circuit is built up out of silver and polyimide (PI) ink after the placement of a microprocessor in a QFN48 package. The QFN48 package is placed upside down so that it can be glued to the substrate and conductive traces can be printed up the sidewalls to integrate it into the rest of the circuit. It is important to insure there is no airgap between the edge of the package and the substrate. Otherwise the conductive ink will have difficulty traversing the crack. This component placement was done first due to the challenges of
accurately placing components. By placing the component first and printing the circuit based on that component, the location of the QFN48 on the substrate is not important. It was done for this package and not any of the other components due to the signal line density of the package and the pitch of the package pads. The challenges of accurately placing a module with 12 pads per side with approximately a 200 µm pitch were thus avoided.

After the placement of the QFN48 package, the ground plane was then printed along with the sidewall interconnections (from package pad to circuit). The ground plane print was done in two passes to reduce the resistance and also to increase uniformity of the layer. The sidewall print was done in 5 passes with the goal of decreasing resistance as much as possible. This layer and the sidewall features were then cured. Subsequently, targeted dielectric deposition was done to shield the ground layer from conductive routing traces on the upper silver layer. The package surface was also used for routing through the deposition of dielectric and silver. After curing, the upper layer silver was then deposited, cured and the rest of the COTs components were placed. This resulted in a programmable SOC, an important milestone for proving the effectiveness of a printed transceiver circuit. By nature of this process, printing this SOC board on a rigid substrate is a direct analog to the same board on a flexible substrate with the exception of sintering based on the substrate material. This is due to the versatility of the print method, which makes the print onto most substrates, flexible or rigid, fairly straightforward. Therefore this research provides an avenue to reduce the technology gap between SOC capabilities and flexible circuitry.

Accelerated ageing data was also taken to determine ink reliability (i.e. whether conductors/insulators degrade) and the feasibility of aerosol jet printed (AJP) circuits for reliable device manufacture. Two rapid ageing tests based on IPC standards were done along with a test of ageing at elevated temperature. All data obtained from these three tests were analyzed for resistance change and failure of the modules. Adhesion test structures were put into the rapid ageing environments in order to
qualify the adhesion change in the printed material over exposure time to the environment. Since adhesion is the primary failure mechanism of printed electronics, it was deemed necessary to qualify it with respect to the ageing environments. For the wafers going into the rapid ageing environments, the silver ink was sintered at 250°C for 1hr 20 min per layer while the CNT structures were sintered at 40°C for 2 hours. These testing modules were multilayer structures, so the bottom layer experience twice the bake of the top layer. More specific detail can be found in the “Ink Ageing and Reliability” section. The accelerated ageing wafer with silver ink was sintered at 150°C for 2 hours while the CNT ink was sintered for 2 hours at 40°C.

IPC-TM-650-2.6.7.2a Thermal Shock was used to determine the reliability of operational and storage temperature regimes. The ageing structures were exposed to temperatures of -55°C to 125°C in 15 minute cycles. The test structures were tested before environmental testing, then again after 50, 150, 379, and 1000 cycles. For the silver ink, this data showed no statistically meaningful change in mean resistance, however there was a large change in standard deviation. This appears to be related to adhesive failure of many of the structures resulting in variable resistances. Over 40% failure of modules is observed by the end of the testing. Adhesion tests verify the weakening bond between the printed conductor and the substrate as environmental exposure increased. For the CNT ink, no meaningful change in resistance can be determined with only 7% failure of the structures after the 1000 cycles were completed. Adhesion for the CNT ink was never stronger than 30 oz-force/in and usually resulted in failure at the weakest tape strength 16 oz-force/in. The adhesion test method is described in the section “Resistance and Adhesion Testing Procedure.”

The second rapid ageing environment was based on IPC-TM-650-2.6.3F Moisture and Insulation Resistance. This environment was in the 50°C/85% relative humidity regime and the exposure lasted seven days with intermittent testing. This environment was used to characterize conductor and insulator degradation or changes in performance in a moist environment. For the silver ink, the mean of the
resistance change data appears to be decreasing, however it coincides with an increase in the standard deviation. Therefore, it doesn’t appear an meaningful statistical variation is happening between the test. The structures experience 7% failure by the end of the test, drastically less than the 40% of the thermal shock testing. The adhesion test data verifies this as structures are able to survive the strongest adhesive tape, 90 oz-force/in, as compared to the thermal shock test. Therefore it appears the printed structures performed well in this environment. For the CNT ink, the resistance mean is increasing along with the standard deviation. Mechanisms such as CNT adhesion to the substrate may be causing this result. Module failure peaks at just over 2.5% showing a low rate of module failure during the testing. Adhesion for these CNT structures is poor as shown in “Ink Ageing and Reliability.”

Lastly, an accelerated ageing test was done on some modules at 60°C. These modules were aged for months to determine the effects of long-term heat exposure. This environment was the least controlled as it was simply an available oven in a lab. Since the silver modules’ sintering temperature was much lower than the rapid ageing modules sintering temperature, the devices could be further sintered. This is reflected in the resistance change data as the resistance has been statistically significantly decreasing for over 8 months. The module failure rate on this device is also next to zero, with all failures introduced in the printing of the structures. The CNT ink shows a unique pattern of getting more relatively resistive initially then getting less resistive as the test goes on. The mechanism for this behavior is still being investigated and requires further analysis. The CNT ink has a module failure rate between 8-10% which is largely a consequence of the printing process. Only around 2% module failure was documented throughout the testing. No adhesion tests were performed on these structures.

1.3 Contributions

To the best of the researchers’ knowledge, this research is novel in that it is the most complicated multilayer circuit that has been built using aerosol jet printing technology. This specific circuit enables a
host of geometrically dependent applications along with providing manufacturing flexibility to electronics manufacturing. The inherent advantages of using a direct print, non-contact printing methods enable this process to create a complex PCB to be used in applications with varying geometry, and substrates. By nature of this process, printing this SOC board on a rigid substrate is a direct analog to the same board on a flexible substrate with the exception of sintering based on the substrate material. This is due to the versatility of the print method, which makes the print onto most substrates, flexible or rigid, fairly straightforward. Therefore this research provides an avenue to reduce the technology gap between SOC capabilities and flexible circuitry.

This research is also distinctive in that it is potentially the first in PCB manufacture that actually places a non-embedded component before the manufacture of the PCB. This technique greatly simplifies alignment and placing challenges experienced with high pad density packages. This thesis allows for the long design and fabrication cycle of boards to be cut down so that more ambitious iterations can be done in less time. The research also broadens the applicability of “internet of things” devices to be constructed of and printed on a variety of materials.

To the best of this researcher’s knowledge, the ageing data collected is a unique contribution to the field for a variety of reasons. First, aerosol jet printed CNTs, an organic conductor, were tested with IPC ageing standards to determine their reliability. Despite a plethora of research into the use of CNTs for a variety of applications, there is not as much literature analyzing their reliability. Second, the IPC rapid ageing tests done on silver ink were on multilayer structures. These structures included a dielectric patch that prevented two lines from shorting. Lastly, the effects of ageing for both CNTs and silver with the traces shielded vs. unshielded by dielectric were also examined. To the best of this researcher’s knowledge, this multi-material analysis has not been done before.
2 Background

2.1 Rapid Prototyping Electronics

Rapid manufacturing in general can be traced back to the late 80’s [7]. A review written in 2003 on rapid manufacturing by Levy et. al. discusses the history of these processes [7]. Table 2.1 depicts the development years of several standard rapid prototyping technologies. At the time this article was written, Levy et. al. state “over the last decade 30 companies developed and marketed [rapid prototyping] machines based on different physical principles and implantation concepts [see Table 2.1]” [7]. In Table 2.1, there is a difference between Fused Deposition Modeling (FDM) and 3D Printing (3DP). FDM works through the extrusion of plastic or metal filaments through a nozzle while 3DP works by the deposition of a liquid binder deposited on a powder. The powder is spread between each layer that is printed.

<table>
<thead>
<tr>
<th>Name</th>
<th>Acronym</th>
<th>Development years</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stereolithography</td>
<td>SLA</td>
<td>1986 - 1988</td>
</tr>
<tr>
<td>Solid Ground Curing († = year of disappearance)</td>
<td>SGC</td>
<td>1986 – 1988 1999†</td>
</tr>
<tr>
<td>Fused Deposition Modelling</td>
<td>FDM</td>
<td>1988 - 1991</td>
</tr>
<tr>
<td>Selective Laser Sintering</td>
<td>SLS</td>
<td>1987 - 1992</td>
</tr>
<tr>
<td>3D Printing (Drop on Bed)</td>
<td>3DP</td>
<td>1985 - 1997</td>
</tr>
</tbody>
</table>

*Table 2.1: Rapid Prototyping technologies and their development years [7].*

2.1.1 Hybrid Additive Manufacturing

Fundamentally, additive manufacturing of electronics vastly reduces the number of processing steps needed for device development as shown in Figure 2.1. The rapid prototyping of electronics is an essential component towards proving the viability of rapidly produced additive manufactured (AM)
systems. As such, there are a variety of manufacturing techniques for the rapid prototyping (RP) of electronics. However, most electronics manufacturing techniques require a hybrid manufacturing approach. As summarized by Macdonald et. al., “in the context of prototyping electronic circuits, which are increasingly encased in 3D forms, rapid prototyping only provided fit and form verification of the housing. In order to verify functionality, a separate bread boarding activity was required that did not integrate the verification of form with function —two separate activities... these deficiencies have begun to be addressed through enhanced 3D printing. Such as [SLA] or FDM, in combination with both conductor embedding and robotic pick-and-place” [1]. Both SLA and FDM are well researched techniques employed in rapid electronics manufacturing. Figure 2.2 depicts a standard process flow involving FDM printing. As Joshi et. al. state, “The advances in the AM techniques have only recently been explored in the context of electronics integration. The hybrid additive manufacturing enabled by the design freedom of AM techniques and additive printed electronics technology is changing not only how things are made, but what is made” [8].

![Figure 2.1: A comparison between traditional subtractive IC processing and additive printing for device development](image)
Espalin et. al. contrasts a stereolithography technique and an FDM-based technique for the manufacture of 3D-printed electronics [9]. For the stereolithography (SL) technique, the dielectric structure was fabricated with SL while conductive inks were used in channels for interconnection between components. As Espalin et. al. state, “In spite of the structure passing qualification—including temperature cycling, shock and vibration, and outgas testing—the photocurable materials in SL do not provide the level of durability required for long term-functionality” [9]. The FDM technique was combined with a thermal embedding technology to submerge copper wires in the dielectric structure during the FDM process. To accommodate some of the shortcomings of FDM, primarily surface finish, feature size and porosity, a hybrid approach was used which also included laser ablation and micromachining capabilities [9]. In fact Espalin et. al. used FDM with direct printing methods to functionalize electronics. Work done by this group is shown in Figure 2.3, Figure 2.4, and Figure 2.5. These figures are of a magnetic flux system, a novel fabrication system, and an electronic gaming die respectively. Macdonald et. al. used stereolithography and embedded conductors to fabricate an
electronic game die as show in Figure 2.5. The reduction of manufacturing time for the prototype was significant. As Macdonald et. al. state, “by applying 3D printing of structural electronics to expedite prototyping, the development cycle was reduced from weeks to hours” [1].

Figure 2.3: A magnetic flux sensor system using stereolithography, developed by Espalin et. al., with curved surfaces and surface mount components, conductive ink interconnects, LEDs, Hall effect sensors, and power supply connectors [9].

Figure 2.4: A fabrication system which used FDM and thermal embedding of copper wires (left) and a fabrication schematic (right). Two FDM machines are integrated together to enable multi-material prints. The middle compartment of the tool can have a variety of capabilities including thermal embedding of wires, component placement, micromachining, and ink dispensing. Components placement can be done during process interruption [9].
Another major technique for rapid manufacture of printed electronics is powder based printing. This method uses a 3D powder bed-based printer, such as a Voxeljet AG as shown on the left in Figure 2.6, to deposit powder in the appropriate locations. Then a cylindrical recoater planes the deposited powder and a binder material is applied by another printhead. An enhanced version of this technique which enables integration of conductive lines and COTs components was developed by Hoerber et. al. and is shown on the right in Figure 2.6. The exact techniques employed for steps 4-6 are described in the paper [10]. Cryzewski et. al. used a plaster-based powder, binded by an inkjet printed liquid binder, then infiltrated with a dispersion of carbon nanofibers in an epoxy resin [11]. This method worked due to the porous nature of the powder bound model. As Cryzewski et. al. state, “First, a model is made of powder deposited layer-by-layer and bound by an inkjet printed liquid binding agent. As a result, a relatively weakly bound, fragile, porous, and permeable structure is formed. In the second step, the structure is impregnated by hardenable infiltrant, e.g. based on epoxy resin, which, after curing makes the prototype stiff and durable enough to handle. The electric conductivity can be added to the model in the
second step by adding an electrically conductive filler to the infiltrate” [11]. Such methods are good examples of hybrid technology to create conductive components.

Another technique to make multilayer devices was done by Hübler et. al. The group made 3D circuits by physically stacking layers of printed inverter stages for a ring oscillator [12]. The results of this technique are shown in Figure 2.7.

Figure 2.7: Multilayer ring oscillator composed of stacked planar circuits [12].

Other research has gone into effectively simulating printed circuits. In order to reduce the “trial-and-error” fabrication strategy often used with printed organic electronics, Bartzsh et. al. developed a
model to simulate the behavior of printed organic circuits. As Bartzsh et. al. state, “With the model it is possible to simulate device parameters of printed transistors and inverters with high accuracy. Furthermore, more complex circuits can be easily simulated both in terms of static and dynamic behaviour” [13]. Such models expedite the design process thus enabling rapid prototyping by helping to create a functional product.

One subset of RP electronics that has been explored is radio frequency (RF) electronics. Additive manufacturing not only decreases the manufacturing time for antennas, it can enable unique geometries that leverage size reduction with the maintenance of efficiency [14-17]. One advantage of these 3-D designs is their ability to make efficient use of available volume for radiation [16]. Non-antenna structures have also been fabricated. Obrien et. al. also developed the first high frequency phase shifter fabricated with additive manufacturing [18]. Such research indicates the interest in rapid prototyping of high frequency electronics, not just A/C and DC. Some basic RF design is done in this thesis.

Hybrid manufacturing methods have been essential to pioneering RP electronics manufacturing. As Macdonald et. al. state, “The use of advanced 3D printing technology enhanced with component placement and electrical interconnect deposition can provide electronic prototypes that can now be rapidly fabricated in comparable time frames as traditional 2D bread-boarded prototypes; however, these 3D prototypes include the advantage of being embedded within more appropriate shapes in order to authentically prototype products earlier in the development cycle” [1]. Since the publication of Macdonald et. al., newer technology has been developed and commercialized to further 3D circuit manufacturing technology.

2.2 Direct Writing Manufacturing Techniques for Printed Electronics

Direct writing (DW) technology is the focus of a plethora of research on rapid electronics manufacturing. According to Hon et. al., a precise and accurate definition for DW is that “direct writing
denotes a group of processes which are used to precisely deposit functional and/or structural materials on to a substrate in digitally defined locations” [2]. As can be seen from Figure 2.8, four major distinct processes define DW: Droplet, energy beam, flow and tip. Droplet based processes encompass ink deposition onto a substrate where drops of a liquid are deposited through a nozzle. Energy beam processes involve the use of lasers or ion beams in the deposition of materials. Flow-based processes all “require a positive mechanical pressure to achieve micro-dispensing through a positive displacement pump, air pressure or extrusion through a syringe” [2]. Tip-based processes involve the dipping of an AFM probe into an ink then transferring it to the substrate through capillary transport [2]. Table 2.2 shows a brief comparison between all these methods excluding laser-based methods. This thesis will focus on droplet DW methods, specifically aerosol jet. A brief discussion of ink-jet printing is included in order to contrast with the process used in this research (aerosol jet), as it is the most analogous and is a more mature process.

![Figure 2.8: The primary processes of direct writing based on the methods of material transfer [2].](image)
Table 2.2: Summary of direct writing processes. Note laser based methods are not included [2].

<table>
<thead>
<tr>
<th>Process characteristics</th>
<th>Methods</th>
<th>Mechanisms</th>
<th>Line width ($l_w$) or droplet dia. ($D_d$)</th>
<th>Deposition rate or writing speed</th>
<th>Materials</th>
</tr>
</thead>
<tbody>
<tr>
<td>Droplet</td>
<td>Inkjet continuous</td>
<td>Deposition of liquid droplets, generated by break-up of continuous jet</td>
<td>$l_w$ from 20 μm to &gt;5 mm, $D_d$ from 10 to 150 μm, typically 120 μm</td>
<td>0.25 mm/s with a single nozzle</td>
<td>Liquid with viscosity 2–10 mPa s, can contain small particles</td>
</tr>
<tr>
<td></td>
<td>Inkjet drop-on-demand</td>
<td>Deposition of liquid droplets, generated individually when required</td>
<td>$l_w$ from 20 μm to &gt;5 mm, $D_d$ from 10 to 150 μm, typically 50 μm, $l_w$ from 5 μm to 5 μm, $D_d$ from 20 nm to 5 μm</td>
<td>To 0.3 mm/s with a single nozzle</td>
<td>Liquid with viscosity 10–100 mPa s, can contain small particles</td>
</tr>
<tr>
<td></td>
<td>Aerosol jet</td>
<td>Kinetic bombardment of atomized droplets</td>
<td></td>
<td></td>
<td>Any materials that can be atomized plus biomaterials such as cells</td>
</tr>
<tr>
<td>Flow</td>
<td>Pump</td>
<td>Precision micro-dispensing pump with push-back action</td>
<td>$l_w$ from 25 μm to 3 mm</td>
<td>Max $v_w$ is 300 mm/s, typically 50 mm/s</td>
<td>Liquid, paste and slurry materials up to 1,000,000 mPa s</td>
</tr>
<tr>
<td></td>
<td>Extrusion</td>
<td>Syringe-based and flow distribution block</td>
<td>$l_w$ from 50 μm to 2.5 mm</td>
<td>Typical $v_w$ is 25.4 mm/s</td>
<td>Liquid, paste and slurry materials up to 500,000 mPa s</td>
</tr>
<tr>
<td>Tip</td>
<td>Dip pen nanolithography (DPN)</td>
<td>Molecular deposition via an AFM tip</td>
<td>$l_w$ from 10 nm to a few μm</td>
<td>Typical range is 0.2–5 μm/s</td>
<td>Molecule thiol, macromolecule, nanoparticles</td>
</tr>
<tr>
<td></td>
<td>Nanofountain pen (NFP)</td>
<td>Capillary action of micro-pipette and the substrate</td>
<td>$l_w$ from 40 nm to over 1.15 μm</td>
<td>Typical $v_w$ is about 0.4 μm/s</td>
<td>Monomer, nanoparticles</td>
</tr>
<tr>
<td>Energy beam</td>
<td>Focussed ion beam (FIB)</td>
<td>Ion-induced deposition of precursor gas molecules</td>
<td>$l_w$ from 80 nm to 20 μm</td>
<td>Typical deposition rate is 0.05 μm/s</td>
<td>Metals and insulators</td>
</tr>
</tbody>
</table>

2.2.1 Ink-Jet Printing

Ink-jet printing is a primary means of printing electronics. Fundamentally ink-jet printing is where ink is deposited through a nozzle and is carried by gravity and momentum to the substrate surface. Upon colliding with the surface, the ink droplets spread out into a thin film layer. This process has many advantages over other electronic manufacturing methods. As Singh et. al. note, “The appeal of the technology lies in it being a non-contact, additive patterning and maskless approach. Direct write attribute of ink-jet printing allows for deposition of versatile thin films, the designs of which can be changed with ease from batch to batch. Other attractive features of this technology are: reduced material wastage, low cost and scalability to large area manufacturing” [6]. Traditional fabrication costs also arise in the form of high processing temperatures and clean environment maintenance, something that can be avoided with ink-jet printing. Lastly, ink-jet printing has potential compatibility with roll-to-roll manufacturing, the gold standard in efficient and scalable production. Such compatibility would render the printing of flexible electronics highly cost effective. As Caglar et. al. state, “Ink-jet printing technology offers substantial electronics manufacturing advantages in decreasing the manufacturing cost and material waste, and in increasing the production flexibility” [19]. Mäntysalo et. al. analyzed the
capabilities of ink-jet printing with a focus on using six sigma methodology [20]. This group’s work
includes ink-jet printed interconnections and conventional passive components (i.e. silicon chips) to
create System-in-Package modules [20].

As shown in Figure 2.8, Ink-jet printing is primarily divided into two major categories, continuous
mode and drop-on-demand (DoD). Continuous mode is defined by the continuous output of ink onto the
substrate. This method is governed by the Plateau-Rayleigh instability since the liquid that comes out
the nozzle breaks into discrete drops [2]. The DoD method forces ink out the nozzle selectively when it
needs to be printed. Common methods of DoD actuation are piezoelectric and bubble-jet [2]. Bubble-jet
technology uses a heating element and vapor pressure to force the ink from the nozzle.

The material flexibility of ink-jet printing enables the construction of devices from a wide range
of materials. Silver, copper and gold are all commonly used metals solubilized in inks [21]. Polymers and
along with other non-metallic materials are also frequently printed using this technology. Cho et. al.
printed high-capacitance dielectrics used as gate insulators in organic thin film transistors [22].
Sirringhaus et. al. printed all-polymer transistor circuits including via hole interconnections [23]. Forrest
[24] forecasts the organic electronic industry also being affected by the printed electronics
phenomenon. In a review paper on low-cost organic electronic appliances on plastic, he notes that ink-
jet printing provides the crucial ability to locally pattern devices in comparison to full-surface deposition
techniques [24]. For example, the fabrication of color displays requires three closely spaced red (R),
green (G) and blue (B) polymer organic light-emitting devices (OLED). As Forrest states, “The R, G, and B
sub-pixels must be separately contacted and energized such that their intensities can be individually
controlled to achieve both the desired color and intensity grey-scale. Unfortunately, using spin-on or
spray-on methods, the entire substrate is coated with only a single material, requiring different
strategies for such a lateral functionalization... one emerging [fabrication] strategy is ink-jet printing”
The ink-jet printed OLED displays from this review are shown in Figure 2.9. Denneulin et. al. used a carbon nanotube ink to analyze nanotube orientation based on ink formulation [25].

Ink-jet printing is a technology that has both benefits and detriments. Singh et. al. state these qualities as follows:

Unlike ink-jet printing, traditional deposition approaches involve a great deal of wasted material, but result in a fairly uniform deposition profiles over the substrate. By contrast, ink-jet printing is an anisotropic (localized) deposition process that lends itself readily to patterned writing/maskless processing. Given the inherent cost of lithography steps in industrial manufacture and the imperative to reduce the number and level of complication of such steps, ink-jet printing provides an attractive,
material-conserving alternative for several patterning applications. However, the anisotropic nature of ink-jet printing also gives rise to issues not encountered in planar processing currently used in industry. In closing, ink-jet printing is also a suitable process in situations where deposition of a given material must occur in predetermined locations on a substrate having pre-existing structures and devices that would, otherwise, be contaminated and/or damaged if a vacuum or spin-coating process were used [6].

Despite the rapid expansion of the printed electronics industry, few predict printed electronics will displace current manufacturing methods due to the electrical quality disparity between the two methods. The strengths of the printed methods, then, are in enabling new technologies and potentially “hybrid” manufacturing methods [19, 26] and rapid prototyping and realization of electrical designs. Caglar et al. summarize the main weaknesses of this technology as the “drying of the printhead nozzles, undesirable satellite droplets, uncontrolled spreading of the droplets on the substrate and varying ink-jet-printed layer thickness” [19]. In this sense, it is very similar to aerosol jet technology since this is a fundamental problem among droplet based direct writing processes, as discussed next.

2.2.2 Aerosol Jet Printing

Aerosol jet printing (AJP) is a process that creates a colloid of fine droplets to be deposited on a substrate. AJP is a non-contact process that uses a carrier gas (pneumatic atomization) or ultrasonic energy (ultrasonic atomization) to atomize the material to be deposited. The atomized droplets of material, often 2-5 µm in diameter are then focused into a collimated beam which can range from a 10 µm diameter spot to a 1 cm wide ribbon [27]. The atomized droplets are then shot out of the deposition head at approximately 80 m/s where they ballistically, as a high speed projectile, travel to the substrate.
The focused beam of droplets can hit a substrate accurately from up to 5mm standoff of the nozzle to the substrate. This process is depicted in Figure 2.10.

Initially it may seem aerosol jet printing and ink-jet printing are very similar, yet they have several distinct differences. First the aerosol droplet size is much smaller. As previously mentioned, aerosol jet printing has a drop size on the order of 2-5 μm [27] compared to that of ink-jet which is more directly limited by nozzle size, jetting conditions, surface energy of substrate and viscosity of the ink [6].

In a paper written by an aerosol jet manufacturer [29], Optomec®, the following advantages of the process were noted:
• The ability to accommodate a wide range of inks with high solids loadings and viscosities from 1 to 1000 cP
• Non-contact, conformal printing with high stand-off distances 2-5 mm
• The ability to print on textured, stepped and curved surfaces
• The ability to dynamically control the print rate to create low- and high-resistivity interconnects
• Single nozzle ink print rates up to 10 mg/min
• Printed feature sizes ranging from 10 µm to several millimeters [29]

These capabilities enable technologies that are not easily achieved with other forms of manufacturing such as conformal and 3D printing of conductive and dielectric materials. A large suite of materials are potentially compatible with this technology compared to traditional printed circuit board (PCB) processes. Many materials can be printed as long as the ink, the desired material along with solvents and other chemicals, has a viscosity in the aforementioned range.

A wide array of research has been conducted with AJP despite the technology being in its nascent stages. In 2009, the aerosol jet printing method was used for non-contact metallization of solar cells [30]. Through a multi-nozzle design, Optomec proved both the efficiency of this method, since it allowed for rapid printing comparable to screen printing, while simultaneously reducing the width and thickness of the seed layer needed on the solar cells [30]. One of the most utilized conductor inks in this tool is silver based ink, and is the subject of much of the published work. Research groups have investigated how to print optimal silver traces with aerosol jet technology, along with several other ink types [31-33]. Zhao et. al. combined silver nanoparticles and carbon nanotubes to bridge defects in the printed silver resulting in a 38% reduction in resistivity [34]. Figure 2.11 shows this conductivity enhancing process. Sensors and circuits are also commonly made from silver ink. One such sensor is a strain sensor developed by Zhao et. al. As Zhao et. al. state, “printing electronics inside composite
structures without degrading the mechanical properties [was demonstrated]... strain sensors were successfully printed onto carbon fiber prepeg to enable fabricating composites with intrinsic sensing capabilities” [35]. A hybrid manufacturing technique for device fabrication is often employed in literature. Li et. al. used AJP to print silver electrodes for highly sensitive, aligned carbon nanotube strain sensors fabricated through another process [36].

![Figure 2.11: An SEM image of (a) unsintered silver nanoparticle ink, (b) sintered nanoparticle ink, (c) printed carbon nanotubes and silver, (d) “CNT aggregation with 1 wt.% concentration” [34].](image)

Structures built with non-silver ink types are also prevalent. One popular material used is carbon nanotubes (CNTs). Mingjing et. al. used CNTs to partially print “five-stage ring oscillators with >20 kHz operating frequencies and stage delays <5µs at supply voltages below 3V. The fastest ring oscillator achieved 1.2 µs delay time at 2V supply” [37]. Liu et. al. developed a fully printed all-carbon field effect transistor (FET) on a flexible polyethylene terephthalate substrates [38]. As Liu et. al. state, “The all-carbon-based FET shows a good mobility of 350 cm² (Vs)⁻¹ at a drain bias of -1V. This simple and novel
method explores a promising way to fabricate all-carbon-based, flexible and low-cost electronic devices” [38]. The author of this thesis has also worked with commercial CNT formulations in comparison with other conductive materials. The scope of this work includes the deposition characteristics and the electrical properties of CNTs deposited through AJP [39]. Other carbon inks are also used such as graphene. Jabari et. al. used graphene for interconnects [40].

Others make their own inks including Kim et. al. who used a polymer semiconductor poly (3-hexylthiophene) ink they functionalized in the aerosol jet printer to make electrolyte-gate transistors [41]. Not only was exceptional fabrication reproducibility obtained, Kim et. al. state that the transistors, “display an unusual combination of metrics including sub-1-V operation, ON/OFF current ratios of $10^6$, OFF currents of $<10^{-10} \text{ A (}<10^{-6} \text{ A cm}^{-2})$, saturation hole mobilities of $1.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, threshold voltages of $-0.3 \text{ V}$, and subthreshold swings of $70 \text{ mV decade}^{-1}$. Furthermore, optimized [electrolyte-gate transistors] printed on polyester substrates are extremely robust to bias stress and repeated mechanical strain” [41]. Ceramics devices have also been printed; for example, Folgar et. al. used a barium titanate ink to make multilayer ceramic capacitors [42]. This process used selective laser sintering in order to develop the 3D structures without damaging the substrate [42]. Sukeshini et. al. created a NiO (Nickel oxide) and a YSZ (yttria-stabilized zirconia) ink for printing functionally graded solid oxide fuel cells [43].

The printing of circuit boards and the integration of COTS components has also been investigated. Hoerber et. al. embedded an upside down QFN48 package then integrated it to a circuit [10]. This interconnection is shown in Figure 2.12. Conformal and multilayer demonstrations have been done by Optomec also. As can be seen in Figure 2.13, multilayer structures similar to that printed for the proposed thesis are shown along with conformal prints up a die stack and a printed circuit board on the side of a tank [27]. Lastly a functional circuit board was printed by Optomec using “printed interconnects, printed resistors, printed capacitors, and COTS attachment” [29]. This circuit board is
shown in Figure 2.14. It is important to note this is not a transceiver circuit and does not have the lab-on-a-chip capabilities this thesis is focused on.

*Figure 2.12: QFN 48 package interconnected with silver to a circuit (not shown) on a PMMA substrate. The profilometry image on the top right shows the silver line going on to the QFN48 packages from left to right [10].*

*Figure 2.13: Several aerosol jet prints done by Optomec. A multilayer print with 3 different materials is shown in (a). A die stack integration with a fillet to help connect between layers is shown in (b). A functional circuit printed on the side of the tank is depicted in (c) [27].*
2.2.3 Ink Sintering Methods

One of the critical enabling technologies for the rapid fabrication of printed circuits is the sintering method of the ink. As Kamysny et. al. state, the sintering of inks “can be achieved by exposure of the printed pattern to heat (thermal sintering), intense light (photonic sintering), microwave radiation, plasma, by applying an electrical voltage, and by chemical agent at room temperature (RT sintering)” [21]. Thermal sintering is perhaps the most well defined process as it can be accomplished solely with an oven set at the appropriate temperature. For this work, sintering was done between 200°C and 250°C. However, a significant drawback of this method is the heat exposure to the substrate which the inks are on. Low temperature substrates, including many thermoplastics, are damaged when heated to ink sintering temperatures. The melting or deformation of the substrates can then be observed. As such, thermal sintering, despite being the most understood due to its simplicity, is not desirable due to substrate restrictions. Flexible substrates are often in the regime of heat sensitivity. The main alternative to thermal sintering investigated for this thesis work was photonic sintering/annealing.

Figure 2.14: A circuit board printed with silver ink by Christenson et. al. [29].
also known as intense pulsed light sintering (IPL). This process uses pulsed light from a xenon lamp to sinter the inks.

A type of ink commonly sintered with IPL technology is silver nanoparticle ink. Sintering experiments show the resistivity achieved with silver ink is good enough to be used in printed electronics [44] and can even be have lower resistivity than traditional oven-based thermal sintering with substrate specific temperature regulations [45]. For example in the low temperature substrate regime, some formulas of silver ink can be more effectively sintered, thus having lower resistivity, with IPL than with thermal sintering. In Figure 2.15 Kang et. al. show three SEM images of IPL exposed silver ink and thermally sintered silver ink [44]. As a metal is more effectively sintered, the grains become larger and the metal becomes denser resulting in lower resistivity. Motivation for cheaper materials than silver has led to research into the IPL sintering of copper nanoparticle ink [46, 47]. Kim et. al. showed that this process can achieve resistivity around three times that of bulk copper [46]. Ryu et. al. leveraged IPL to sinter copper while removing the oxide shells of the nanoparticles thus reducing resistivity [47]. Figure 2.16 shows the sinter of copper nanoparticles by Ryu et. al.

![Figure 2.15: This figure shows three SEM images of the surface of silver nanoink patterns. The image on the left shows two pulses of an IPL sinter, the middle shows 3 pulses of an IPL sinter, and the right shows a traditional thermal sinter. At the relatively high thermal sintering temperature of 200°C, it can be seen that the traditional process provides the best sinter among the three methods [44].]
One significant advantage this technique has over traditional methods is its drastic reduction in sintering time. While thermal sintering in an oven generally takes on the order of hours, photonic annealing sinters on the order of milliseconds. This radical reduction in sintering time expedites the rapid prototyping process especially as a multi-material system is developed. For the research conducted for this thesis, the oven sintering time is around 3 hours. Just using photonic annealing for the conductor layers reduces the oven cure time to 1 hour. It should be noted that the dielectric used in the research, polyimide, does not cure well with photonic annealing thus limiting the sintering time reduction to about an hour. This technique also allows for commercial off-the-shelf (COTS) component
integration early in the fabrication process without concern for package damage resulting from thermal exposure.

3 Ink Compatibility Analysis and Circuit Design

Initial research was focused on two major areas to investigate the viability of an aerosol jet printed circuit board, process compatibility and circuit selection/design changes. The general approach for these areas of research are summarized as follows:

A. Ink Compatibility Tests

A variety of conductor and dielectric inks were analyzed to determine which would were most compatible. After initial attempts failed to use Loctite 3104, an amber acrylic, with silver, a polyimide dielectric layer was settled on. SEM images were taken so that silver both above and below the dielectric could be analyzed. Another ink compatibility test was the reaction of the inks to conductive epoxy, specifically EPO-TEK® H20E Silver Epoxy. It is well known that many aerosol jet printed inks are incompatible with more traditional component attach methods, so it is important that conductive epoxy can work to simplify the component integration of this complex circuit.

B. Selection and design of circuit system for relevant emerging applications

A model board was then selected to print with the developed process. This also allowed the printed result to have a one-to-one comparison between it and the traditionally fabricated PCB board. Design alterations were done to the printed version of the board so that it was more printable (i.e. reduced footprint, less ink deposition) and so that only the necessary components for our tests were kept.

The following sections describe these two processes in more detail.
3.1 Ink Compatibility Analysis

A fundamental part of the design process for the use of aerosolized conductors and dielectrics in a PCB is their capabilities to operate with predictable outcomes. For a silver trace, the resistance of that trace should be in a regime which doesn’t require excessive voltage to overcome line loss or generate unnecessary heat on the board. For the dielectric, the material should provide little to no amperage leakage across an appropriate range of input voltages. Novacentrix silver flake ink [48] was tested and succeeded in providing a resistivity of approximately 5.83E-8 ohm·m (an average of 16 resistivities calculated) or roughly 4x that of bulk silver. Corin XLS [49], a polyimide ink from Nexolve, was determined to be a compatible dielectric with both the silver ink, the substrate, and the dielectric shielding it provided. Other tested dielectrics rendered the Novacentrix silver ink nonconductive when the silver ink was applied over the dielectric. Attempts to determine a breakdown voltage of the Corin XLS were unsuccessful, as the required input voltage to cause a breakdown could not easily be reached. A maximum of 20V were applied to the dielectric in the breakdown tests. Not even rapid ageing environments resulted in observable dielectric breakdown. Several other inks were considered for testing including Loctite 3104, a UV curable amber acrylic, and CNTRENE 3023 A7-R, a CNT ink made by Brewer Sciences. However, both inks had incompatibilities with the chosen printed circuit board rendering them ineffective. When in direct contact with silver, Loctite rendered the silver non-conductive for an undetermined reason. The CNT ink on the other hand was simply too resistive for application in the circuit board, necessitating very high currents for the board to function. Table 1 shows some of the ink formulations used in various work by Draper. This table was created by Abbie Spencer, an employee at Draper.
Table 3.1: This table shows several commercial ink formulations tested by Draper on various substrates with several curing methods. Note the CNT is the CNTRENE 3023 A7-R made by Brewer Sciences and UTDots is another ink manufacturer. This table was created by Abbie Spencer, a Draper Employee.

Another crucial component of ink compatibility is the ability of the ink to successfully deposit on conformal surfaces. This is crucial to the design as the buildup process results in uneven thicknesses across the module. This will also prove to be an important trait of the Optomec®, which is leveraged for the electrical attachment of one of the components.

On a silicon wafer, two test cases were printed so that SEM analysis could be done. In the first case, polyimide was printed followed by a line of silver on top of it. In the second case, the silver trace was printed then covered in polyimide. The goal of this experiment was to determine if any diffusion or erosion occurred between the silver and polyimide surfaces. Previously it had been observed that traces under polyimide exhibited a lower resistance than those above polyimide, however it was not determined whether that was simply print variation or some failure mechanism for the silver over the polyimide like thermal coefficient of expansion mismatch. The SEMs were thus used to ensure no visible
structural deformation was occurring to silver on top of polyimide. A silicon wafer was cleaved in order to make cross sections of the silver and polyimide prints. As can be observed in some of the subsequent pictures, the polyimide seemed to tear apart as opposed to the silver, which split cleanly.

Figure 3.1, Figure 3.2, and Figure 3.3 show a printed silver trace over printed polyimide. Figure 3.1 shows the full cross section of the trace. As can be seen from the pictures, the polyimide did not cleanly cleave with the silicon wafer. Also the silver distribution throughout the trace can be observed based on its thickness. As expected, the center of the trace is thickest as this is where the ink impacts the substrate. Figure 3.2 shows a zoomed in version of the same trace. Here the boundary between the polyimide and the silver can be observed. At this magnification, it appears there is no diffusion occurring between the silver and polyimide. Another interesting note is that the porosity of the silver can be observed at this magnification. A ripple in the polyimide on the left side is also observed. It is suspected that is this a product of the wafer cleaving process used to create the cross-section. Figure 3.3 shows a more magnified version of the inks where the flakes of silver ink can readily be observed. The porous nature of the sintered ink can be observed even more clearly than with the previous pictures. The boundary between the polyimide and the silver appears to be distinct, indicating no diffusion of one ink into the other.
Figure 3.1: An approximately 50 µm trace on top of printed polyimide. Overspray from the aerosol jet print can be seen to the right of the figure. The maximum height of the trace is where the center of ink contacts the substrate as expected.

Figure 3.2: The same trace as above is analyzed 5x closer. As can be seen the silver ink is porous in nature and the polyimide is not. A ripple in the polyimide on the left is observed where it delaminated from the silicon wafer.
Figure 3.3: A zoomed in picture of the silver on the polyimide is shown above. As can be observed, the silver is composed of flakes that are stuck together. The porosity between some of these flakes is readily observed. The polyimide looks similar to the previous two pictures. As can be seen, the boundary between the silver and the polyimide is clean and no diffusion from one to the other can be observed.

SEMs of silver traces under polyimide are shown in Figure 3.4 and Figure 3.5. In Figure 3.4, the polyimide on the right and left of the trace can be seen delaminating from the SiO$_2$. There also appears to be an airgap between the polyimide and the silver. This airgap is probably a result of the cleaving process which resulted in the polyimide tearing and a flap-like structure hanging down. Figure 3.5 shows a magnified image. As can be seen in, the silver on the left edge of the trace is being pulled up with the delaminating polyimide. This indicates that the adhesion of the silver to the polyimide is greater than the adhesion of the silver to SiO$_2$. The boundary between the silver and the polyimide is once again clean meaning no diffusion between the inks is visibly taking place.
Figure 3.4: Silver buried under a polyimide layer is shown above. The polyimide is shown clearly delaminating from the silicon wafer on the left and right edges of the picture due to the cleaving of the wafer.

Figure 3.5: A zoomed in version of the silver under the polyimide is shown in the SEM above. As can be seen, the silver on the left edge is being pulled up with the polyimide. This appears to indicate that the adhesion between the substrate and the silver is worse than that of the polyimide to the silver. The boundary between the silver and the polyimide is clean indicating no diffusion between the materials.

Figure 23 shows the how peeling polyimide effects the underlying silver. As can be seen in the SEM image, the entire trace is being pulled up with the polyimide. The silicon surface of the wafer is left clean. A crack has formed in the silver trace on the right side presumably form the stress induced on it
from bending. It is this image that demonstrates adhesion between the silver and polyimide inks should not be an issue. This may partially be due to the porous nature of the silver. When the polyimide coats the silver, the ink may seep into the pores on the surface of the silver so that when it cures it is strongly attached.

![Image of adhesion between silver and polyimide](image)

*Figure 3.6: This figure shows the adhesion the silver has to the polyimide layer. As the polyimide delaminates from the substrate, it pulls the silver with it. It is therefore with confidence we can state that there should be no issue adhesion issues between the silver and the polyimide.*

Another aspect of the ink’s compatibility with building a transceiver circuit is its ability to electrically connect to wires and COTs components. Testing was done to ensure that the conductor would not be consumed by the H20E conductive silver epoxy, and the electrical path would remain functional. In Figure 3.7, silver pads and a polyimide line were deposited and cured. Afterwards a conductive epoxy dot was put onto one of the pads and cured. As can be seen, there is not visual degradation of the silver pad, and electrically the pad to the epoxy dot is continuous. Figure 3.8 shows what happens when the conductive epoxy is cured on top of cured polyimide. As can be seen, the dielectric is consumed around the conductive epoxy. This could be problematic if the conductive epoxy overflows the printed pads for the transceiver circuit. In such a case, a short to the ground layer would
most likely occur. Therefore, the integration of the COTs components must be done carefully and with minimal conductive epoxy.

Figure 3.7: Printed silver pads and a printed polyimide trace are shown. As can be seen, a conductive epoxy dot is on the upper silver pad. This test shows that the placement and curing of conductive epoxy on top of cured silver does not destroy the silver.

Figure 3.8: A dielectric line with a conductive epoxy dot placed on it is shown. As can be seen, at the boundary between the two, a gap has formed between the dielectric and the epoxy where the dielectric was either chemically or physically destroyed. Electrical testing has shown that this phenomena results in a short to the conductor the dielectric is shielding.
3.2 Semiconductor PCB

The ideal candidate circuit was a general purpose “system on chip” (SOC) integration platform that could be used in applications such as a biosensor, a high-end processor, Bluetooth communications, and for “internet of things” applications. The Nordic Semiconductor nRF51822 Multiprotocol Bluetooth low energy/2.4 GHz RF SOC chipset fulfills these requirements, while its commercially available off-the-shelf (COTS) demonstration board (nRF51 Development Kit board (PCA10028)) is an ideal candidate to compare “standard” PCB integration with the printed approach. The board has many features that leverage its data collection and communication features allowing its application scope to be broad. For example it is reprogrammable, has both active and passive components, has an appropriately sized footprint for printing, and uses a variety of easily obtained commercial components. Figure 3.9 shows the full commercial board along with the red region which is being replicated in the AJP circuit. Unnecessarily peripherals are being stripped out of the design so that the focus is only on interconnection to the chip, power and wireless communication. An alternative for a 1:1 comparison was to design a laminate PCB, however this is more difficult and a direct COTS comparison provides a more valid benchmark.
The original layout for the approximately 34 mm x 34 mm board is shown in Figure 3.10 and Figure 3.11. This file is virtually the same as provided by Nordic Semiconductor, with the exception of small tweaks to the ground layer. As can be seen in Figure 3.10, the yellow and green hashed area denotes the ground plane along with some routing traces printed along with the ground plane. The purple hashed area marks the dielectric layer with circles denoting exclusion of dielectric. These circles are the vias between the upper routing layer and the ground plane. The vias are difficult to see as they are all filled in by the upper routing layer, blue hashed lines. Vias are located where blue circles appear to dead end in the drawing. As can be observed by the black text, the QFN48 package is centered in the layout schematic. Many of its 48 pads are used to integrate the circuit with the microprocessor. The three crosses within circles are all fiducials for alignment and serve no electrical function in the schematic. Above the QFN48 package are the LEDs, two crystal oscillators and their corresponding...
components. Below the QFN48 are switches, and the programming lines for the microprocessor. The switches are removed in further design iterations. On the left of the QFN48 is the RF matching circuitry along with the antenna for Bluetooth communication. A voltage divider is on the right side of the QFN48 package. Figure 3.11 offers a close-up of the immediate vicinity of the QFN48 package. The red box outlines the RF matching circuit. Both crystal oscillators can be seen on the top of this figure, denoted as X1 and X2.

Figure 3.10: The initial .def design for the transceiver circuit. This design is a portion of the PCB directly from the Nordic Semiconductor nRF51822 Multiprotocol Bluetooth low energy/2.4 GHz RF commercial demo board. The yellow outlines the ground plane, the purple outlines the dielectric, and the cyan shows the upper layer silver routing. The placement of the QFN48 package for the microprocessor is in the center of the figure surrounded by pads.
3.3 Design Iterations

Design modifications to the board were made to primarily enhance printability and leverage the selective deposition capabilities of this 3D printing tool. For a PCB to be aerosol jet printed, a primary challenge is component integration. It was determined that the most efficient demonstrator for this research would involve integrating COTS with both printed interconnect and assembly techniques. Two other component integration methods were discussed: printing just interconnect and using standard assembly, or printing active devices. Printing just interconnects and using standard assembly is not an ideal process due to the assembly step required after printing. Another added difficulty of this method is that the Novacentrix silver ink cannot be soldered to as the solder consumes the silver ink. Printing
active devices is actively being pursued by other researchers, however, leveraging silicon devices is most attractive for near-term adoption of printed electronics integration.

Therefore, non-traditional component integration methods were explored. One method was the mounting of a component upside down then printing traces up the sidewall and onto the pads as shown in Figure 3.12. This method was remarkably successful for the QFN48 package. This same package will be used in the proposed printed circuit board. However, early tests indicated that significant variation in line resistance can occur. The source of this resistance appeared to be from the concave corner the trace traverses and the bottom of the component. In the area, a small air gap between the component and the substrate resulting from the gluing process can be observed. This issue was solved by using the adhesive that secures the component to the substrate to smooth out this corner from 90 degrees to a softer angle while filling in any airgaps. Figure 3.12 shows the QFN48 package implemented upside down with routing traces on top. As can be seen, sidewall traces are used to integrate the microprocessor with the rest of the circuit. The adhesive used to adhere the chip to the substrate also makes a filet for the printed silver to go up the sidewall.
3.3.1 General Circuitry Design Changes

In order to accommodate the placement of the microprocessor in the QFN48 package upside down, the whole artwork of the PCB was mirrored so that components could be selectively put upside down. This mirroring is already shown in Figure 3.10 and Figure 3.11. Since all components, except for one, have only two pads, the mirroring would not affect their ability to be implemented as is in the circuit. For the four-pad crystal oscillator, its pad functionality is symmetric so it can be placed right side up with the package pads corresponding properly to the circuit pads. Once again, the primary advantage of this process is that it integrates the components with aerosol jet printing technology. However, flipping the chip also warrants the placement of traces on top of the package for reasons later described.
in “Manufacturing Procedure.” By using the process developed for dielectric and conductor deposition, this routing was easily done.

Another major series of changes to the design layout involved the reduction of the footprint of the ground layer. Since the whole circuit was being printed with AJP technology, the ground plane needed to be small enough to be printed rapidly so that the printing nozzle wouldn’t clog. The ground plane was thus reshaped various times until the printing time was down to around 30 min. The ground plane was always printed in at least 2 layers in order to provide a thicker and more uniform layer.

Changes to the dielectric layer were also made to leverage the selective deposition capabilities of the tool. The dielectric layer was edited so that it was only put in areas where it was needed. Therefore, only areas where the upper layer lines crossed over the ground plane were covered in dielectric. Vias were formed through the exclusion of dielectric. This is a fundamental change in the layout and fabrication compared to traditional PCB/microelectronics methods. This method prints dielectric only where adjacent layers need electrical insulation rather than cutting holes into the dielectric layer for electrical connections. One of the early versions of the board is shown in Figure 3.13 and Figure 3.14.
Figure 3.13: An early iteration of the fully printed transceiver circuit is shown above. Only the QFN48 was integrated with AJP technology while the rest of the COTs components were placed by hand with conductive epoxy.

Figure 3.14: An early integration of the fully printed transceiver circuit is viewed from an angle. This allows for the sidewall integration lines of the QFN48 package to be observed.

One of the major goals in many of the redesigns was the reduction of potential shorts. By removing the ground plane in many areas with components, shorting was greatly reduced due to the
tendency of the applied conductive epoxy to rip through the dielectric if it spilled over the silver pad.

More unnecessary components for our tests were also removed, specifically the switches at the bottom of the layout. By reducing the components, the chances of a short happening were reduced. The resistors by the LEDs were also moved in order to reduce the number of components over the dielectric and ground plane. The layout of the final design is shown in Figure 3.15. The shaded regions in the figure indicate material deposition sites. As can be noticed, the RF matching network and antenna design have changed significantly. The discussion of changes in the RF design are in the subsequent section RF changes.

Figure 3.15: The final layout of the transceiver circuit is shown. As can be seen, changes to the ground, dielectric and upper silver layers were made in order to more effectively print the circuit. Major changes were made to the RF circuitry so that it could function on this printed board.
3.3.2 RF changes

One of the area’s most subject to significant changes in design and components was the RF
matching network and antenna. Since the matching network and antenna were originally designed to
work with a dielectric layer over 10x thicker than the AJP dielectric layer, significant issues were
encountered. The thinness of the dielectric that was printed resulted in the shorting of the RF network
to the ground plane. This shorting effectively rendered the Bluetooth capabilities of the chip useless.
Therefore the matching network and the antenna had to be completely redesigned with the expectation
the dielectric thickness was 10 µm. The output of the antenna is very sensitive to the dielectric thickness
in this regime, raising concerns of making a uniform thickness dielectric layer.

One of the primary changes of the matching network was the switching of capacitors and
inductors and the shrinking of their footprint. The Nordic Semiconductor PCB uses a 0402 footprint for
its components while the final design for the matching network uses a 0201 footprint. The idea here is
to reduce the area the matching network is operating in order to reduce line loss and also to reduce the
risk of failure. The downside of shrinking the footprint is the increased requirement for technical skill in
component placement. Since a technician hand placed all the components, the smaller components
became more difficult to place accurately. Therefore spilling of the conductive epoxy over the pad and
onto the dielectric occurred more frequently. This is a situation that needs to be avoided due to the
conductive epoxy ripping apart the dielectric and shorting to the ground plane upon curing. This
occurrence highlights the fragility of many aerosol jet printed inks, especially concerning adhesion.

Similarly, the antenna needed to be redesigned so that it too didn’t short to the ground plane
when powered. The design of the antenna was changed to a planar inverted F antenna (PIFA) antenna
since the distance to the ground plane is regulated laterally rather than through the dielectric. This
allows for a much higher degree of precision than with the thickness of the dielectric deposition. This is
largely because the x and y planes of an aerosol jet print are much easier to control than the trace thickness. The final matching network design is shown in Figure 3.16 and Figure 3.17.

Figure 3.16: The matching network on the left of the QFN48 package along with the PIFA antenna is shown above. As can be seen, the antenna and matching network design was radically changed from the initial layout.
Advanced Design System software (ADS) was used in the design of the matching network. Much of this work was done by Jonathon O’Brien, an employee at Draper Laboratory. As changes to the matching network and the antenna were made, retuning of the network were required to ensure its functionality at 2.4 GHz. Therefore the capacitance and inductance of many of the components changed each design iteration. Figure 3.18 and Figure 3.19 show plots final matching network design. Figure 3.18 shows the Smith Chart for frequencies from 1 GHz to 3 GHz. This plot is of the amount of power transferred into the network also known as the reflection coefficient. As can be seen in the plot below of frequency vs reflection strength, at 2.4 GHz, there is approximately -15 dB. This indicates a strong signal.
over Bluetooth frequencies. Figure 3.19 shows the Smith Chart at the other port of the network. This is the port that comes from the microprocessor. The impedance calculated is the impedance at the beginning of the matching network.

Figure 3.18: Shown above is the Smith chart for the final design of the matching network and the dB strength of the signal over those frequencies. Specifically it shows the amount of power transferred into the network, also known as the reflection coefficient. As can be seen, the strength of a 2.4 GHz signal (Bluetooth) is -15 dB.
Figure 3.19: Above is the smith chart for the port by the microprocessor. The plot shows the reflection coefficient along with the impedance out of the microprocessor.

Since the goal of this thesis is not RF design, more details on the redesign of this portion of the circuit are not included. The author was significantly assisted by Jonathon O’Brien, a Draper employee, for this portion of the research.

4 Manufacturing Procedure of Transceiver Circuit

The following chapter describes the methods to fabricating the transceiver circuit. This process has been subdivided into five main steps as shown in the chapter’s subsections. The manufacturing process takes a total of approximately 10-12 hours, a drastic reduction in PCB manufacture time compared to traditional methods. Most fabrication attempts were done on a silicon wafer with a 1 µm layer of SiO₂. However, initial building has been done on other substrates such as bare silicon and Kapton. The flexibility of the subsequently detailed process allows it to be applied to a variety of substrates, both
rigid and flexible. Small adaptations to the process can be made for low temperature substrates, such as the substitution of thermal sintering with photonic annealing. This reduces the temperature exposure the substrate sees while still sintering the ink. Such techniques are being researched, however they are not included in detail in this thesis.

4.1 Mounting of QFN48 and Integration

As previously mentioned, a significant shortcoming of many current aerosol jet inks is that they do not survive common COTs attachment methods. Use of solder or other traditional methods result in ink failure through its consumption or destruction of the printed ink. Conductive epoxy has been shown to work with many of the aerosol printed inks. However, with a complicated circuit like the transceiver circuit, hand placement of epoxy followed by component placement is tedious and difficult. For the QFN48 package, its density of pads on each of its four sides add additional complexity when attaching it to the circuit. The challenge of pad alignment to the printed circuit after the placement of the epoxy dots was shown to be very difficult. As such, a redesign of was done which necessitated the placement of the QFN48 package upside down first, then subsequently building up the rest of the circuit around it. Then the QFN48 surface itself can be used for the routing that previously went under the package. This process, including adhesive cure time at 100°C, takes approximately an hour.

Armstrong C-7/W epoxy (C-7) was not only used to attach the microprocessor to the substrate, but also to create a fillet on the interior edge the QFN48 package makes with the substrate. This eliminates the airgap between the package and the substrate which can prove difficult to bridge with conductive inks. A primary challenge of this adhesive application is minimizing the amount used to secure the package to the substrate and to create the fillet. Too much glue can result in cracking, opening any connection lines that go up the sidewall. This is potentially from the coefficient of thermal expansions difference encountered in a heterogeneous material system. It is important to note that when done properly, no visible glue cracking occurs. Figure 4.1 and Figure 4.2 shows the QFN48 package
directly after the gluing process. As can be seen in Figure 4.1, the glue spreads out a little from under the package helping to make the fillet of the concave corner. Figure 4.2 shows this fillet along with the sidewall of the QFN48 package. As can be seen, the C-7 spreads along the sidewall.

Figure 4.1: An overview of the QFN48 package after the attachment to the SiO₂ wafer with C-7 is shown. As can be seen, the glue spreads out slightly around the package helping to form the fillet of the concave corner. This not only helps the ink climb the sidewall, it eliminates airgaps which can break the sidewall traces.

Figure 4.2: A side view of the QFN48 package after it has been adhered to the SiO₂ wafer is shown. As can be seen, the C-7 makes a ram up a portion of the sidewall and covers any airgap between the QFN48 and the substrate.
Another benefit of placement of the QFN48 first is that the sidewall lines are printed early in the process. These lines, which integrate the upside down QFN48 pads with the circuit have been shown to be the most prone to failure. By printing them early in the process, success or failure can be determined without necessitating the printing of the whole circuit. Common failure modes of these lines are shorting by ink spreading and cracking of the underlying C-7 adhesive.

The integration lines are printed with the aerosol jet print head at a 45° angle using NovaCentrix HPS-030AE1 Silver Flake Ink. This allows all parts of the sidewall to be covered. However, several geometric challenges arise with print head rotation. Primarily, vertical offset between the alignment camera and the deposition camera effects the printing area. Also the distance of the sidewall trace must be calculated so that it is long enough to reach the connection lines of the upper layer of silver but not too long to cause shorts. Both of these problems can be effectively solved with straightforward geometric analysis. The fillet of the corner also assists in the prevention of ink spreading at the interior corner of the package and substrate. Due to the 200 µm pitch of the pads, ink spreading can easily cause shorts.

All sidewall lines were printed with five passes of Novacentrix Silver Ink using a 150 or 200 µm nozzle with print width between 20-50 µm. Five passes were used in order to thicken up the trace and reduce the resistance. The variability is a direct result of what nozzles were functional at the time of the print. The workpiece was manually rotated for each sidewall to be printed on. The platen was set to 40°C in order to more quickly dry out the ink before the next pass. This helped reduce the spreading of the ink after it had been deposited. This printing process takes about 30 minutes.

The incorporation of the sidewall print early on also allowed for corrections to be made in the event of printing failure. If a print shorted or overspray ruined the traces, a foam swab soaked with isopropyl alcohol could be used to completely remove the deposited ink and start the print over. This
flexibility saves time from needing to put more QFN48 packages on substrates. Figure 4.3 and Figure 4.4 shows the sidewall traces for microprocessor circuit integration.

Figure 4.3: An overhead view of the QFN48 package, with the epoxy fillet, and the printed sidewall traces going down the exterior of the package.

Figure 4.4: A side view of the QFN48 package integration lines. As can be see, they ramp up the epoxy onto the package sidewall.
SEMs of conductive traces up the QFN48 package are shown in Figure 4.5, Figure 4.6 and Figure 4.7. These images were taken during testing of the sidewall integration process. They depict integration lines and pads completing a daisy chain QFN48 module so that resistance of many sidewall traces and continuity across all of them could be determined. These images are included since they depict the epoxy filet and the integration line print that is mimicked in this research. In Figure 4.5 and Figure 4.6, the C-7 epoxy used to adhere the package to the substrate and to create the fillet for the sidewall print can be clearly observed. Bubbles seem to have formed in between the traces, not effecting them. As can be seen, when done properly, the traces are continuous and easily climb the sidewall. The pattern in the SEMs is not the pattern used for the sidewall lines, which can be seen in Figure 4.4. Figure 4.7 shows an example without the C-7 fillet. Faint cracks at the base of the sidewall can be observed along with non-uniform deposition at that interior corner.

*Figure 4.5: An SEM image of conductive traces up the sidewall of a QFN48 package is shown above. Bubbles seem to have formed between the traces, without effecting the traces themselves. The lines are clearly continuous optically, and are continuous electrically.*
Figure 4.6: Another SEM image of the sidewall traces is shown. No bubbles appear on this side of the QFN48 package. The traces going up the epoxy fillet can clearly be seen.

Figure 4.7: An SEM of a QFN48 package without an epoxy fillet is shown. Faint cracks in the conductive traces can be observed at the base of the package. Also non-uniform distribution of the ink occurs at that concave corner.
4.2 Printing of Ground Plane

The ground plane is printed immediately after the sidewall lines on the QFN48 package. This layer is printed from NovaCentrix HPS-030AE1 Silver Flake Ink. This is done without sintering of the sidewall lines to reduce heat exposure to the QFN48 package. The CAD is designed for each line of the rastering of the area to be 55 µm apart. The width of the line coming out of the AJP system ranged approximately between 80-100 µm. This ensured that between 30-50% of the trace overlapped with its neighboring traces. Two passes were done in order to build up thickness of the ground plane and reduce resistance. Another benefit of multiple passes is it covers up any anomalous defects that occurred during printing during the first pass. Since the print is over a large area and takes over half an hour, there is a higher probability of a non-catastrophic printing error to occur. A non-catastrophic printing error qualifies as one where the volumetric output of the nozzle changes significantly for a brief period of time. The platen was set to 40°C to help dry the ink in between passes. The printing takes approximately one hour for two passes.

After the ground plane is printed, the wafer is put into a 200°C or 150°C vacuum oven and sintered for one or three hours respectively. 200°C at one hour was chosen with the desire of a well sintered ink while limiting package heat exposure. However, cracks would sometimes form in the sidewall lines on the QFN48 package potentially from coefficient of thermal expansion (CTE) mismatch between the glue and the silver. Therefore, another iteration was done at 150°C which resulted in drastically fewer cracks in the sidewall integration lines. Alternative sintering methods such as photonic annealing are actively being investigated. For the sintering of the ground layer, photonic annealing was a very effective sintering method. However, for non-planar traces such as the sidewall traces, photonic annealing was not as effective. Thus the incorporation of photonic annealing is still being worked on.

Figure 4.8 shows the transceiver circuit after printing of the ground layer and the sintering of the silver ink. The “F” of the left side of the structure is the PIFA. Routing lines to LEDs can be observed at
the top of the picture. The three fiducials, in the shape of crosses, used for the rest of the layers can also be observed. Sidewall lines can be seen coming off the top of the QFN48 package. Most of these lines remain unconnected and will be connected during the printing of the top silver layer.

![Figure 4.8: The transceiver circuit after the printing of the ground layer and the sintering of the silver ink is shown. The “F” on the left side of the pictures is the PIFA. Sidewall lines can be seen coming off the top of the QFN48 package, however at this stage most remain unconnected.](image)

### 4.3 Printing of Dielectric layer

The dielectric layer is printed in patches, in stark contrast to traditional spin-on dielectric methods. Dielectric is only dispensed in areas of need. For most areas, as long as the dielectric provides electrical insulation, its thickness doesn’t matter. For the majority of the design, the dielectric was built up with three passes of NeXolve Corin XLS Polyimide. The CAD raster is designed with 120 µm of spacing between traces. The output of the AJP system was ensured to be between 170-200 µm so that there would be 30-40% overlap between the traces. The platen the substrate rested on was set to 40°C to help dry out the polyimide between printing passes.
However for the RF circuitry, the thickness is of critical importance. The design of the matching circuit was done with the assumption the dielectric was a uniform 10 µm thick. A quick sensitivity analysis in ADS showed that if the dielectric was 7 µm, the antenna reflection coefficient would be around 0 dB, therefore unreadable. Several attempts were made to obtain the flattest possible structure with the polyimide. The RF dielectric section was printed with a serpentine pattern in an attempt to reduce pooling of the dielectric in the middle of the structure. The passes to build up the RF polyimide layer were also spaced out in an attempt to let the solvent dry from the polyimide and reduce the mobility of the polyimide induced by the air and ink coming out of the printing nozzle. After some testing, 7 passes were determined to get the dielectric thickness into the ballpark of 10 µm.

Profilometry measurements showing the profile of the RF polyimide from two different prints are shown in Figure 4.9 and Figure 4.10. As can be observed, the goal of a uniform dielectric layer is very difficult to achieve. Getting it planar at a specified thickness is near impossible. In Figure 4.9, between the left and the right marker, the average height is 12.625 µm over a width of 2.44 mm. As can be seen in the figure, throughout this distance, the height of the polyimide layer is increasing. In Figure 4.10, the polyimide layer has undulations in it. The average height of the layer is 6.97 µm over a 3.8 mm distance. Both polyimide RF layers were made with 7 print passes. In order to estimate the height the silver contributes to the RF polyimide profilometry reading, the profilometry of the antenna, which does not have polyimide, was taken. As can be seen in Figure 4.11, the silver thickness is approximately 4 µm. The variability between the thicknesses of the polyimide layers points to a shortcoming with AJP technology, especially with respect to this ink formulation. The nature of the AJP process does not lend itself to uniform layer deposition, especially with this particular ink. Therefore, RF designs should be made to reduce the sensitivity of the dielectric thickness.
Figure 4.9: A profilometry measurement of the RF polyimide and the silver underneath it. As can be seen, the height of the polyimide is increasing across almost 4 mm and never seems to plateau. The average height between the left and the right marker is 12.625 µm over a width of 2.44 mm.

Figure 4.10: A profilometry measurement of another print of RF polyimide over the silver ground plane is shown. As can be seen, the height of the polyimide undulates and is never consistent. Between the left and right marker the average height is 6.97 µm over a distance of 3.9 mm. This figure and the previous figure highlight the challenges of uniform layer deposition using AJP, with Nexolve Polyimide ink.
Figure 4.11: A profilometry measurement of the silver antenna, which has no polyimide, is shown above. As can be seen, the height is fairly consistent. Between the left and right markers, the average height is 3.98 µm.

Figure 4.12 shows the transceiver circuit after the printing and curing of the dielectric layer. The printing of the whole dielectric layer takes about 30 minutes. The curing of the polyimide is either done at 150°C for two hours or 200°C for one hour. For the modules where max exposure temperature was attempted to be minimized for CTE reasons, the first cure was used. As can be seen, only patches of dielectric were printed corresponding to areas where a routing layer of silver will be printed. Some of the areas of thicker dielectric appear to have burned during curing, however, this doesn’t appear to have an effect on its electrical insulation properties. Dielectric can also be seen on top of the QFN48 package. This dielectric was dispensed so that routing could be placed on top of the QFN48 package. This was done in order to compensate for the loss of routing below the package since the package was placed before any traces were printed. Figure 4.13 shows the formation of a via hole through the exclusion of dielectric deposition. As can be seen by the location of the hole in the dielectric, there was a slight misalignment during this print, on the order of 50 µm. This margin of error is acceptable for this design.
Figure 4.12: The transceiver circuit after the printing and curing of the polyimide layer is shown above. As can be seen, dielectric was only printed where it was needed. Areas of thick dielectric were prone to burning during curing. This has no noticeable impact on its performance as an electric insulator. Polyimide traces on top of the QFN48 package can be observed. Routing traces will be printed on top of it in the subsequent layer.

Figure 4.13: The via formed through the exclusion of dielectric is shown above. As can be seen, the dielectric layer was misaligned by about 50 µm during this print. This margin of error should be acceptable for the design.
4.4 Printing of Upper Conducting Layer

The upper conducting layer was printed with NovaCentrix HPS-030AE1 Silver Flake Ink. The layer, except for the RF circuitry, was printed at one time. The RF circuitry was printed separately so that more control could be exerted over the printing in that area through slowing down of the print speed. This is necessary due to the small feature sizes of the circuit in this area. While the rest of the layer is based on components with a 0402 footprint (imperial units) or larger, the RF portion of the circuit uses components with footprints of 0201. Printing the whole layer at the speed of the RF portion isn’t feasible since it would substantially increase the print time and the risk of clogging the print head or virtual compactor.

This layer integrates the majority of the QFN48 package and provides all the pads and traces for component placement to the circuit. Some routing is done on top of the QFN48 package to accommodate pad connection that were designed to go under the package. The printing of this layer takes approximately 1 hour. The sintering is done at 200˚C or 150˚C in a vacuum oven for one or three hours respectively. The decision between the two sinter times is chosen as outlined in previous sections.

Figure 4.14 shows the transceiver circuit after the printing of the top silver layer. As can be seen, all the pads for the components are now printed and ready for component placement. The unpopulated RF matching network can be seen on the left side of the QFN48 package in a red box. Routing on top of the QFN48 package can also be observed. This routing ensures that several pads all have Vcc, voltage high, going into them. This is required for the microprocessor in this circuit configuration. Six breakout pads for direct connection are shown in the bottom right of the figure. This is for wired programming and powering of the transceiver circuit.
Figure 4.14: The figure above shows the transceiver circuit after the printing of the top conducting layer. As can be seen, routing is done on the package of the QFN48, along with an attachment of the package ground to the circuit ground. The pads and traces for the RF matching network can be seen on the left of the chip, connecting to the antenna. Breakout pads for wired programming and power are on the bottom right of the module.

Figure 4.15 and Figure 4.16 show magnified shots of two locations with three layers of material: ground silver, polyimide dielectric, and upper silver. Figure 4.15 shows ground traces going to a crystal oscillator, and routing traces going between the LEDs and the microprocessor. Figure 4.16 shows the filling of a “via” to make a connection from the top layer through the ground layer. This figure is in the same location as Figure 4.13, after the upper silver layer print. As can be seen, the alignment issue of approximately 50 µm did not result in any visible shorts or breaks in the lines. The circuit was designed to handle alignment issues of this magnitude. Overspray can be observed on the polyimide from the printing of the silver. The overspray is too sparse to create an electrical connection and thus a short. Therefore this level of overspray is relatively harmless in the printing of the circuit.
Figure 4.15: One of the areas with polyimide dielectric separating a ground line and routing lines is shown. This is one of several locations where the silver and polyimide make a multilayer stack.

Figure 4.16: Three layers of material can be observed above. This image is of the same location as Figure 4.13 but now has the upper layer of silver printed on it too. As can be seen, the slight misalignment doesn’t result in any shorts in this area nor does it result in any open lines.
4.5 Placement of COTs and wires

The COTs components, consisting of capacitors, inductors, resistors and oscillators, were hand placed. Since only a few boards are being made, the time it would take to integrate equipment into the process such as a pick-and-place tool would be greater and cost more than the time and money it would save for this demonstration. A key component of the transceiver circuit success is the population of the board with conductive epoxy and components before the conductive epoxy cures. Several methods have been discussed for the application of conductive epoxy. Using a screen and a squeegee was the first idea, however, the small pad size (0.5mm x 0.5mm) would necessitate a small screen which wouldn’t allow the epoxy to go through. Therefore, hand placement of the conductive epoxy was determined to be the most convenient. As such a conductive epoxy dot and a component were placed sequentially for each location by a technician. The conductive epoxy used was EPO-TEK® H20E, a two-part epoxy. Refinement of the process is possible after this proof-of-concept work.

Wires were also connected to the breakout pads through conductive epoxy. These wires allow the microprocessor to be programmed through a hardwired connection. The powering of the circuit is also a capability achieved through these wires. The population of the circuit board takes at least 3 hours. The conductive epoxy was cured for 30 minutes at 100˚C several times during the placement process. This was done to aid in the placement of many close components thus reducing the chances of bumping a loose component and spreading epoxy across the circuit surface.

Figure 4.17 shows the transceiver circuit after the placement of the components and the attachment of wires. The wires are for powering and for programming the microprocessor. As can be seen in the image, a multi-material and a multi-layer structure was completely printed and COTs components were integrated. Figure 4.18 and Figure 4.19 show isometric views of the completed transceiver circuit.
Figure 4.17: The final transceiver circuit is shown in this figure. This image shows three layers of material, COTS components, breakout wires for programming and powering of the microprocessor, and integration lines for the QFN48 package.

Figure 4.18: An isometric view of the whole transceiver circuit.
Figure 4.19: An isometric view of the transceiver circuit focused on the QFN48 packaged and the sidewall integration lines is shown.

Figure 4.20-Figure 4.24 show magnified images of portions of the transceiver circuit. Figure 4.20 shows the QFN48 package and the sidewall connections that integrate it into the rest of the circuit. Several small epoxy dots can be seen on the sidewall connection lines which bridge cracks that potentially resulted from TCE mismatches. Routing on top of the package can be seen upon careful observation. Figure 4.21 shows the LEDs at the top of the transceiver circuit and their associated resistors. Figure 4.22 shows the two crystal oscillators, one in a large square package the other in a large rectangle package, and the associated capacitors. Figure 4.23 shows the voltage divider to the right of the QFN48 package. Figure 4.24 shows the RF network and the beginning of the antenna. The RF network contains the smallest components, with a package size of 0201 (metric). The network also has three inductors along with capacitors to form the network.
Figure 4.20: A magnified picture of the QFN48 module and its interconnections to the routing layer are shown. Small dots of epoxy can be observed on some of the sidewall interconnections where cracks formed during sintering.

Figure 4.21: A magnified picture of the LEDs on the top of the transceiver circuit is shown above.
Figure 4.22: A magnified version of the crystal oscillators and their corresponding capacitors is shown. The oscillators are the two components in the image that do not have a 0402 footprint.

Figure 4.23: A magnified picture of the right side of the QFN48.
Figure 4.24: A magnified image of the RF network and the beginning of the PIFA antenna.

5 Results and Data Analysis of Printed Transceiver Circuit and of a MEMS Acoustic Sensor Packaging Application

The results section is split up into two subsections, Transceiver Circuit Results and MEMS Microphone Array Packaging Application. Transceiver Circuit Results is a section covering the results and data analysis from the circuit discussed throughout this thesis. It is a direct consequence of the manufacturing methods discussed in “Manufacturing Procedure of Transceiver Circuit”. However, since this thesis is based on heterogeneous material systems, the applications of AJP technology to another packaging problem is investigated in the section “MEMS Microphone Array Packaging Application”. This research is based on leveraging the capabilities of AJP technology to improve the packaging and potentially the functionality of a previously designed MEMS microphone array.
5.1 Transceiver Circuit Results

Originally, the transceiver board was going to be analyzed to see how it stacks up against the traditionally fabricated board. Metrics such as voltage required to power, success of the programmed SOC firmware to communicate over Bluetooth, the RF transmission power, and the ability to transmit signals from the SOC such as data from the onboard temperature sensor were planned to be used in this evaluation. However, due to the lack of success in getting the RF circuitry to work, the testing goals have changed. Metrics measuring the success of the transceiver circuit have been determined to be resistivity of routing traces, power requirements for programming and operation, time to manufacture, and reproducibility. The programming of the microprocessor was also changed from one that relied on the RF circuitry to one that programmed an LED light sequence. This was then used to show the programmability of the sensor and the functionality of a majority of the circuit. The conclusion of this analysis is that printing a board through means such as the aerosol jet process is a robust, ability-expanding, and beneficial to the innovation process, despite more wrinkles that need to be figured out.

5.1.1 Resistivity Analysis of Multilayer Board

As previously mentioned, one metric to measure the electrical performance of the board is resistivity of the routing traces. The resistance was taken from the base of the QFN48 package to another significant feature in the line, either a via or a breakout pad. Profilometry measurements were taken in order to get cross sectional area. The two programming lines for the microprocessor were chosen as the representative traces for resistivity data. It is important to note that since the routing silver is on top of polyimide, the leveling zones used are not very flat. Figure 5.1 shows one of the profilometry measurements.
Figure 5.1: A profilometry measurement of one of the programming lines is shown above. The average height between the left and right markers is 2.32 µm over a width of approximately 0.2 mm.

The resistivity was calculated using equation (1):

\[
\rho = R \frac{A}{l}
\]  

(1)

where \( R \) is resistance of the trace, \( A \) is the cross sectional area, \( l \) is the traces length and \( \rho \) is resistivity.

Two modules were tested, one module was successfully programmed and the other wasn’t not due to a short. This short was determined to not have an effect on the resistance measurement of the trace. The two modules also differ in their sintering temperatures, with one being sintered at 200°C and the other at 150°C respectively.

The module sintered at 200°C has a resistivity of 7.81x10⁻⁸ Ω·m for the right programming line and 6.19x10⁻⁸ Ω·m for the left. The module sintered at 150°C has a resistivity of 8.93x10⁻⁸ Ω·m for the right and 4.88x10⁻⁸ Ω·m for the left programming line. These resistivities are all 3-6x the bulk resistivity of silver. If the somewhat liberal assumption that the sidewall integration lines have the same profile as the routing traces is made, an estimate for the total resistivity of the traces to the top of the QFN48 package can be made. An exact profile cannot be measured since the sidewall lines are on the side of the package. Therefore, the estimate of their profile is the best that can be done with the available tools. The total resistivity of the 200°C module is 1.01x10⁻⁷ Ω·m for the right and 6.40x10⁻⁸ Ω·m for the
left trace. The total resistivity of the 150°C module is $1.06 \times 10^7 \Omega \cdot m$ for the right and $5.4 \times 10^8 \Omega \cdot m$ for the left trace. The variation observed in these resistivities is approximately 3-7x that of bulk silver.

The traditionally manufactured PCB is made with copper traces, having a resistivity of $1.68 \times 10^8 \Omega \cdot m$. Therefore the silver printed traces have approximately 3-7x higher resistivity than the standard 1 mil thick PCB trace. The acceptability of this difference is largely application dependent. Assuming the same trace profilometry, 3-7x higher resistivity results in 3-7x higher current needed to power the device at the same voltage. This module was designed to be powered at 3.1V.

5.1.2 Manufacturing Time and Reproducibility

A major goal of this research was to reduce the design and fabrication time of prototype PCBs. As mentioned in the introduction, the design and fabrication cycle of PCBs can take from weeks to months. After the preliminary design was made, design iterations were made rapidly. Significant changes to the design, including machine code generation, took no more than an hour to do and create the machine code. The fabrication time was reduced to 10 hours and there is potential to reduce it by approximately 4 more hours. These 4 hours would be gained back by changing the sintering method of the silver to photonic annealing and switching to an automated method for population of the circuit board.

Not only was the manufacturing of the board significantly faster than the traditional method, it was also easy to account for printing mistakes early in the process. Aerosol jet printing technology can have variable output and sudden nozzle clogging which can ruin a print. However, with IPA and a foam swab, many errors can be hand erased, saving time from redoing the whole circuit.

The reproducibility of the board is an area which needs some improvement. Shorting was a major failure mechanism of these circuits. This is most likely due to the fragility of the polyimide ink as a dielectric and its variation in output over a print. When exposed to the H20E conductive epoxy, the polyimide ink seemed to tear, resulting in a short to the ground layer. Therefore, careful application of
the conductive epoxy was needed to ensure it did not flow over the printed pads and onto the dielectric. Also focus on the print must be maintained in order to make real time adjustments to ensure the appropriate material output.

Other reproducibility issues centered around trace width for the dielectric and routing layer. During a long print, the width of the traces would grow, especially for the dielectric. On the dielectric layer, this resulted in smaller “via holes” for connections to ground. On the routing layer this resulted in traces that were closer together than they should be. For the RF portion of this circuit it was a particular concern since a short can result from traces too close to one another. Whenever a visible short happened during the printing of a layer, attempts were made at scratching between the traces to establish electrical insulation. Of all the modules printed, including partial prints, approximately 10% experienced an issue directly related to erratic ink deposition. However, almost all these issues were fixable by hand.

Lastly, reproducibility was effected by the manual epoxying method of the QFN48. The amount of glue and the placement of the component on top to ensure the creation of the fillet was an inexact process. This rendered about 10% of the QFN48 modules glued onto wafers not useable from either too little or too much glue. This issue was almost entirely eliminated with placement practice however.

Table 5.1 shows the fully populated transceiver circuits, the design changes they underwent and failure analysis. A total of 8 circuits were manufactured, with evolutions in design in order to reduce identified sources of failure. Therefore process yield was never optimized since getting a circuit with functionality was a priority. All dates shown in the table are estimates, to give an idea of chronology. It is important to note many partial builds were done in between these dates where sources of failure were noticed and designs were altered.
<table>
<thead>
<tr>
<th>Circuit Number</th>
<th>Approximate Start Date</th>
<th>Design Changes</th>
<th>Programmable?</th>
<th>If No, Why?</th>
<th>Process or Design Dependent Issues</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>8-Oct</td>
<td>Original Design</td>
<td>No</td>
<td>Shorting from conductive epoxy spilling over pads and onto dielectric.</td>
<td>Both process and design. Design caused high probability of conductive epoxy shorting through dielectric with small pads and a ground layer underneath. Process issues involved the use of a dielectric that cannot withstand conductive epoxy.</td>
</tr>
<tr>
<td>2</td>
<td>28-Oct</td>
<td>Removed ground plane from under COTS</td>
<td>No</td>
<td>Shorting between components. Traces sometimes grounded. Microprocessor connections improperly setup.</td>
<td>Design issue: Too much conductive epoxy used, wicked under COTS and shorted them. Not enough polyimide was used in areas with overlapping conductors. Gaps in dielectric coverage resulted from variations in design file rastering.</td>
</tr>
<tr>
<td>3</td>
<td>8-Dec</td>
<td>Changed design from Low Voltage setup to LDO</td>
<td>No</td>
<td>Shorting between the ground layer and the RF circuitry along with other instances of shorting.</td>
<td>Process: Printing misalignment resulted in some shorting. Still too much conductive epoxy being applied.</td>
</tr>
<tr>
<td>4</td>
<td>8-Dec</td>
<td>Same, then tried putting on 30 mm wire for antenna</td>
<td>Yes</td>
<td>N/A</td>
<td>Tried to get RF portion to work by attaching a 30 mm wire antenna. Did not work. Need ground layer back under matching network.</td>
</tr>
<tr>
<td>5</td>
<td>8-Jan</td>
<td>Implemented PIFA antenna, put ground plane back under matching network and shrunk matching network</td>
<td>No</td>
<td>Shorts between routing traces and ground.</td>
<td>Process: Misalignment between layers resulted in shorting of one of the programming lines.</td>
</tr>
<tr>
<td>6</td>
<td>13-Jan</td>
<td>No change</td>
<td>Yes</td>
<td>N/A</td>
<td>RF still not functional. Potentially from dielectric thickness variation.</td>
</tr>
<tr>
<td>7</td>
<td>1-Feb</td>
<td>Adjusted PIFA and matching network components. Shifted the matching network away from the QFN48 package. Used less epoxy to try and reduce TCE resultant cracking</td>
<td>No</td>
<td>Short on routing trace on top of package to package ground.</td>
<td>Process: Short likely from pinhole in the polyimide. Everything else on the circuit is testable while unpowered seems to work. This issue unfortunately prevents programming.</td>
</tr>
<tr>
<td>8</td>
<td>1-Feb</td>
<td>Sintered at 150°C and below in an attempt to reduce cracking of silver ink over C-7 Adhesive</td>
<td>No</td>
<td>Short to ground on trace used for programming.</td>
<td>Process: Short from tiny gap in polyimide. Likely a result of changing output of the ink. Can be fixed with printing more polyimide.</td>
</tr>
</tbody>
</table>

Table 5.1: This table shows the progression of fully completed transceiver prototypes. Many partial fabrications were made in between these complete builds. Main failures and their determined reason were also included along with significant design changes that were made.
5.2 MEMS Microphone Array Packaging Application

The microphone chips were designed and fabricated by Joshua Krause and Robert White at Tufts University. Krause et. al. discusses the manufacturing procedure and the results obtained in wind tunnel tests from the microphone chips [50]. Each microphone has a diaphragm which deflects corresponding to pressure. This deflection results in a capacitance change which is then output from the sensor. Through this method, the fluctuating pressures under the turbulent boundary layer and over the 64 microphone array can be analyzed. Figure 5.2 shows an image of the MEMs microphone array with 64 individual microphones from which turbulent boundary flow data can be obtained. Figure 5.3 and Figure 5.4 show cross-sections and an SEM of an individual microphone respectively. Principal features are labeled in the figures. Figure 5.5 depicts the standard packaging process of the sensor. This process is defined by placement of the sensor in CPGA and the use of wirebonding to electrically integrate the two [50].

![Figure 5.2: The MEMS microphone array developed by Krause et. al. is shown. There are 64 individual microphone membranes, each which take data on the turbulent boundary layer through the capacitive measurements resulting from pressure change. This chip is then electrically connected to a CPGA for capacitance data access [50].](image-url)
Figure 5.3: The schematic for a single microphone is shown above. Two cross-sectional views are shown [50].

Figure 5.4: An SEM image of an individual microphone element is shown above [50].

Figure 5.5: The series of pictures above show the packaging method employed for the MEMS Microphone Array sensor [50].
Due to the sensor’s manufacturing methods, the edge of the sensor is exposed silicon which can result in an electrical short when attempting to do low profile wire bonds which contact the edge of the chip. Low profile wire bonds are necessary to reduce the interference the wire bonds have with the air flow. Namics Chipcoat G8345-6 epoxy was hand painted along the corner of the device to reduce the amount of shorting that occurred. However, due to the difficulty of accurately placing the epoxy along the edge, many shorts occurred which effected the yield obtained from their 64 microphone array. The use of AJP technology was investigated for more precise and repeatable shielding of the silicon from the wire bonds thus increasing the yield of working microphones. The subsequent section documents the targeted dielectric deposition onto this sidewall.

However, the profile of the wire bonds may be disturbing the turbulent boundary layer flow the microphone array is trying to measure. For testing, the microphone array is directional. The flow direction is depicted in Figure 5.2, down the axis without any wire bonds. As can be seen in Figure 5.6 the relative profiles of major features of the chip are shown. The highest feature is the wire bond height, which can potentially be greatly reduced through the implementation of AJP technology. Instead of the hand painted conductive epoxy, a several micron layer of polyimide along with hand applied Armstrong C-7/W epoxy would be used to shield the silicon along the exposed edge and sidewall respectively. Theoretically the whole sidewall could be covered in AJP polyimide, however, for this demonstration, the sidewall was painted with C-7 epoxy which is easier to control on vertical surfaces. Then conductive traces would be printed up the sensor sidewall connecting the ceramic pin grid array (CPGA) and the sensor pads. The final sub-section documents the attempt on avoiding the use of the high profile wire bonds in order to reduce device surface topology that interferes with the air flow. It is important to note that a microphone is considered nonfunctional if the element shows significant 3rd harmonic distortion (approximately around -50 dB or worse) indicating a possible short. A microphone is also considered
non-functional if its capacitance is too low compared to its neighbors indicating a possible open interconnection. Through either of these two metrics, a microphone is determined to be non-functional.

![Figure 5.6: The profilometry of the packaged sensor invented and fabricated by Krause et. al. is shown. The wire bonds are the dominant feature in terms of height that can be reduced [50].](image)

5.2.1 Dielectric Deposition in Conjunction with Wire Bonding

Polyimide was printed along the edge of the chip surface to shield the exposed bare silicon. The intent of this process was to replace the hand painting of epoxy along that edge which was difficult and effected the yield of the microphone array. Two passes of polyimide were printed onto the sensor at an elevated platen temperature of 40°C. The elevated temperature was used to increase the speed the ink’s solvent dried to minimize movement after printing. Only two sensors were done due to limitations in sensor availability. The polyimide was baked overnight for 13 hours at 130°C in atmosphere. There was no obvious changes in the PI after baking. Profilometry measurements show the film is between 0.5-1.5 µm thick. This variability is no concern assuming the film is solid. Then wirebonds were attached to the pads on the sensor and on the CPGA. The pictures and plots were created by Professor Robert White.
The two chips that were printed on with polyimide are denoted as MEMS109-6 and MEMS109-9. All the pictures shown are for MEMS109-6. Figure 5.7(a) shows the edge after dielectric deposition. As can be seen, an approximately 160 µm polyimide line was printed along the edge. The lighter gold color on the leftmost edge of the device under the polyimide is the exposed silicon. Through this picture it appears that the edge was successfully covered. Some spots on the surface of this chip however caused the polyimide print to shoot away from the targeted area. Potential causes of this may be finger oil, or another substance that was only on some spots of the sensor edge. One such spot is shown in Figure 5.8. As can be seen, the polyimide layer disappears on the edge of the sensor, flowing away from the deposition site to in-between sensor traces to the right. During printing it appeared to go over the pads. However after curing, analysis showed that the polyimide went around the pads, roughly 4 µm tall. That means this process has a decent margin for error. Figure 5.7(b) and Figure 5.8 show the sensor with the wire bonds attached in two different locations. MEMS109-9 did not experience any of the polyimide adhesion issues MEMS109-6 did. Instead the polyimide stayed in the deposition target area.

Figure 5.7: The pictures above of MEMS109-6 show a part of the microphone chip edge after dielectric deposition and again after wire bonding. This is how the process was intended to work.
Figure 5.8: The picture above of MEMS109-6 shows what happens when the polyimide does not adhere to the target surface. The polyimide wicked to the right in-between two of the sensor’s traces. Since the sensor pads are 4 µm tall, they were not covered when the polyimide flowed by them.

The capacitance results for the two sensors with polyimide prints along with a control sensor packaged with the previous method, sans polyimide, are included below. The capacitance is a measure of the diaphragm deflection with respect to the bottom electrode. Therefore, the environmental pressure changes are reflected by the microphone sensors capacitance changes. MEMS109-1 was packaged using the previous method of hand-painting epoxy onto the edge. The difficulties in applying the epoxy accurately resulted in 39/64 elements that were functional while the rest shorted. This yield rate is around 60%. Figure 5.9 shows an intensity plot of the 64 microphone sensors for MEMS109-1 and their respective capacitances.
Figure 5.9: MEMS109-1 is a MEMS microphone array packaged with the old method of hand painting epoxy along the edge to shield the exposed silicon. There are many shorted elements with only 39/64 functional ones.

Figure 5.10 and Figure 5.11 shows the sensors MEMS109-6 and MEMS109-9 respectively. Both of these sensors used AJP polyimide for precise and repeatable dielectric application. As previously discussed, MEMS109-6 had areas where the polyimide did not adhere to the surface and instead moved away from the exposed silicon edge. Predictably, this effected yield. As can be seen in Figure 5.10, there are nine shorted elements meaning 55/64 elements are functional. This is drastically better than yield from the hand-painted epoxy method. Figure 5.11 shows an even higher yield with 60/64 functional microphones. This data indicates the use of AJP technology can greatly increase the yield for these MEMS microphone arrays.
Figure 5.10: MEMS109-6 leveraged AJP technology to print polyimide along the exposed silicon edge. Despite adhesion issues with the polyimide in several locations, 55/64 elements were functional.

Figure 5.11: MEMS109-9 was made with the same process as MEMS109-6. No adhesion issues with polyimide on the surface of the sensor occurred resulting in a yield of 60/64 functional elements.

5.2.2 Replacement of Wire Bonding with Printed Sidewall Interconnects

The replacement of the wire bonds with low profile printed sidewall connections may improve the accuracy of the sensors by disturbing the TBL flow less. This technique is more complicated than that employed in the previous sub section. As previously mentioned, C-7 epoxy was hand-painted onto the
sidewall of the chip along with the polyimide lines printed along the edge. Then conductive traces were printed up the sidewall integrating the chip with the CPGA.

Figure 5.12 shows the C-7 epoxy painted on the sidewall to shield it from the conductive traces that will subsequently be printed. The C-7 also performs the essential purpose of filling in a trench between the chip and the package. In order for the AJP trace to make a successful connection, there cannot be trenches where line breaks will occur. The filling of this trench also results in a nice fillet which assists the conductive trace up the sidewall. By removing the 90° concave corner, ink pooling effects are eliminated at this location. The epoxy was cured for 30 min at 100°C.

After the C-7 application, polyimide was aerosol jet printed to shield the top edges of the sensor using the same method described in the previous section. Two passes of polyimide on each of the sensor edge adjacent to the pads was done and then cured for overnight at 130°C.

The side wall interconnections were then printed in order to electrically connect the sensor and the package. Figure 5.13 shows a portion of one side of the chip and the sidewall traces. Each trace is approximately 50 µm and consisted of five passes of the NovaCentrix HPS-030AE1 Silver Flake Ink in the

Figure 5.12: The C-7 applied to the sidewall can be seen in the red box. This epoxy was hand-painted on to cover the bare silicon sidewall and to fill a trench between the CPGA and the chip. This enables printing conductive traces up the sidewall for sensor-package integration.
AJP system. The ink was sintered for 19.5 hours at 130°C. This process required a much higher density of sidewall interconnect lines than the transceiver circuit. Sensor to package alignment must be done since the sensor is hand-placed into the package. Despite a significant amount of preparation, alignment challenges were still present. However, none appear to cause a microphone sensor to fail. This may be a result of inaccuracies in the measurement of the misalignment between the sensor and the package. Using a higher precision tool to determine offset and rotation of the sensor compared to the package should fix these inaccuracies. Figure 5.14 shows what happens to the traces at the other extreme end of the sidewall where the alignment is worse. As can be seen, after it was noticed initial prints were off, the trace location was adjusted and reprinted, hence two traces coming from one sensor pad. Several locations on the pad likely resulted in open lines. One location appears to have a bubble in the epoxy that popped, breaking the trace. In another location, several package pads had peeled up due to the package modifications made in order to make the sensor fit during a previous step.

*Figure 5.13: Part of the acoustic sensor can be seen with the printed conductive sidewall traces connecting the chip pads to the package pads.*
Figure 5.14: Part of the acoustic sensor where alignment issues occurred for the sidewall interconnect lines can be seen.

Figure 5.15 shows the capacitance of the microphones on this module. 25 elements show 3rd harmonic distortion of -50 dB or worse, probably signifying a short. In order to clearly show which microphones were shorted, a filter was applied to the plot at -50dB so that all microphones with a worse distortion show up as white in the figure. 2 elements show a 3rd harmonic lower than -50 dB but capacitances are lower than 25 pF. This may indicate that these two microphones are not connected. Functional microphones were identified by having a 3rd harmonic lower than -50 dB and a capacitance greater than 25 pF. Therefore 37 elements of the 64 were determined functional. This is a 57% yield. This low yield is potentially due to difficulties covering the sidewall with C-7 to shield the exposed silicon. Any pinholes in the C-7 would result in shorts.
6 Ink Ageing and Reliability

Ink ageing testing was done to determine the long-term viability of two types of aerosol jet printed inks, silver and carbon nanotubes (CNTs). This is important knowledge to determine the long-term reliability of an aerosol jet printed board, and helps frame whether AJP is simply a rapid prototyping method for quick-turn circuit innovation or a candidate replacement for commercial and industrial PCBs. As such, two tests were identified through the IPC standards for rapid ageing. IPC standards are a set of industry standards aimed at standardizing the production of electronics. Multilayer test structures composing of barbell shaped conductor prints, either Ag or CNT, and dielectric, polyimide, were printed so that resistance, dielectric breakdown voltage and carrying capacity of the lines could all be measured. Test structures for adhesion tests were also created so that the following adhesive tests could be done at each evaluation step of the ageing process: Ag on SiO$_2$ and Ag on a polyimide layer on a SiO$_2$.
substrate. Hoerber et. al. is the only source the author is aware of that has done rapid ageing tests on aerosol jet printed inks [51]. These tests focused solely on Ag ink on four thermoplastics with the result that ageing has only marginal effects on conductivity but significant effects on adhesion [51].

According to IPC standard J-STD-001C, a class II device is the classification for dedicated service electronic products. This encompasses “products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically, the end-use environment would not cause failures” [52]. According to IPC-TM-650-2.6.3F, the Moisture and Insulation Resistance test, a class 2 device is tested in the 50°C/85% relative humidity regime. The full test lasts five days. Therefore the testing was designed to take periodic measurements throughout the moisture ageing process in order to observe any ink deterioration. The second test was to determine the ink’s susceptibility to thermal changes as outlined by IPC-TM-650-2.6.7.2a Thermal Shock. Through this guideline, the test condition of -55°C to 125°C in 15 minute increments was selected in order to encompass the extremes the board could operate in. In other words, the board spends 15 minutes at -55°C then is rapidly switched to 125°C for another 15 min. A cycle is therefore a half hour total. This test is done for 1000 cycles with periodic testing in between.

The electrical testing was done on two variations of the structure as shown in Figure 6.1. This artwork was chosen in order to get resistance tests of lines above and below dielectric, test dielectric breakdown voltage, and test conductivity linearity on one structure. Adhesion tests were done on modules similar to those shown in Figure 6.1. These structures were not originally intended for high precision 4-wire measurements, and as such are not in a traditional four-wire resistance measurement configuration.

The rapid ageing process tests are described below. IPC standards were used as a reference in determining these criteria, especially for resistance change. The dielectric breakdown tests and the
linear response to electrical excitation tests are derived from perceived requirements of a multilayer printed circuit board. The dielectric breakdown tests are shown in the Appendix.

![Image](image_url)

Figure 6.1: The figure above shows the structures used for the ageing tests. There is an Ag bottom layer “barbell” structure consisting of one line with pads on each side. The second layer is dielectric which shields the lower line from the subsequently printed upper line. Lastly, the upper line with pads is printed such that the lower and upper Ag structures don’t connect. The figure on the right has one extra dielectric deposition step used to see the effect of shielding the lines with polyimide from the environments.

A CNT ink was used for rapid ageing testing along with the silver ink used throughout this research in order to provide a comparison between a traditional conductor and a more novel, organic conductor. A fundamental component of the process developed in this thesis is its applicability to a wide range of inks and substrate materials. By using virtually the same process and structures to test the CNT ink, it not only allows for a one-to-one comparison between the conductors, but also demonstrates the ease with which different inks can be printed. Many applications prohibit metallic conductors, thus CNTs are one of many alternatives. The formulation of CNT ink used for this testing was CNTRENE® 3023 A7-R SWCNT made by Brewer Science, Inc. An SEM of this ink after aerosol jet deposition is shown in Figure 6.2. As can be observed from the figure, the nanotube formulation does not align when deposited, but rather makes a matrix of unorganized tubes.
Figure 6.2: Shows the CNT network after aerosol jet deposition. Larger rings of CNTs appear to form randomly on top of the material. This image was taken by Brewer Science, Inc.

6.1 Conductor Electrical Properties: Carrying Capacity and Response of Line

Conductivity to Electrical Excitation

A current sweep was performed to insure the linearity of the response of the printed lines. The printed conductors need to behave linearly throughout the ageing process in order to be reliable. Figure 6.3 and Figure 6.4 show the current vs voltage for silver and CNTs respectively. As can be seen from the Figure 6.3, a plot of the electrical testing on the silver line, a roughly linear response is seen to the current sweep. A current sweep between 0 and 1 amp resulted in a roughly linear response from 0 to 0.9 volts. The electrical testing of the CNT line, Figure 6.4, shows a linear response to the current sweep from 0 A to 0.18 A. This plot was voltage driven since the voltage increases to 20 V, the maximum of the
supply used. The difference between these two plots is a result of the difference in conductivities between the two materials.

![Response of Ag line to a Current Sweep](image)

*Figure 6.3: The electrical response of a silver line to a current sweep. As can be seen, voltage and current have a roughly linear relationship as would be expected out of silver. This data was taken after the first thermal shock test.*
The electrical response of CN

t line to a current sweep. As can be seen, voltage and current exhibit a very linear relationship. This data was taken after the first thermal shock test.

The carrying capacity of the silver lines was also tested several times. The significance of this test is that it gives a current density for which the lines have instantaneous failure. This provides a good idea of how much current the lines can handle. One example of such a calculation is shown in equation (2).

The trace length was 1 mm, the width 40 µm, the height approximately 3 µm and the measured current at instantaneous failure was 2 amps.

\[
J = \frac{I}{A} = \frac{2A}{120 \times 10^{-8} \text{cm}^2} = 1.67 \times 10^6 \frac{A}{\text{cm}^2}
\]

where \( J \) is the current density, \( I \) is the measured current at instantaneous failure, and \( A \) is the cross sectional area. It is important to note that is this instantaneous failure which doesn’t include long term failure mechanism like electro-migration. This result is believable due to similar experiments done on sputtered silver by Hauder et al [53]. Their tests showed sputtered silver survived over 10000 hours at 7.3\( \times 10^6 \) A/cm². Since the aerosol jet deposited silver has worse electrical properties than the sputtered silver, it follows that instantaneous failure can be achieved at the calculated current density. The aerosol
jet printed lines can carry substantial current (up to 2 A in this case for a 3 µm thick line). However, current carry capability is not as high as sputtered silver, so for some high current applications AJP silver may not be appropriate.

6.2 Resistance and Adhesion Testing Procedure

One of the essential metrics for the effects of rapid ageing on the inks is the change in resistance. As the traces are stressed with moisture and temperature change, the conductivity can be affected. Therefore resistance change over the course of the tests was measured using the four-point probe method. The four-point probe method was used due to its greater accuracy and its ability to circumvent contact resistance. It is also the resistance measurement standard used across all industries. As shown in Figure 6.1, the structures were formed by two “barbell” structures perpendicular to each other and crossing at the midpoint. The barbell structures were electrically insulated from each other by polyimide. Therefore half the lines go below the polyimide insulator and half go above. This was done to predict any anomalies that would occur in the ageing of a multi-material stack. Since a small portion of the upper conductor goes over the polyimide, significant changes in the conductor’s resistance for reasons such as thermal coefficient of expansion (TCE) mismatch between it and the dielectric can be quickly identified. This also simulated a multilayer circuit design, such as the transceiver circuit, which was the goal of the test. The significance of this is that on the multilayer board, some silver will be on SiO₂, while some will be on polyimide. Therefore it is important to track how a simplistic model system is effected by rapid ageing.

The resistance measurements were taken with a Signatone s-1160 probe station using an Agilent 34420A 7½ Digital Nano Volt/Micro Ohm Meter. Fine probe tips were used so that two probes could fit on each of the 300 µm pads (1 source and 1 sense). The measurements were taken at intervals depending on the test conducted. Then the data was analyzed with MATLAB and the results were plotted.
Adhesion test wafers were put into the thermal shock and the moisture/insulation resistance rapid ageing environments for the sole purpose of tracking adhesion change. These tests roughly followed the guidelines of IPC-TM-650-2.4.1d. A suite of adhesive tape strengths were used which consisted of the following: 16 oz-force/in, 30 oz-force/in, 50 oz-force/in, 60 oz-force/in, 75 oz-force/in, 90 oz-force/in. These tests are based on visual results, therefore are less quantitative then the moisture and thermal shock resistance change tests. Each adhesion wafer had silver and CNT modules in the shape of a barbell. Half of both types of modules were on SiO$_2$ while the other half was on polyimide. Therefore for both of the rapid ageing environments, four results were analyzed: Ag on SiO$_2$, Ag on PI, CNT on SiO$_2$, and CNT on PI. Figure 6.5 depicts the testing of adhesion. As can be seen from the picture, the tape is being removed along with the structures which were adhered to the substrate. Figure 6.6, Figure 6.7, Figure 6.8, and Figure 6.9 show examples of how modules respond to the adhesion testing. These pictures were taken after 379 cycles of the thermal shock test.
Figure 6.5: An example of the adhesion testing. The tape has already been applied and is being pulled off. As can be seen, all the structures are being removed from the wafer and are sticking to the tape.

Figure 6.6 and Figure 6.7 show silver and CNTs on SiO$_2$. In Figure 6.6, (a) shows the adhesion modules before they are tested, (b) after adhesion test with 16 oz-force/in tape, (c) after adhesion test with 30 oz-force/in tape, (d) after adhesion test with 50 oz-force/in tape. As can be seen from these pictures, the modules are effectively destroyed after the first test of adhesion strength. Figure 6.7 shows (a) the CNT modules before tape application and (b) after application of 16 oz-force/in tape. As can be observed, the CNTs were completely pulled up by the 16 oz-force/in tape.
Figure 6.6: The adhesion testing results for silver on SiO$_2$ on the thermal shock wafer after 379 cycles is shown above. As is shown, (a) is the modules before testing, (b) is after a test with 16 oz-force/in tape, (c) after a test with 30 oz-force/in tape, and (d) after a test with 50 oz-force/in tape.

Figure 6.7: The adhesion testing results for CNTs on SiO$_2$ on the thermal shock wafer after 379 cycles is shown above. As can be observed, (a) is the CNT structures before testing, and (b) is the structures after testing with 16 oz-force/in tape. The structures have been completely removed in (b).

Figure 6.8 and Figure 6.9 depict silver and CNTs structures on a polyimide layer. This test was done to determine if adhesion would affect the layers on top of the dielectric for a multilayer structure than those that are below it. One of the main challenges experienced during this test is the tendency for
the polyimide to peel off the substrate when it was gripped from its edge. If the tape was only applied to the center of the polyimide, the polyimide adhered strongly to the substrate. Since this was very difficult to do, the test results below show the effects of simply applying tape over the whole polyimide patch including the structures on top of it. Some of the data that survived the 16 oz-force/in was more successfully tested without catching the edge of the polyimide. Figure 6.8 (a) shows the silver structures on the polyimide before adhesive testing and (b) shows the surface after the polyimide and the structures peeled off together. As is shown previously in the SEM images of the silver ink and the polyimide, it appears the silver strongly adheres to the polyimide. Figure 6.9 shows (a) CNT structures on polyimide before adhesive testing and (b) after application of the 16 oz-force/in adhesive tape test.

Figure 6.8: The adhesion testing results for silver on polyimide on the thermal shock wafer after 379 cycles is shown above. As is shown, (a) is the modules before testing and (b) is after a test with 16 oz-force/in tape. The polyimide is clearly ripped away with the adhesive tape in (b) taking with it all the silver test structures.
Figure 6.9: The adhesion testing results for CNTs on polyimide on the thermal shock wafer after 379 cycles is shown above. As can be observed, (a) is the modules before testing and (b) is the modules after the testing with 16 oz-force/in tape. Once again the polyimide clearly ripped away with the adhesive tape as shown in (b) taking the CNT structures with it.

6.2.1 Estimating Effect of Probe Placement Variability

Due to the lack of a traditional 4-point resistance measurement structure where the line length the resistance is being measured across is precisely known, an analysis was done of the effect of probe placement variability on the results to ensure significance of the findings. Figure 6.10 shows a model of one of the ageing structures. The trace between the pads has a 30 µm width and 2.18 µm thickness. The pads are both 300 µm squares with 2.18 µm thickness. The thickness and width measurements are based off of measurements taken on printed modules with a Tencor profilometer and a confocal microscope.

The method for determining probe placement variability was an electric currents simulation in Comsol Multiphysics®. Based on the analysis of many measured structures and scratch lines from their measurements, the extreme and middle points where chosen. Figure 6.11 shows the Comsol® model with the probe points superimposed onto its surface. All the points are for the sense (low and high) of the 4-point resistance measurement. The source (low and high) were set the extreme sides of the structure as denoted in Figure 6.11 by the red and black boxes. This was determined to be acceptable since the probe locations of the source were always at least 100 µm towards the extremes of the structure compared to the sense probes. Since 4-point resistance measurements measure the resistance between the sense probes, this model was deemed effective. By looking at this figure, one can infer that having sense probes at 1 and 2 would result in a minimum resistance while having them at 4 and 8 would result in a maximum resistance. The non-uniformity of the cross-section is why simple electrical equations were not used.
Figure 6.10: The dimensions of the barbell-like structure used for the ageing studies is shown above. All units are in millimeters.

Figure 6.11: The above schematic is the Comsol® artwork with the addition of the probe points where voltage data was taken. These points were chosen by reasonable extremes for resistance probe placement. These are all “sense” probes. The source was chosen as the sidewall area on the furthest walls of the module. They are denoted by red (source high) and black (source low).

The material for the simulation was set to silver. Figure 6.12 shows the simulation’s graphic after computation. As expected, the trace has a high gradient of electric potential due to its width and length disparity compared to the pads. The data from this simulation is shown in Table 6.1. The voltage at each probe point is documented in the table. This information will then be used to determine the resistance between the various probe points.
Figure 6.12: The above module shows the electric potential across the printed structure. As expected, the trace between the pads is the location of the highest gradient of electric potential.

Table 6.1: Voltage values of probes as shown in Figure 6.11. This data was used to calculate error bars resulting from probe placement for the 4-wire resistance measurements.

<table>
<thead>
<tr>
<th>Voltage Probe 1 (V)</th>
<th>Voltage Probe 2 (V)</th>
<th>Voltage Probe 3 (V)</th>
<th>Voltage Probe 4 (V)</th>
<th>Voltage Probe 5 (V)</th>
<th>Voltage Probe 6 (V)</th>
<th>Voltage Probe 7 (V)</th>
<th>Voltage Probe 8 (V)</th>
<th>Voltage Probe 9 (V)</th>
<th>Voltage Probe 10 (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.19E-5</td>
<td>1.91E-3</td>
<td>1.92E-3</td>
<td>1.97E-3</td>
<td>1.97E-3</td>
<td>1.92E-3</td>
<td>5.76E-5</td>
<td>1.24E-5</td>
<td>3.83E-5</td>
<td>1.94E-3</td>
</tr>
</tbody>
</table>

Now the resistance between any two of these probe points can be solved for with equation (3):

\[ R = \frac{V_2 - V_1}{I} \]  

(3)

where V is the resistance at a probe point, I is the current going through the structure, and R is the resistance. Since the data was taken on an Agilent 34420A Micro-Ohm Meter, the current used to measure resistances in the single ohm range is 0.01 Amps. As such, this value was used in the equation above. The min, max and middle values along with the total resistance are shown in the Table 6.2 below.
In order to determine a normalized error, an average resistance from one pad to the other within the probe area must be approximated. If the number of probe points on the left pad, as shown in Figure 6.11, are increased to mirror that of the right pad, then the weighted average of voltage for each can be calculated. Then the average resistance can be calculated using equation (3). Finally, the normalized error can be calculated by (4):

$$E = \frac{R_{\text{MAX}} - R_{\text{MIN}}}{x_{\text{probe}}} = 6.33 \times 10^{-2}$$

(4)

where $R_{\text{MAX}}$ is the resistance max, $R_{\text{MIN}}$ is the resistance min and $x_{\text{probe}}$ is the approximate mean resistance over the probing area. Therefore the resistance is up to 6.33% too low or too high on any given measurement. If the number of probe points on the left and right pad are not weighted, the resulting change is only 0.01%. This confirms the method that six points per pad is enough of a sample to get an accurate evaluation of the average probe resistance in the probing area. As seen in Figure 6.12 almost all the voltage change in the module occurs on the trace between the pads once again reaffirming the validity of the employed method. This error is already incorporated into the resistance results since they are based on results with probe variability. Therefore, the resistance changes between each test can be attributed up to 6.33% from probe placement variability.

### 6.3 Rapid Ageing Results

The following resistance results were analyzed with MATLAB and plotted using the “errorbar” function. This function makes the error bars on the graph one standard deviation from the mean. The data compiled below is the resultant of each individual structure’s resistance normalized to its initial
pre-ageing test. The mean and standard deviation data shown on many of the plots below is the mean and standard deviation of all these individual normalized resistance changes from each test combined. The reason this was done was to effectively circumvent the need to calculate resistivity. By analyzing the data in the form of resistance change, the result is a non-dimensional number which can be easily compared to all other similar structures regardless of their initial resistance. This effectively removes the need to figure out the exact dimensions of every structure. The equation is shown in (5):

\[ R_{\text{change}} = \frac{r_x}{r_0} \]

where \( R_{\text{change}} \) is the resistance change, \( r_x \) is the resistance at time \( x \), and \( r_0 \) is the initial resistance before testing was started. Each data point on the resistance change plot thus shows the average resistance change of 96 to 196 structures throughout the ageing process, depending on the data set. These methods also allow for the comparison of traces that are completely on \( \text{SiO}_2 \) and those that go over polyimide at the intersection with the aforementioned type of line. This test wasn’t to determine whether it was better to go over polyimide or not, but rather to analyze how these lines as a system aged. Thus summing their mean resistance changes and determining the accumulative standard deviation is valid to see how the simplified multilayer system changes during the test. The following data shows how rapid ageing mostly seems to effect the adhesion of the printed modules and not the resistance.

6.3.1 Thermal Shock Results

As previously stated, the thermal shock test was conducted according to IPC-TM-650-2.6.7.2a Thermal Shock. The test units were exposed to temperatures of -55°C to 125°C in 15 minute cycles as a representative regime of potential operation temperatures. In other words, the board spends 15 minutes at -55°C then is rapidly switched to 125°C for another 15 min. This is done for 1000 cycles with periodic testing in between. 192 silver structures were tested along with 96 CNT structures. Since the
fabrication of the modules result in three layer structures in certain places, three sinter steps were needed to make the conductor and dielectric layers functional. A sinter step followed each printed layer. Therefore, before the ageing test, the following sinter steps took place: first layer silver sintered at 250°C for 1 hour and 20 min, polyimide layer sinter at 100°C for 30 min, second layer of silver sintered at 240°C for 1 hour and 25 min. The CNTs were printed after the sintering of the silver structures to reduce unnecessary heat exposure. Once again, these structures are shown in Figure 6.1. The intersection of the cross formed by the two lines in a structure is shielded with the dielectric polyimide to prevent shorting.

6.3.1.1 Resistance Change Analysis

The silver structures are analyzed in Figure 6.13 and Figure 6.14. Figure 6.13 shows the data from the thermal shock tests. As can be seen there is no statistically significant change in the mean of each data set, just an increasing in the standard deviation. It is theorized that this increase in the standard deviation of the resistance change is a direct result of adhesion issues with the silver structures to the substrate. The adhesion issues effect the resistivity by causing material loss and bends in the structure. Figure 6.14 shows the increase in failed modules as the thermal shock tests are conducted. This information verifies the damage sustained by the structures throughout this test. The data, which shows over 40% failure of the structures by the end of the thermal shock testing, indicates a failure mode such as adhesion taking place. The conclusion drawn from this data set is therefore that the resistance of the ink is not greatly affected by the rapid temperature change, but the adhesion to the substrate is. Since the resistance change is the metric being measured, the traces that go under and over the polyimide have been combined into the same data set. The very small standard deviation shown in the beginning of the thermal shock data indicates this is an acceptable choice since adhesion issues tended to effect the pads more than the lines themselves. This is potentially a result of the force applied by probing the pads for every test.
Figure 6.13: The results of the rapid ageing thermal shock tests on silver structures as previously outlined. The mean is the blue circle and one standard deviation above and below the mean is denoted with the blue lines.

Figure 6.14: The percentage of failed modules as cycle number increases for this silver structures is shown above. Adhesion appears to be the main failure mechanism.
The CNT structures are analyzed in Figure 6.15 and Figure 6.16. Figure 6.15 shows the data from the thermal shock tests. As can be seen there is no statistically significant change in the mean of each data set. However, there is an increase in the standard deviation throughout testing. In this case it appears the increase in standard deviation of the resistance change is an artifact of the fragility of the CNT structures. During measurement, the structures were damaged visibly during probing resulting in subsequent probing on a damaged pad. Therefore adhesion seemed to have played a role, just like with the silver, in the standard deviation change. Figure 6.16 shows the increase in failed modules as the thermal shock tests are conducted. This information shows just over 5% of structures were nonfunctional at the end of testing. The CNTs did not suffer complete adhesion failure like the silver, therefore the incidents of nonfunctional structures was greatly reduced. This may be due to the fact that the CNT structures are not bound as cohesively together as the silver structures. More testing will need to be done to verify this. The conclusion drawn from this data set is therefore that the resistance of the ink is not greatly affected by the rapid temperature change, nor is the adhesion effected enough to result in a plethora of complete failure. Therefore it appears the CNT ink is more compatible with this harsh environment. However it should be noted that the unreliability of the CNT ink is displayed through the resistance change plot. The CNTs are shown to have a high variability in resistance from test to test despite the mean staying approximately the same.
Figure 6.15: The results of the rapid ageing thermal shock tests on CNT structures as previously outlined. The mean is the blue circle and one standard deviation above and below the mean is denoted with the blue lines.

Figure 6.16: The percentage of failed modules as cycle number increases for the CNT structures is shown above. Adhesion appears to be the main failure mechanism.
6.3.1.2 Adhesion Analysis

The thermal shock adhesion tests for silver and CNTs on SiO$_2$ and polyimide are shown in Table 6.3, Table 6.4, Table 6.5, and Table 6.6. A columns numbers signify the cumulative number of adhesion failures for the modules as tape strength increases for a given ageing cycle. A red number indicates once all the tested modules failed during tape testing. Varying numbers of test samples were used for each test depending on the number of modules remaining. For example, some modules did not fail in early testing, so more were available for later adhesive tests. The minimum number tested was 8 modules and the maximum was 16 modules. Table 6.3 shows the strength at which silver adheres to SiO$_2$ before ageing. The strongest tape, 90 oz-force/in did not result in a single failure. However after 150 cycles, all the modules failed by 90 oz-force/in. The two subsequent tests experienced failure at the first tape strength 16 oz-force/in. This shows a drastic decrease in adhesion as the test is done. The CNTs on SiO$_2$, as seen in Table 6.4, also showed better adhesion in the early stages than in the later stages of testing. Although it is readily apparent that the CNTs adhere to the substrate with less strength then the silver, their bond to the substrate appears to occasionally withstand 16 oz-force/in tape tests.

<table>
<thead>
<tr>
<th>Tape Strength (oz-force/in)</th>
<th>Cumulative Adhesion Failures of Ag Modules on SiO$_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>0</td>
</tr>
<tr>
<td>30</td>
<td>0</td>
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<tr>
<td>50</td>
<td>0</td>
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<tr>
<td>60</td>
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<tr>
<td>75</td>
<td>0</td>
</tr>
<tr>
<td>90</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 6.3: The cumulative number of silver modules that failed under adhesive tapes on SiO$_2$ during the thermal shock tests is outlined in this table. As can be observed, there is a significant change in the adhesion of the silver to the SiO$_2$ substrate during the rapid ageing process. The silver modules go from being able to survive 90 oz-force/in tape to failing at the weakest tape of 16 oz-force/in.
Table 6.4: The number of CNT modules that fail under adhesive tape testing on SiO$_2$ during the thermal shock tests is outlined above. As can be seen, there is variability in the CNTs adhesion regardless of ageing. This is evidenced by the fact that all modules failed on the weakest tape the before testing, but then some survived to the second tape strength on subsequent tests. However, at the end of the tests it appears the environment had made affected the modules adhesion.

Table 6.5 and Table 6.6 show the adhesion test results for silver and CNTs on a layer of polyimide. This test was done to ensure silver wouldn’t have adhesion issues in a multilayer circuit. As previously mentioned, the polyimide’s adherence to the SiO$_2$ substrate failed before the silver’s adherence to the polyimide. This was partly because of the way polyimide peels when you pull it from its thin edges. With how the structures were designed, it was very difficult to not pull from the edges. Therefore the conclusion can be drawn that the silver-polyimide adhesion isn’t as big of an issue as polyimide-SiO$_2$. Table 6.5 shows silver modules and the polyimide surviving the adhesion tests until 50 oz-force/in. The long survival of these test structures to the adhesive tape is attributed to the edges of the polyimide being avoided with the tape as best as possible. However as the rapid ageing commenced, the polyimide-SiO$_2$ interface failed under the 16 oz-force/in tape every time. Table 6.6 shows CNTs on the polyimide throughout the thermal shock testing process. As can be seen, the CNTs failed every time they were tested under the weakest tape. This is due both to the weaker adhesive strength of the CNTs and because of the underlying polyimide peeling off the substrate.
Table 6.5: The number of failed silver modules on polyimide is shown in the table. As can be seen, the structures and the polyimide survived several tape strengths before rapid ageing, but as the testing commenced failure was achieved under the weakest tape.

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<tbody>
<tr>
<td>16</td>
<td>0</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>30</td>
<td>0</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>50</td>
<td>16</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Table 6.6: The number of failed CNT modules on polyimide is shown in the table. As can be seen, all the structures and the polyimide they were on failed under the weakest tape in all the tests. This is determined to be a result of CNTs and their weaker adherence to the substrate than silver and from polyimide peeling off the surface of the SiO2.

6.3.2 High Temp/High Humidity Results

As previously stated, another rapid ageing environment was high temperature and high humidity. This environment was in the 50°C and 85% relative humidity regime in accordance to IPC-TM-650-2.6.3F and the test lasted seven days with intermittent testing. 192 silver structures were tested along with 96 CNT structures. Since the fabrication of the modules result in three layer structures in certain places, three sinter steps were needed to make the conductor and dielectric layers functional. A sinter step followed each printed layer. Therefore, before the ageing test, the following sinter steps took place: first layer silver sintered at 250°C for 1 hour and 20 min, polyimide layer sinter at 100°C for 30 min, second layer of silver sintered at 240°C for 1 hour and 25 min. The CNTs were printed after the
sintering of the silver structures to reduce unnecessary heat exposure. Once again, these structures are shown in Figure 6.1.

6.3.2.1 Resistance Change Analysis

Data from the silver structures analyzed in the 50°C/85% relative humidity environment are shown in Figure 6.17 and Figure 6.18. Figure 6.17 shows the resistance change of the 192 structures over the 5 day test. Similar to the thermal shock tests, a significant change in standard deviation of each data set is observed but a less significant change in mean is observed. It appears that the resistance change is significant from the first test to the last. Therefore it appears that the silver ink actually slightly sintered in this elevated temperature environment. The increased standard deviation can be attributed once again to adhesion issues, a known problem with printed inks. As the environment effects adhesion, the resistance results become less consistent. As can be seen in Figure 6.18, slightly under 7% structure failure is observed by the end of this 5 day test. This indicates that the adhesion issues are not significant enough to cause mass module failure, but can affect the line conductivities.
Figure 6.17: The results of the moisture and insulation resistance tests as previously outlined. The mean is the blue circle and one standard deviation above and below the mean is noted with the blue lines.

Figure 6.18: The percentage of failed modules as over time is shown. Adhesion appears to be the main failure mechanism.
Data from the CNT structures is shown in Figure 6.19 and Figure 6.20. In Figure 6.19, the resistance change data set for this environment shows an interesting quirk, a drastic change in standard deviation after the first resistance change analysis. This could be a result of inadequate sintering before the test resulting in a wide range of resistances of the structures. However, the means of these tests increase over time, a behavior that is expected with ink ageing. Module failure for the CNT ink in this test is just above 2.5% as shown in Figure 6.20. Once again the CNT structures appear to show a much lower failure rate than the silver modules, however they also seem to be subject to more variability between measurements.

![Figure 6.19: The results of the rapid ageing moisture and insulation resistance tests on CNT structures as previously outlined. The mean is the blue circle and one standard deviation above and below the mean is denoted with the blue lines.](image)
Figure 6.20: The percentage of failed modules over time for the CNT ink is shown above. Adhesion appears to be the main failure mechanism. Scratching of the pads by the probes appears to be the main factor causing module damage.

6.3.2.2 Adhesion Analysis

The moisture and insulation resistance tests for silver and CNTs on SiO$_2$ and polyimide are shown in Table 6.7, Table 6.8, Table 6.9 and Table 6.10. Similar to the previous adhesion results, a column’s numbers correspond to cumulative failure of module adhesive. A red number indicates all modules tested failed. Number of modules tested varies from 8 to 32 depending on number of remaining modules from previous adhesive testing. As can be seen in Table 6.7, silver modules on SiO$_2$ survived the strongest tape during the first two tests. Only 4 modules failed by the strongest tape in the subsequent test after 2 days in the environment. However, after another day, complete module failure was observed. Interestingly the post ageing data has several modules that survived. Therefore it is reasonable to conclude that this environment had a significant effect on adhesion after 3 days in the environment. Table 6.8 shows CNT modules on SiO$_2$. Failure is consistently achieved at the first tape strength for the first 4 tests. However, after the moisture environment exposure, an adhesive test
actually shows some of the CNT modules surviving the strongest tape. This can best be described as an anomaly. The reason for such an occurrence has not been determined at this point and requires more investigation.

<table>
<thead>
<tr>
<th>Tape Strength (oz-force/in)</th>
<th>Pre Moisture</th>
<th>Moisture 1 (1 Day)</th>
<th>Moisture 2 (2 Days)</th>
<th>Moisture 3 (3 Days)</th>
<th>Post Moisture (5 Days)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>10</td>
<td>11</td>
</tr>
<tr>
<td>30</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>12</td>
<td>19</td>
</tr>
<tr>
<td>50</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>13</td>
<td>20</td>
</tr>
<tr>
<td>60</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>17</td>
<td>20</td>
</tr>
<tr>
<td>75</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>30</td>
<td>25</td>
</tr>
<tr>
<td>90</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>32</td>
<td>27</td>
</tr>
</tbody>
</table>

Table 6.7: The adhesive test for silver modules on SiO₂ throughout the moisture and insulation resistance environment are shown. As can be seen, the adhesion of the silver is greatly affected over time. After initially being able to withstand the strongest tape, 90 oz-force/in, the silver structures cannot survive the weakest tape, 16 oz-force/in. Due to the survival of the modules in the first three ageing cycles, more modules were available for the last two testing cycles allowing 32 modules to be tested each time.

<table>
<thead>
<tr>
<th>Tape Strength (oz-force/in)</th>
<th>Pre Moisture</th>
<th>Moisture 1 (1 Day)</th>
<th>Moisture 2 (2 Days)</th>
<th>Moisture 3 (3 Days)</th>
<th>Post Moisture (5 Days)</th>
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<tbody>
<tr>
<td>16</td>
<td>16</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>1</td>
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<tr>
<td>30</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>2</td>
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<tr>
<td>50</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
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<td>5</td>
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<tr>
<td>60</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>10</td>
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<tr>
<td>75</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>12</td>
</tr>
<tr>
<td>90</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>14</td>
</tr>
</tbody>
</table>

Table 6.8: The adhesive test for CNT modules on SiO₂ throughout the moisture and insulation resistance environment are shown above. An interesting anomaly can be observed. After failing under the weakest tape during the first four testing points, some of the structures survive the strongest tape after the rapid ageing environment exposure. 16 modules were tested for the Post Moisture test.
Table 6.9 and Table 6.10 detail the adhesive tests for silver and CNTs on polyimide. As can be seen in both tables, failure under the weakest tape occurs at every testing interval. The failure consistently is between the polyimide and the SiO\textsubscript{2} substrate and not between the CNT and polyimide interface. This data is likely effected by polyimide’s tendency to peel up from the substrate when pulled from its edges.

<table>
<thead>
<tr>
<th>Tape Strength (oz-force/in)</th>
<th>Pre Moisture</th>
<th>Moisture 1 (1 Day)</th>
<th>Moisture 2 (2 Days)</th>
<th>Moisture 3 (3 Days)</th>
<th>Post Moisture (5 Days)</th>
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</thead>
<tbody>
<tr>
<td>16</td>
<td>16</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>24</td>
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</tbody>
</table>

*Table 6.9: The failure of the silver modules on the polyimide is detailed in this table. As can be seen, all the silver structures fail under the weakest tape. It is important to note that the adhesive failure appears to be between the polyimide film and the SiO\textsubscript{2} substrate and not the silver/polyimide interface.*

<table>
<thead>
<tr>
<th>Tape Strength (oz-force/in)</th>
<th>Pre Moisture</th>
<th>Moisture 1 (1 Day)</th>
<th>Moisture 2 (2 Days)</th>
<th>Moisture 3 (3 Days)</th>
<th>Post Moisture (5 Days)</th>
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</thead>
<tbody>
<tr>
<td>16</td>
<td>16</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>16</td>
</tr>
</tbody>
</table>

*Table 6.10: The failure of the CNT modules on polyimide is detailed in this table. Once again complete failure is observed when tested with the weakest tape. It is important to note the adhesive failure appears to be between the polyimide and the SiO\textsubscript{2} substrate and not the CNT/polyimide interface.*

6.3.3 Elevated Temperature Results

Another set of test structures was put into a 60°C oven in a lab to see the accelerated effects of ageing. 112 silver and 96 CNT structures were made for this test. This test was not guided by any standard, but rather by the goal to simulate accelerated ageing in a lab-like environment. It was estimated that this would give the tightest data set in respect to standard deviation due to the relatively gentle environment the modules were being put into. These modules also were not multilayer modules. Instead they are simply a barbell structure of either silver or CNTs. The first measurements shown for
this data were started one month after the module had already been in the 60°C oven. This was due to the initial use of a 2-point probe resistance measurement method which become very inaccurate as an oxide formed on the metal. In order to make all results comparable and as accurate as possible, it was determined to switch to the 4-point probe method. The silver ink in this test case was sintered at 150°C for 2 hours, a much less effective sinter than the other rapid ageing modules experienced. The CNTs experienced a 2 hour bake at 40°C. Despite the initial data not included in the data set, the rest of the data is included in this thesis to demonstrate the effect of accelerated ageing in a lab environment.

6.3.3.1 Resistance Change Analysis

Data from the silver structures in the elevated temperature environment are shown in Figure 6.21 and Figure 6.22. Figure 6.21 shows the resistance change of the modules as months pass. As can be observed, there is definitive change in the mean as time passes. Also of note is the extremely tight standard deviation among these modules. Since none are being damaged by extreme environments, it appears the variation between measurements has been greatly decreased. A significant sintering effect is being observed as the modules actually don’t become worse conductors (as one would expect from ageing), but better. There is virtually no module failure as shown in Figure 6.22. Less than 1% of modules are nonfunctional and this is attributed the printing process. Therefore, the data shows that printed inks can actually improve in their conductivity over the span of months instead of just sintering at high temperatures (150°C-250°C).
Figure 6.21: The results of the rapid elevated temperature resistance tests on silver structures as previously outlined. The mean is the blue circle and one standard deviation above and below the mean is denoted with the blue lines.

Figure 6.22: The percentage of failed modules over time for the silver ink is shown above for the elevated temperature ageing tests. No major failure mechanism has been observed here.
Figure 6.23 and Figure 6.24 show the data obtained from the elevated temperature ageing of the CNT modules. Figure 6.23 shows a very interesting trend of first worsening of electrical conductivity followed by an improvement of it as time progresses. Further analysis needs to be done to understand this unique trend in the resistance change. The standard deviation of each data set is small, especially when compared with the CNT resistance change results from the other two rapid ageing tests. Module failure for the CNTs finished around 9.8% as shown in Figure 6.24. Since the modules have only one step increase in their percent failure and don’t exhibit a consistent trend, it appears that damage from probing or handling may have occurred.

![CNT Ink Elevated Temperature Ageing (60C)](image)

*Figure 6.23: The results of the rapid elevated temperature resistance tests on CNT structures as previously outlined. The mean is the blue circle and one standard deviation above and below the mean is denoted with the blue lines.*
Figure 6.24: The percentage of failed modules over time for the CNT ink is shown above for the elevated temperature ageing tests. The damage incurred during handling appears to be the lead cause for module failure.

7 Conclusions and Future Work

7.1 Conclusions

The process employed throughout this thesis results in PCB manufacturing with much greater flexibility at the expense of electrical properties. A variety of substrates, inks and sintering methods can be employed. However, conductor and dielectric deposition are not uniform presenting challenges for some applications such as RF. Also the resistivity of the inks is at best 2x worse, with ideal sintering conditions, than that of the bulk material. Therefore, these methods should be employed only where there is capability to handle more trace resistance than would be obtained with a traditionally manufactured PCB of the same layout.

This research focused on the production of heterogeneous material systems through use of the aerosol jet. A primary goal was the reduction of fabrication time for a complex circuit so that the
innovation cycle can be expedited. This was achieved as the concept to prototype fabrication time was reduced from on the order of many weeks or months to days.

Primarily, a SOC circuit was fabricated with novel methods. One of the shortcomings of the developed process is the hand-placing of many small components after the printing of all the circuit layers. This can be avoided through the expanded use of the integration method used on the microprocessor, sidewall interconnections. This integration method should be scalable for the integration of many COTs components. This would then eliminate the need for conductive epoxy from the process, which results in many electrical shorts.

The fabricated transceiver circuit was able to be programmed and to successfully execute the program. The program to demonstrate the functionality of the circuit flashed three LEDs in a pattern. This demonstration shows that the resistivity of the silver used as a conductor is functional. The circuits developed had a resistivity 3-7x higher than that of copper traces in a traditionally manufactured PCB. Therefore, since the circuit designed was voltage limited, the current drawn was 3-7x higher than what would be needed for a traditionally made equivalent board with copper traces.

The transceiver circuit however, did not completely function as intended. The RF portion did not end up working despite extensive redesign. The problem here is two-fold, the inaccuracies of dielectric deposition and the attachment method of the COTs components in this area. The RF network was designed to be used in conjunction with 10 μm thick polyimide, however, uniform and accurate thickness proved difficult. This is partially due to the material output changes of the polyimide ink during print time. Also, after the polyimide is on the substrate, it can get blown around by the air from the nozzle resulting in an uneven layer. The design employed was very sensitive to dielectric thickness, with several microns of thickness inaccuracy resulting in a non-functional matching network. Therefore, this sensitivity to the dielectric thickness needs to be reduced in future iterations. The size of the packages in the RF network, 0201, also made their attachment very difficult. Since the conductive epoxy used can
consume the polyimide dielectric, any overspill of the epoxy off the printed pads can result in a short. Ideally this would be dealt with by redesigning the matching network to use larger components.

Another shortcoming of the sensor was the repeatability of the product. Repeatability was not a focus of this research since the priority was a functional prototype. Of the 8 modules that were built completely, only 2 were programmable. Failure mechanisms were almost entirely regulated to shorts resulting from either misalignment or conductive epoxy shorting to the ground plane. The first failure mechanism can be solved with improved fiducial locations and alignment procedures. A solution to the latter failure mode is described in the Future Work section.

The use of a precisely dispensed AJP dielectric was also leveraged to improve the yield of microphones in an acoustic sensor. This technique was needed to shield the exposed edge of the silicon chip from the wire bonds. This process exhibited a repeatability to the dielectric application that was absent from the prior process. Two passes of the polyimide resulted in a yield increase of 25% when compared to a sensor packaged with hand spread dielectric.

The applicability of the sidewall interconnect process was also shown for another design, a MEMS acoustic sensing array. Instead of just shielding the exposed silicon edge from the wire bonds as was a previously mentioned, the design was taken a step further and the wire bonds were replaced with integration lines. Therefore, the integration lines were used to connect the sensor to the package. This application also benefits from the low profile nature of this integration method as compared with wire bonds. However, yield is an issue for this process with approximately 57% of the microphones functional. More research needs to be done to improve the yield of this process.

The effects of rapidly ageing several AJP inks was also analyzed with respect to several test environments. These tests concluded that the primary mechanism of failure for the printed inks was adhesion. This finding is contiguous with other researchers’ work on modes of printed electronics failure. Average resistance of the modules appeared to be much more consistent throughout the tests.
These results indicate that AJP inks can be effectively used in many moderate environments. However, extreme environments may result in adhesion issues leading to device failure. This in itself can be leveraged for vanishing electronics. With the reduced adhesion of the conductors, they feasibly could be physically wiped away with much less effort than conductors on traditionally manufactured PCBs.

In conclusion, leveraging aerosol jet printing technology is a viable method for rapid prototyping complex functional circuits along with assisting in the packaging of other technologies. The key advantages of this method are printability on topography including vertical package sidewalls, targeted deposition of small width conductors and insulators, rapid manufacturing time and flexibility with respect to ink, substrate and sintering method used. Aerosol jet printing technology can be effectively leveraged for rapid prototyping applications, however it does have its limitations. Primary difficulties include uniform material deposition, trace resistivity, alignment challenges and repeatability. The latter two challenges can be solved with more research while the former two are more inherent to the process and the ink used. Therefore, if the goal is to expedite the design cycle and create flexible and functional, but not optimal, circuits, the implemented manufacturing process researched is a viable option.

7.2 Future Work

There are several key areas for future work with the development of the transceiver circuit. One area is the application of the process to a variety of substrates, including flexible and low temperature. Flexible Kapton® was printed on early in the process with promising results, however, many circuit redesigns have happened since. Integration of the photonic annealer into the process also could functionalize many low temperature materials as substrates. Initial tests with the photonic annealer showed successful sintering of the ground plane, but issues were encountered when sintering the upper silver layer of the multilayer stack. Primarily it appears that the dielectric off-gassed violently causing the upper silver layer to blow off. This should be fixable with more careful sintering of the dielectric. Use of the photonic annealer will also greatly reduce the manufacturing time of the transceiver circuit. Using
the higher temperature cure process as a comparison because it is the faster of the two processes done, the photonic annealer curing the conductive layers would save two hours of the manufacturing time. That’s almost a 30% reduction in manufacturing time for the circuit solely from changing the conductor sintering method. Such demonstrations would prove the flexibility of the designed process and the capability to rapidly manufacture prototypes for a plethora of environments.

Another area of future work is the redesign of the circuit so that all components can be integrated through AJP technology. In the process developed in this thesis, only the QFN48 package was integrated with AJP technology. Such a design could greatly reduce fabrication time as it would remove the hand placement procedure used for most of the COTs components in this thesis. This would almost certainly involve using a pick-and-place tool to set COTs locations in a repeatable manner. In order for this to work, space between the components and their orientation must be adjusted to make the integration process as straightforward as possible.

Expanding the AJP ink material set is another goal of future work. By expanding the material set that can be used, more applications in niche environments such as the human body can be enabled. Non-metallic conductors, such as carbon nanotubes, can be more effectively functionalized to create such circuits. Similarly, flexible conductors could be used to develop a truly flexible transceiver circuit. More work can also be done in the ink ageing and reliability component of this research. Expanding the repertoire of inks tested could increase the application areas for AJP circuit boards. For example, finding a reliable, non-metallic, low resistance conductor that can be aerosol jet printed could have big implications in x-ray invisible and biocompatible circuit design.

Shorts have rendered the RF portion of this circuit non-functional. There are two potential reasons for this, inadequate dielectric thickness or the inaccurate placement of conductive epoxy on the 0201 pads. The second problem can be fixed through design changes to the matching network. By spreading
the network out, increasing the COTs package sizes in this section and by exploring alternate integration methods such as was used with the QFN48 package, shorts in this area would be greatly reduced.

Lastly, the MEMs acoustic sensor with sidewall integration lines between the sensor and the package could be improved. This process resulted in only 57% percent yield of the microphone array. Shorts appear to be happening between many of the individual microphones. This could potentially be from pinholes in the C-7 used to shield the exposed silicon on the sensor sidewall. More effectively shielding the sidewall and analyzing exactly how the microphones failed is the next step in future work.
References


Figure 0.1: The ADS design space is shown above
Ink Ageing Dielectric Breakdown Tests

Tests to whether the dielectric break down voltage in a 20V or less regime were done to determine if the dielectric was strong enough for multilayer circuit board applications. The dielectric breakdown tests were conducted with a voltage sweep on the structure shown in Figure 6.1. The voltage sweep was done by a Keithley 2400 sourcemeter. The maximum voltage applied was 20V due to current limits. According to comparisons with commercial polyimide dielectric from DuPont, this voltage is orders of magnitude lower than the breakdown voltage. In fact, no current can be observed leaking through the dielectric with the equipment. This test was conducted throughout the ageing tests with similar results. Figure 0.2 and Figure 0.3 are representative plots for what the data looks like across all tests at all time periods. As predicted, the voltage range for polyimide failure is not reached regardless of the ageing processes done to the modules. Both plots show measurement noise rather than actual current leakage data.
Figure 0.2: This plot is of the dielectric strength test for a CNT module on the thermal shock wafer. The module was tested to determine if current was leaking through the dielectric. As can be seen, the plot only captures measurement noise, showing no current leaking can be observed with the equipment.
Figure 0.3: This plot is of the dielectric strength test for a silver module on the moisture and insulation resistance test. This test was done after the first round of exposure to the environment (1 day). As can be seen only measurement noise is captured in the data. No current leakage is able to be observed.

**Ink Ageing Data Analysis MatLab Script**

```
filename= 'RGP Probe Results _Master_List_Spring_2015editedForMatlab.xlsx';

sheet265= ['Wafer265-1'; 'Wafer265-2'; 'Wafer265-3'; 'Wafer265-4'; 'Wafer265-5'];
cellsheet265=cellstr(sheet265);
Wafer265=zeros(16,12,5);
Wafer265CNT=zeros(16,12,5);
for i=1:5
  S=cellsheet265{i};
x11Range= 'C3:N10';
x12Range= 'C13:N20';
field=S;
TopRow = xlsread(filename,S,x11Range);
BottomRow = xlsread(filename,S,x12Range);
Age_265=[TopRow; BottomRow];
Wafer265(:, :, i)=Age_265;

x1CNT1Range='C25:N32';
```
xCNT2Range='C36:N43';
TopRowCNT=xlsread(filename,S,xCNT1Range);
BottomRowCNT=xlsread(filename,S,xCNT2Range);
Age_265CNT=[TopRowCNT; BottomRowCNT];
Wafer265CNT(:, :, i)=Age_265CNT;
end

sheet266 = ['Wafer266-1'; 'Wafer266-2'; 'Wafer266-3';'Wafer266-4';'Wafer266-5'];
cellsheet266=cellstr(sheet266);
Wafer266=zeros(16,12,5);
Wafer266CNT=zeros(16,12,5);
for i=1:5
    S=cellsheet266{i};
xl1Range='C3:N10';
xl2Range='C13:N20';
field=S;
TopRow = xlsread(filename,S,xl1Range);
%doesn't like to read in NaN's, so I added them later
if i==5
    x=NaN(1,8);
y=NaN(8,4);
    TopRowTopNaN=[x; TopRow];
    TopRow=[TopRowTopNaN, y];
end
BottomRow = xlsread(filename,S,xl2Range);
Age_266=[TopRow; BottomRow];
Wafer266(:, :, i)=Age_266;
xCNT1Range='C25:N32';
xCNT2Range='C36:N43';
TopRowCNT=xlsread(filename,S,xCNT1Range);
BottomRowCNT=xlsread(filename,S,xCNT2Range);
Age_266CNT=[TopRowCNT; BottomRowCNT];
Wafer266CNT(:, :, i)=Age_266CNT;
end

sheet59F= ['AGCNTprint59F_1'; 'AGCNTprint59F_2';
'AGCNTprint59F_3';'AGCNTprint59F_4';'AGCNTprint59F_5';'AGCNTprint59F_6'];
cellsheet59F=cellstr(sheet59F);
Wafer59F=zeros(8,14,6);
Wafer59FCNT=zeros(8,12,6);
for i=1:6
    S=cellsheet59F{i};
xl1Range='H4:U11';
field=S;
Age_59F = xlsread(filename,S,xl1Range);
Wafer59F(:, :, i)=Age_59F;
xCNT1Range='F44:Q51';
AgeCNT_59F = xlsread(filename,S,xCNT1Range);
Wafer59FCNT(:, :, i)=AgeCNT_59F;
end
% Getting Percent Change R/Ro
% Wafer 265
HourCount=[24; 48; 72; 120];
W265A(:,:,1)=Wafer265(:,:,2)./Wafer265(:,:,1);
W265A(:,:,2)=Wafer265(:,:,3)./Wafer265(:,:,1);
W265A(:,:,3)=Wafer265(:,:,4)./Wafer265(:,:,1);
W265A(:,:,4)=Wafer265(:,:,5)./Wafer265(:,:,1);
W265ACNT(:,:,1)=Wafer265CNT(:,:,2)./Wafer265CNT(:,:,1);
W265ACNT(:,:,2)=Wafer265CNT(:,:,3)./Wafer265CNT(:,:,1);
W265ACNT(:,:,3)=Wafer265CNT(:,:,4)./Wafer265CNT(:,:,1);
W265ACNT(:,:,4)=Wafer265CNT(:,:,5)./Wafer265CNT(:,:,1);

% resistance change R/Ro
MeanSTD265=zeros(4,3);
MeanSTD265CNT=zeros(4,3);
for i=1:4
    Array=W265A(:,:,i);
    columnMean=nanmean(Array);
    ArrayMean=nanmean(columnMean);
    ArrayVar=nanvar(Array);
    MeanVar=nanmean(ArrayVar);
    ArraySTD=sqrt(MeanVar);
    MeanSTD265(i,:)=[HourCount(i),ArrayMean, ArraySTD];
end

figure(1);
h=errorbar(HourCount, ArrayMean, ArraySTD, '-ob');
s1=h.MarkerFaceColor;
h.MarkerFaceColor='blue';
title('Silver Ink Moisture and Insulation Resistance IPC-TM-650-2.6.3F(50C/85R.H.)')
xlabel('Hours')
ylabel('Resistance Change R/Ro')
hold on;

ArrayCNT=W265ACNT(:,:,i);
columnMean=nanmean(ArrayCNT);
ArrayMeanCNT=nanmean(columnMean);
ArrayVar=nanvar(ArrayCNT);
MeanVar=nanmean(ArrayVar);
ArraySTD= nanvar(ArrayVar);
MeanSTD265CNT(i,:)=[HourCount(i),ArrayMeanCNT, ArraySTD];

figure(2);
h=errorbar(HourCount, ArrayMeanCNT, ArraySTD, '-ob');
s1=h.MarkerFaceColor;
h.MarkerFaceColor='blue';
title('CNT Ink Moisture and Insulation Resistance IPC-TM-650-2.6.3F (50C/85R.H.)')
xlabel('Hours')
ylabel('Resistance Change R/Ro')
hold on;
%two nan counter plots to monitor number of failed modules
HourCount2=[0; 24; 48; 72; 120];
NaN265=zeros(5,2);
NaN265CNT=zeros(5,2);

for i=1:5
    Array=Wafer265(:,:,i);
    NanFinder=isnan(Array); %NaNFinder!
    NanSum1=sum(NanFinder);
    TotalNan=sum(NanSum1);
    percentfail=TotalNan/192*100;
    NaN265(i,:)=[HourCount2(i), TotalNan];

    figure(3);
    xlabel('Hours'), 30,'FontSize')
    ylabel('Percentage of Failed Modules'), 30,'FontSize')
    title('Ag Ink Moisture and Insulation Resistance IPC-TM-650-2.6.3F (50C/85R.H.)')
    h2=plot(HourCount2(i), percentfail, '-ob');
    s2=h2.MarkerFaceColor;
    h2.MarkerFaceColor='blue';
    hold on;

    ArrayCNT=Wafer265CNT(:,:,i);
    NanFinder=isnan(ArrayCNT); %NaNFinder!
    NanSum1=sum(NanFinder);
    TotalNan=sum(NanSum1);
    percentfail=TotalNan/192*100;
    NaN265CNT(i,:)=[HourCount2(i), TotalNan];

    figure(4);
    xlabel('Hours'), 30,'FontSize')
    ylabel('Percentage of Failed Modules'), 30,'FontSize')
    title('CNT Ink Moisture and Insulation Resistance IPC-TM-650-2.6.3F (50C/85R.H.)')
    h2=plot(HourCount2(i), percentfail, '-ob');
    s2=h2.MarkerFaceColor;
    h2.MarkerFaceColor='blue';
    hold on;
end

%Getting Percent Change R/Ro
%Wafer 266

W266A(:,:,1)=Wafer266(:,:,2)./Wafer266(:,:,1);
W266A(:,:,2)=Wafer266(:,:,3)./Wafer266(:,:,1);
W266A(:,:,3)=Wafer266(:,:,4)./Wafer266(:,:,1);
W266A(:,:,4)=Wafer266(:,:,5)./Wafer266(:,:,1);

W266ACNT(:,:,1)=Wafer266CNT(:,:,2)./Wafer266CNT(:,:,1);
W266ACNT(:,:,2)=Wafer266CNT(:,:,3)./Wafer266CNT(:,:,1);
W266ACNT(:,:,3)=Wafer266CNT(:,:,4)./Wafer266CNT(:,:,1);
W266ACNT(:,:,4) = Wafer266CNT(:,:,5)/Wafer266CNT(:,:,1);

MeanSTDNa266 = zeros(4,3);
MeanSTDNa266CNT = zeros(4,3);
CycleCount = [50;150;379;1000];

% R/Ro
for i = 1:4
    Array = W266A(:,:,i);
    columnMean = nanmean(Array);
    ArrayMean = nanmean(columnMean);
    ArrayVar = nanvar(Array);
    MeanVar = nanmean(ArrayVar);
    ArraySTD = sqrt(MeanVar);
    MeanSTDNaN266(i,:) = [CycleCount(i), ArrayMean, ArraySTD];
end

figure(5);
hold on;
ArrayCNT = W266ACNT(:,:,i);
ArrayMeanCNT = nanmean(columnMean);
ArrayVar = nanvar(ArrayCNT);
MeanVar = nanmean(ArrayVar);
ArraySTD = sqrt(MeanVar);
MeanSTDNaN266CNT(i,:) = [CycleCount(i), ArrayMeanCNT, ArraySTD];
end

%two nan counter plots to monitor number of failed modules
CycleCount2 = [0;50;150;379;1000];
NaN266 = zeros(5,2);
NaN266CNT = zeros(5,2);

for i = 1:5
    Array = Wafer266(:,:,i);
    NaNFinder = isnan(Array);  % NaNFinder!
    NaNSum1 = sum(NanFinder);
    TotalNan = sum(NanSum1);
percentfail=TotalNan/192*100;
NaN266(i,:)=[CycleCount2(i),TotalNan];

figure(6);
h2=plot(CycleCount2(i), percentfail,'-ob');
s2=h2.MarkerFaceColor;
h2.MarkerFaceColor='blue';
title('Silver Ink Thermal Shock Test IPC-TM-650-2.6.7.2a (-55C/125C)')
xlabel('Cycles') %,'FontSize', 30)
ylabel('Percentage of Failed Modules') %,'FontSize', 30)
hold on;

ArrayCNT=Wafer266CNT(:,:,i);
NanFinder=isnan(ArrayCNT); %NaNFinder!
NanSum1=sum(NanFinder);
TotalNan=sum(NanSum1);
percentfail=TotalNan/192*100;
NaN266(i,:)=[CycleCount2(i),TotalNan];

figure(8);
h2=plot(CycleCount2(i), percentfail,'-ob');
s2=h2.MarkerFaceColor;
h2.MarkerFaceColor='blue';
title('CNT Ink Thermal Shock Test IPC-TM-650-2.6.7.2a (-55C/125C)')
xlabel('Cycles') %,'FontSize', 30)
ylabel('Percentage of Failed Modules') %,'FontSize', 30)
hold on;
end

%Getting Percent Change R/Ro
%Wafer 59F

W59FA(:,:,1)=Wafer59F(:,:,2)./Wafer59F(:,:,1);
W59FA(:,:,2)=Wafer59F(:,:,3)./Wafer59F(:,:,1);
W59FA(:,:,3)=Wafer59F(:,:,4)./Wafer59F(:,:,1);
W59FA(:,:,4)=Wafer59F(:,:,5)./Wafer59F(:,:,1);
W59FA(:,:,5)=Wafer59F(:,:,6)./Wafer59F(:,:,1);

W59FCNTA(:,:,1)=Wafer59FCNT(:,:,2)./Wafer59FCNT(:,:,1);
W59FCNTA(:,:,2)=Wafer59FCNT(:,:,3)./Wafer59FCNT(:,:,1);
W59FCNTA(:,:,3)=Wafer59FCNT(:,:,4)./Wafer59FCNT(:,:,1);
W59FCNTA(:,:,4)=Wafer59FCNT(:,:,5)./Wafer59FCNT(:,:,1);
W59FCNTA(:,:,5)=Wafer59FCNT(:,:,6)./Wafer59FCNT(:,:,1);

MeanSTDNaN9F=zeros(5,3);
DayCount2=[30; 59; 91; 136; 199];
for i=1:5
    Array=W59FA(:,:,i);
    columnMean=nanmean(Array);
    ArrayMean=nanmean(columnMean);
    ArrayVar=nanvar(Array);
    MeanVar=nanmean(ArrayVar);
    ArraySTD=sqrt(MeanVar);
    MeanSTDNaN9F(i,:)=[DayCount2(i), ArrayMean,ArraySTD];
figure(9);
h=errorbar(DayCount2(i), ArrayMean, ArraySTD, '-ob');
s1=h.MarkerFaceColor;
h.MarkerFaceColor='blue';
title('Silver Ink Elevated Temperature Ageing (60C)')
xlabel('Days'); ylabel('Resistance Change R/Ro')
hold on;

ArrayCNT=W59FCNTA(:, :, i);
columnMean=nanmean(ArrayCNT);
ArrayMeanCNT=nanmean(columnMean);
ArrayVar=nanvar(Array);
MeanVar=nanmean(ArrayVar);
ArraySTDCNT=sqrt(MeanVar);
MeanSTDNaN59F(i, :)=[DayCount2(i), ArrayMeanCNT, ArraySTDCNT];

figure(10);
h=errorbar(DayCount2(i), ArrayMeanCNT, ArraySTDCNT, '-ob');
s1=h.MarkerFaceColor;
h.MarkerFaceColor='blue';
title('CNT Ink Elevated Temperature Ageing (60C)')
xlabel('Days'), ylabel('Resistance Change R/Ro')
hold on;
end

DayCount3=[0; 30; 59; 91; 136; 199];
NaN59F=zeros(6, 2);
NaN59FCNT=zeros(6, 2);

for i=1:6
    Array2=Wafer59F(:, :, i);
    NanFinder=isnan(Array2); %NanFinder!
    NanSum1=sum(NanFinder);
    TotalNan=sum(NanSum1);
    percentfail=TotalNan/112*100;
    NaN59F(i, :)=[DayCount3(i), TotalNan];

figure(11);
h2=plot(DayCount3(i), percentfail, '-ob'); %fail
s2=h2.MarkerFaceColor;
h2.MarkerFaceColor='blue';
title('Silver Ink Elevated Temperature Ageing (60C)')
xlabel('Days'), ylabel('Percentage of Failed Modules')
hold on;

%CNT
Array2CNT=Wafer59FCNT(:, :, i);
NanFinder=isnan(Array2CNT); %NanFinder!
NanSum1=sum(NanFinder);
TotalNan=sum(NanSum1);
percentfail=TotalNan/112*100;
NaN59FCNT(i,:)=[DayCount3(i), TotalNan];

figure(12);
h2=plot(DayCount3(i), percentfail,'-ob'); %fail
s2=h2.MarkerFaceColor;
h2.MarkerFaceColor='blue';
title('CNT Ink Elevated Temperature Ageing (60C)')
xlabel('Days') %, 'FontSize', 30)
ylabel('Percentage of Failed Modules') %,'FontSize', 30)
hold on;

end